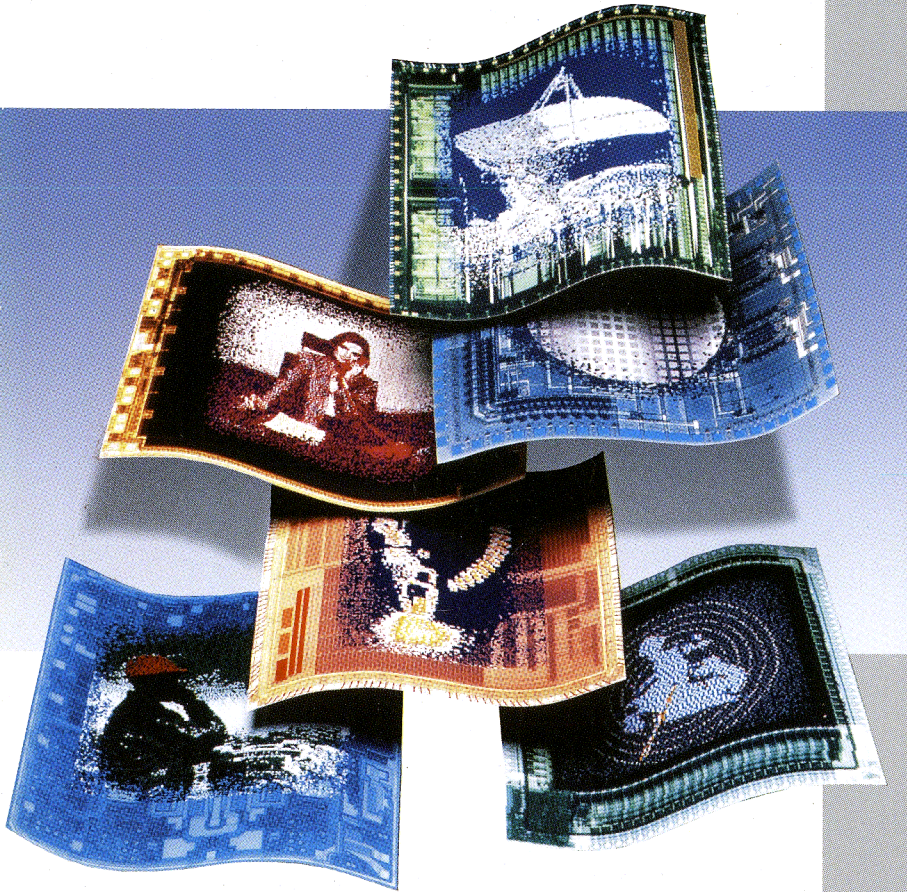


# *Personal Communications*

August 1994

## *IC Handbook*



## **DATASHEET ANNOTATION**

GPS annotate datasheets in the top right hand corner of the first page, to indicate product status. These annotations are as follows:-

### **TARGET SPECIFICATION**

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

### **PRELIMINARY INFORMATION**

The product is in design and development. The datasheet represents the product as it is understood but details may change.

### **ADVANCE INFORMATION**

The product design is complete and final characterisation for volume production is well in hand.

### **No annotation**

The product parameters are fixed and the product is available to datasheet specification in volume.

If you have any queries about the status of any GPS product, please contact your nearest GPS Customer Service Centre.



# PERSONAL COMMUNICATIONS

IC Handbook



# Foreword

This latest Personal Communications IC Handbook from GEC Plessey Semiconductors introduces numerous new devices for this rapidly expanding market. GEC Plessey Semiconductors has been involved in many successful wireless communications projects, providing a vital link between high performance and cost effective implementations in applications as diverse as credit card pagers and digital cordless telephones.

These applications share a number of common goals, small size and low power are paramount, and these are also the goals of our IC design teams. New products such as the SP8715 family of prescalers offer low voltage and low current consumption using state of the art sub micron bipolar processes, whilst the SL6609 direct conversion paging receiver offers improved sensitivity and reduced board area over its predecessor. CMOS developments include higher functionality synthesisers with features such as Fractional N interpolation for improved locking speed and a POCSAG paging decoder to compliment the SL6609.

High performance extends to packaging and all the components in this handbook are offered in industry standard surface mount packages, with latest developments using fine lead pitches of 0.65 and 0.5mm.

Finally, the Quality Assurance programmes that are applied to GEC Plessey Semiconductors products (from consumer electronics to defense projects) are applied to all Personal Communications products with rigour. Performance and long term reliability are therefore guaranteed in what can be a demanding operating environment.

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## Product List - by circuit type

### PLLs (Phased Lock Loop)

Type No.	Description	Page
NJ8820	Frequency synthesiser (PROM interface)	9
NJ8821	Frequency synthesiser (microprocessor interface) with resettable counters	14
NJ88C22**	Frequency synthesiser (microprocessor serial interface)	18
NJ8823**	Frequency synthesiser (microprocessor interface) with non-resettable counters	23
NJ88C24**	Frequency synthesiser (microprocessor serial interface)	27
NJ88C25**	Frequency synthesiser (microprocessor serial interface)	32
NJ88C28	Frequency synthesiser (microprocessor serial interface) with non-resettable counters	37
NJ88C29	Frequency synthesiser (microprocessor serial interface) with non-resettable counters	43
NJ88C30**	VHF synthesiser	49
NJ88C33	Frequency synthesiser (I2C bus programmable) with current source outputs	54
NJ88C50	Dual low power frequency synthesiser	64

### IF Products

Type No.	Description	Page
SL6601C**	FM IF, PLL detector (double conversion) and RF mixer	79
SL6652**	Low power IF/AF circuit for FM cellular radio	85
SL6654**	Low power IF/AF circuit for FM cellular radio	92
SL6659	Low power IF/AF circuit (with RSSI) for FM radio	98

### Prescalers

Type No.	Description	Page
SP8704**	950MHz very low current divide by 128/129 or 64/64	109
SP8713	1100MHz very low current three modulus divider	111
SP8714	2100MHz very low current multi-modulus divider	118
SP8715	1100MHz very low current multi-modulus divider	125
SP8716/8/9	520MHz divide by 40/41 + 64/64 + 80/81	132
SP8789	225MHz divide by 20/21 two modulus divider	135
SP8792/3	520MHz divide by 80/81 + 40/41	138
SP8795	225MHz divide by 32/33	141
SP8799	225MHz divide by 10/11	144

## RF Front Ends

Type No.	Description	Page
SL6442	1GHz amplifier/mixer	149
SL6444	1GHz amplifier/mixer	159

## Amplifiers

Type No.	Description	Page
SL562	Low noise programmable op-amp	175
SL1610	RF/IF Amplifier	178
SL6140	400MHz wideband AGC amplifier	181
SL6270C	Gain controlled pre-amplifier	189
SL6310C	Switchable audio amplifier	192

## CODEC

Type No.	Description	Page
MV3100	3V CODEC with analog interface for digital mobile telephones	197

## Paging Receivers & Decoders

Type No.	Description	Page
MV6639	POCSAG decoder	215
MV6640*	POCSAG decoder	234
SL6609	Direct conversion FSK data receiver	235
SL6619*	450MHz direct conversion receiver with AFC	248
SL6649-1	200MHz direct conversion FSK data receiver	249

\* Outline or development details only - contact GPS Customer Services (see page 359)

\*\* For maintenance purposes only

# Product List - alpha numeric

Type No.	Description	Page
MV3100	3V CODEC with analog interface for digital mobile telephones	197
MV6639	POCSAG decoder	215
MV6640*	POCSAG decoder	234
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NJ88C25**	Frequency synthesiser (microprocessor serial interface)	32
NJ88C28	Frequency synthesiser (microprocessor serial interface) with non-resettable counters	37
NJ88C29	Frequency synthesiser (microprocessor serial interface) with non-resettable counters	43
NJ88C30**	VHF synthesiser	49
NJ88C33	Frequency synthesiser (I2C bus programmable) with current source phase detector outputs	54
NJ88C50	Dual low power frequency synthesiser	64
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SL6270C	Gain controlled pre-amplifier	189
SL6310C	Switchable audio amplifier	192
SL6442	1GHz amplifier/mixer	149
SL6444	1GHz amplifier/mixer	159
SL6601C**	FM IF, PLL detector (double conversion) and RF mixer	79
SL6609	Direct conversion FSK data receiver	235
SL6619*	450MHz direct conversion receiver with AFC	248
SL6649-1	200MHz direct conversion FSK data receiver	249
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SP8714	2100MHz very low current multi-modulus divider	118
SP8715	1100MHz very low current multi-modulus divider	125
SP8716	520MHz divide by 40/41	132
SP8718	520MHz divide by 64/64	132
SP8719	520MHz divide by 80/81	132
SP8789	225MHz divide by 20/21	135
SP8792	225MHz divide by 80/81	138
SP8793	225MHz divide by 40/41	138
SP8795	225MHz divide by 32/33	141
SP8799	225MHz divide by 10/11	144

\* Outline or development details only - contact GPS Customer Services (see page 359)  
 \*\* For maintenance purposes only



# Section 1

## PLLs (Phased Lock Loop)





# NJ8820

## FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory, with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of  $-30^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . The NJ8820MA is available only in Ceramic DIL package with operating temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- $>10\text{MHz}$  Input Frequency

### ORDERING INFORMATION

**NJ8820 BA DP** Plastic DIL Package

**NJ8820 BA MP** Miniature Plastic DIL Package

**NJ8820 MA DG** Ceramic DIL Package

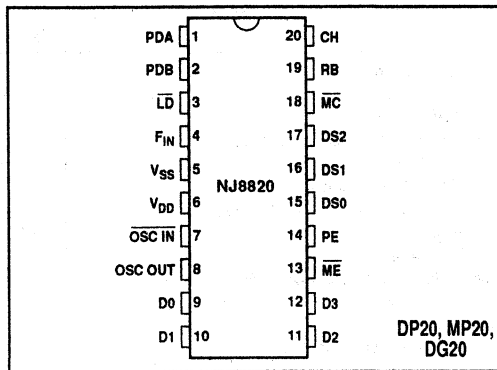


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD} - V_{SS}$	-0.5V to 7V
Input voltage	-0.5V to 7V
Open drain outputs, pins 3 and 13	7V
All other pins	$V_{SS} - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$
Storage temperature	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
	(DG package, NJ8820MA)
Storage temperature	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
	(DP and MP packages, NJ8820)

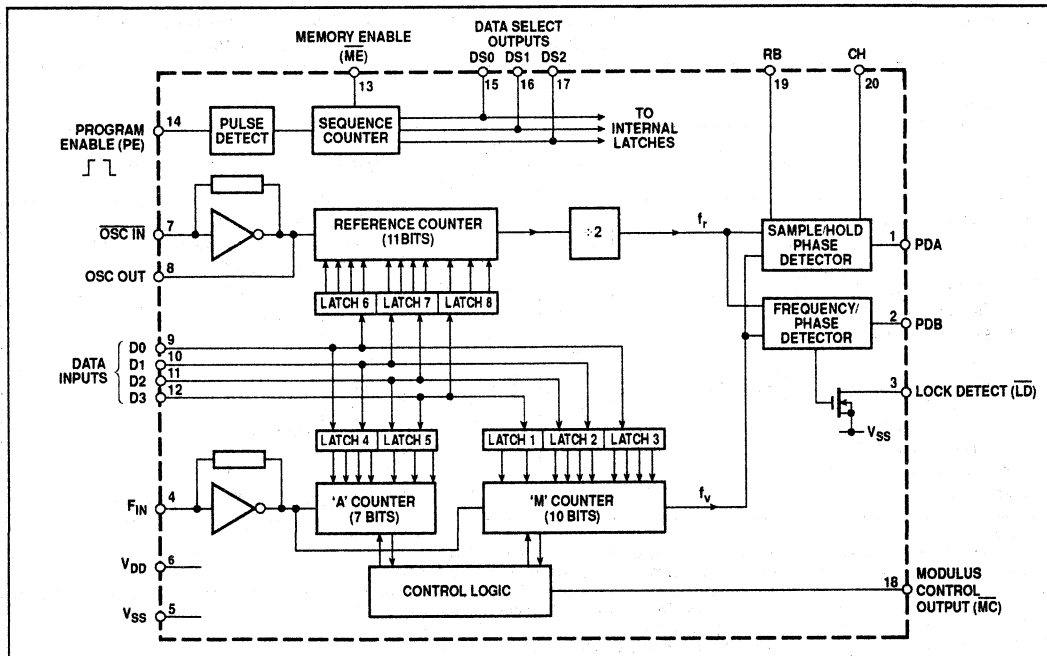


Fig.2 Block diagram

# NJ8820

## ELECTRICAL CHARACTERISTICS AT $V_{DD} = 5V$

Test conditions unless otherwise stated:

$V_{DD} - V_{SS} = 5V \pm 0.5V$ . Temperature range NJ8820 BA:  $-30^{\circ}C$  to  $+70^{\circ}C$ ; NJ8820 MA:  $-40^{\circ}C$  to  $+85^{\circ}C$

### DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	$f_{OSC}, f_{FIN} = 10MHz$ } 0 to 5V square wave $f_{OSC}, f_{FIN} = 1.0MHz$ }
<b>OUTPUT LEVELS</b>		0.7	1.5	mA	
<b>Memory Enable Output (<math>\overline{ME}</math>)</b>					$I_{SINK} = 4mA$
Low level			0.4	V	
Open drain pull-up voltage			7	V	
<b>Data Select Outputs (DS0-DS2)</b>					$I_{SOURCE} = 1mA$ $I_{SINK} = 2mA$
High level	4.6			V	
Low level			0.4	V	
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>					$I_{SOURCE} = 1mA$ $I_{SINK} = 1mA$
High level	4.6			V	
Low level			0.4	V	
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					$I_{SINK} = 4mA$
Low level			0.4	V	
Open drain pull-up voltage			7	V	
<b>PDB Output</b>					$I_{SOURCE} = 5mA$ $I_{SINK} = 5mA$
High level	4.6			V	
Low level			0.4	V	
3-state leakage current			$\pm 0.1$	$\mu A$	
<b>INPUT LEVELS</b>					TTL compatible See note 1
<b>Data Inputs (D0-D3)</b>					
High level	4.25			V	
Low level			0.75	V	
<b>Program Enable Input (PE)</b>					$V_{BIAS} = \text{self-bias point of PE}$ (nominally $V_{DD}/2$ )
Trigger level	$V_{BIAS}$ $\pm 100mV$			V	

### AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$f_{IN}$ and $OSC$ IN input level	200			mVRMS	10MHz AC-coupled sinewave Input squarewave $V_{DD}$ to $V_{SS}$ . See note 5.
Max. operating frequency, $f_{FIN}$ and $f_{OSC}$	10.6			MHz	
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2. Pulse to $V_{SS}$ or $V_{DD}$ .
PE pulse length, $t_W$	5			$\mu s$	
Data set-up time, $t_{DS}$	1			$\mu s$	See note 3.
Data hold time, $t_{DH}$	10			ns	
Digital phase detector propagation delay		500		ns	See note 3.
Gain programming resistor, RB	5			k $\Omega$	
Hold capacitor, CH			1	nF	See note 3.
Output resistance, PDA			5	k $\Omega$	
Digital phase detector gain		0.4		V/Rad	10% to 90%, see note 4.
Power supply rise time	100			$\mu s$	

#### NOTES

- Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
- All counters have outputs directly synchronous with their respective clock rising edges.
- The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ , typically.
- To ensure correct operation of power-on programming.
- Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD} - V_{SS})/2$ when the system is in lock. Voltage increases as $f_V$ phase lead increases; voltage decreases as $f_r$ phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or $f_V$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_V < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_V = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	$F_{IN}$	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	$V_{SS}$	Negative supply (ground).
6	$V_{DD}$	Positive supply.
7, 8	$\overline{OSC IN}/OSC OUT$	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC IN}$ . This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9, 10, 11, 12	D0-D3	Information on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	$\overline{ME}$	An open drain output for use in controlling the power supply to an external ROM or PROM. $\overline{ME}$ is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC-coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15, 16, 17	DS0-DS2	Internally generated three-state data select outputs, which may be used to address external memory.
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP + A$ , where $P$ and $P + 1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $+128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio should be $P^2 - P$ .
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
20	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

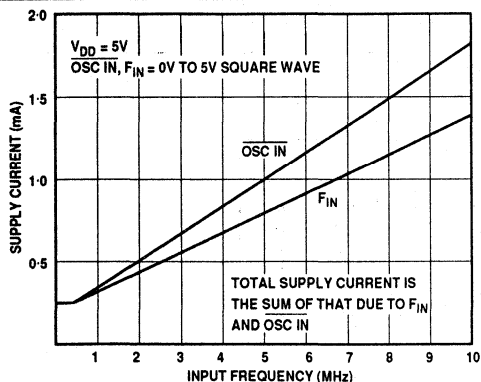


Fig. 3 Typical supply current v. input frequency

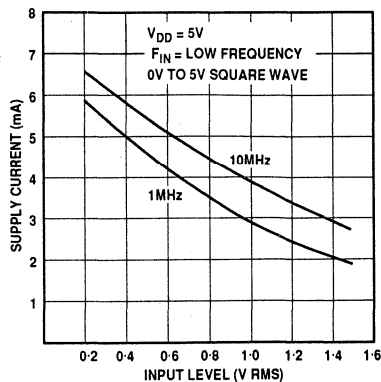


Fig. 4 Typical supply current v. input level,  $\overline{OSC IN}$

# NJ8820

## PROGRAMMING

Program information can be obtained from an external ROM or PROM under the control of the NJ8820. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data transfer time slot and may be used for external control purposes. A suitable PROM would be the 74S287, giving up to 32 channel capability as shown in Fig. 5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25µs.

Reading this data is normally done in single shot mode, with the data read cycle started by either a positive or negative pulse on the program enable (PE) pin. The data read cycle is generated from a program clock at 1/64 of the reference oscillator frequency. A memory enable signal (ME) is supplied to allow power-down of the ROM when it is not in use. Data select outputs (DS0-DS2) remain in a high impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram are shown in Figs. 6 to 8. Data is latched internally during the portions of the program cycle shown shaded in Fig. 7 and all data is transferred to the

counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded, causing the data read cycle to repeat cyclically to allow continuous up-dating of the program information. In this mode, external memory will be enabled continuously (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every  $1024/t_{OSC}$  seconds. This programming method is not recommended because of the higher power consumption and the possibilities of noise into the loop from the digital data lines.

## Power-on Programming

On power-up, the data read cycle is automatically initiated, making it unnecessary to provide a PE pulse. The circuit detects the power supply rising above a threshold point (nominally 1.5V) and, after an internally generated delay to allow the supply to rise fully, the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles, giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function, the power supply rise time should be less than 5ms (at 10MHz), rising smoothly through the threshold point.

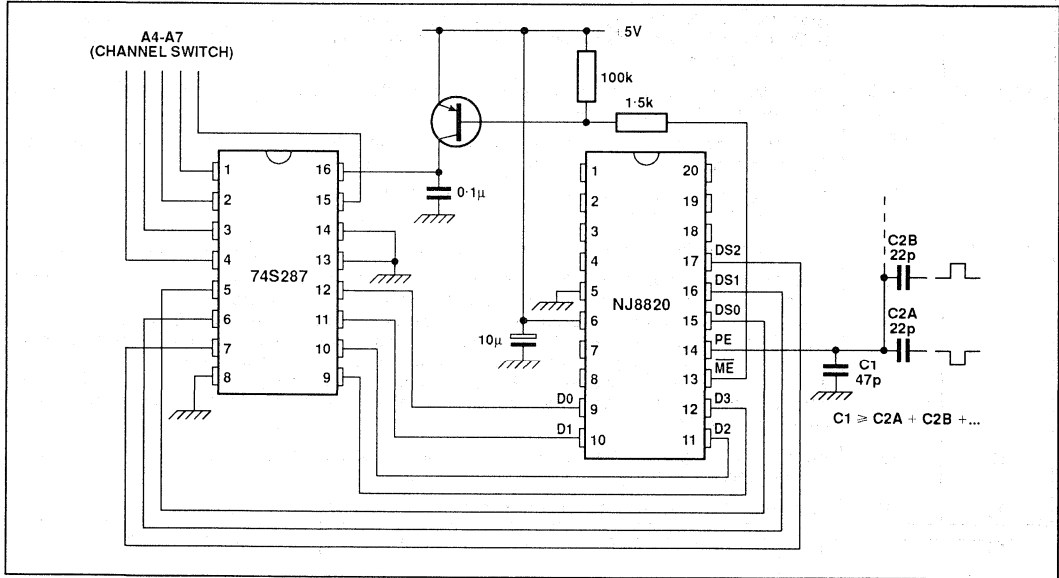


Fig. 5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 6 Data map

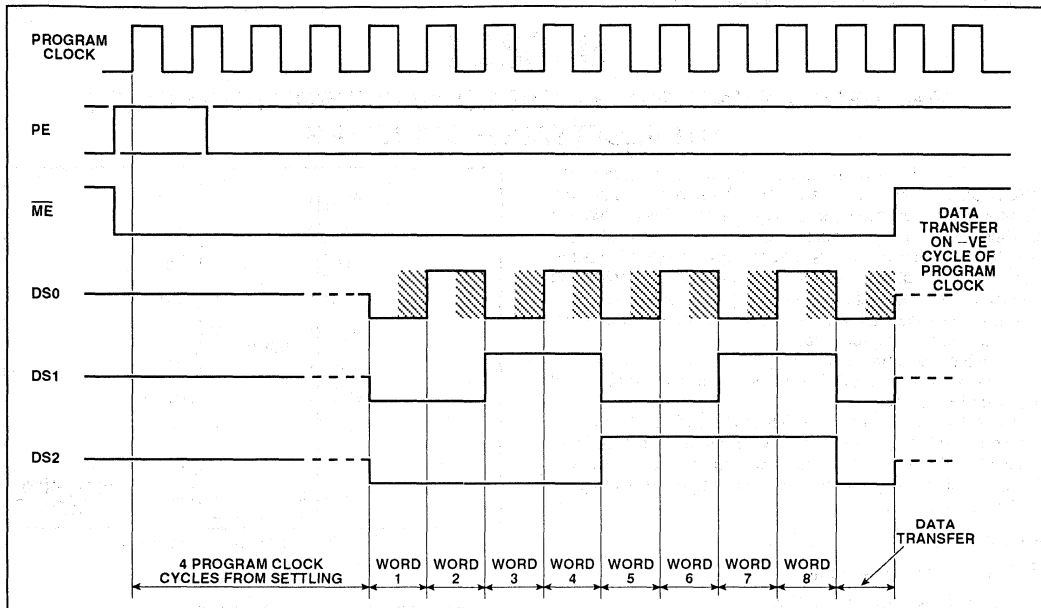


Fig.7 Data selection

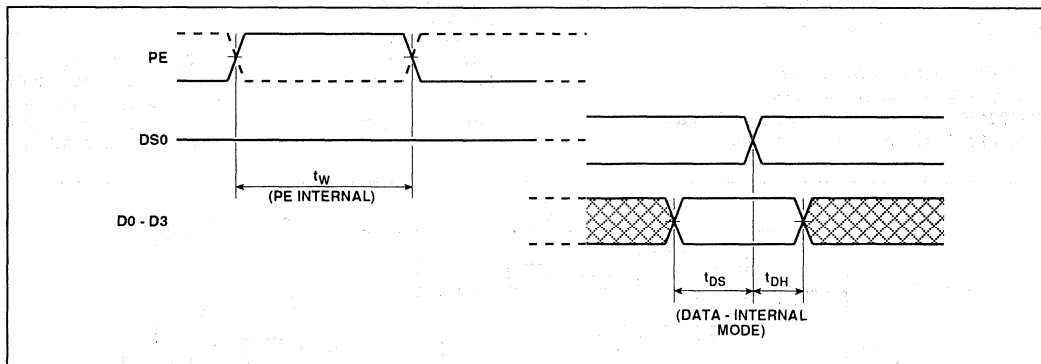


Fig.8 Timing diagram

**PHASE COMPARATORS**

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error. The relationship between this offset and the

phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 2.2kΩ is advised.

**PROGRAMMING/POWER UP**

Data and signal input pins should not have input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur.

# NJ8821

## FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor..

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of  $-30^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . The NJ8821MA is available only in Ceramic DIL package with operating temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### FEATURES

- Low Power Consumption
- Microprocessor Compatible
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

### ORDERING INFORMATION

**NJ8821 BA DP** Plastic DIL Package

**NJ8821 BA MP** Miniature Plastic DIL Package

**NJ8821 MA DG** Ceramic DIL Package

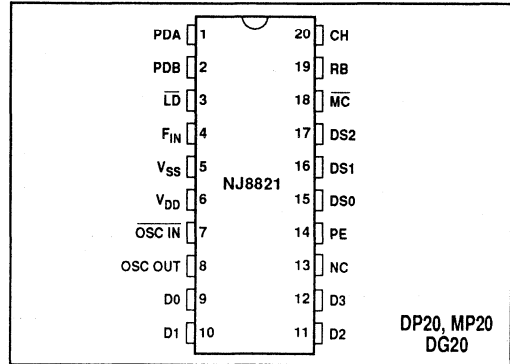


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD} - V_{SS}$	$-0.5\text{V}$ to $7\text{V}$
Input voltage	$-0.5\text{V}$ to $7\text{V}$
Open drain output, pin 3	$7\text{V}$
All other pins	$V_{SS} - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$
Storage temperature	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ (DG package, NJ8821MA)
Storage temperature	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (DP and MP packages, NJ8821)

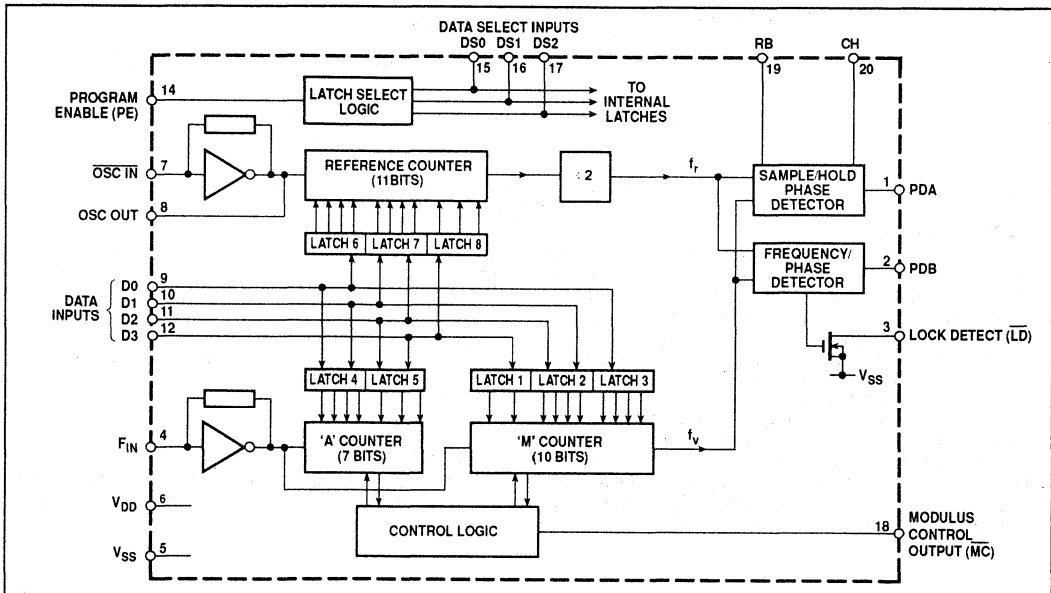


Fig.2 Block diagram



**ELECTRICAL CHARACTERISTICS AT  $V_{DD} = 5V$**

Test conditions unless otherwise stated:

$V_{DD} - V_{SS} = 5V \pm 0.5V$ . Temperature range NJ8821 BA:  $-30^{\circ}C$  to  $+70^{\circ}C$ ; NJ8821MA:  $-40^{\circ}C$  to  $+85^{\circ}C$

**DC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	$f_{OSC}, f_{FIN} = 10MHz$ } 0 to 5V square wave $f_{OSC}, f_{FIN} = 1.0MHz$ }
<b>OUTPUT LEVELS</b>		0.7	1.5	mA	
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>					
High level	4.6			V	$I_{SOURCE} = 1mA$ $I_{SINK} = 1mA$
Low level			0.4	V	
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					
Low level			0.4	V	$I_{SINK} = 4mA$
Open drain pull-up voltage			7	V	
<b>PDB Output</b>					
High level	4.6			V	$I_{SOURCE} = 5mA$ $I_{SINK} = 5mA$
Low level			0.4	V	
3-state leakage current			$\pm 0.1$	$\mu A$	
<b>INPUT LEVELS</b>					
<b>Data Inputs (D0-D3)</b>					TTL compatible See note 1
High level	4.25			V	
Low level			0.4	V	
<b>Program Enable Input (PE)</b>					
High level	4.25			V	
Low level			0.75	V	
<b>Data Select Inputs (DS0-DS2)</b>					
High level	4.25			V	
Low level			0.75	V	

**AC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$F_{IN}$ and $\overline{OSC}$ IN input level	200			mVRMS	10MHz AC-coupled sinewave Input squarewave $V_{DD}$ to $V_{SS}$ , See note 4.
Max. operating frequency, $f_{FIN}$ and $f_{OSC}$	10.6			MHz	
Propagation delay, clock to $\overline{MC}$		30	50	ns	} See Fig. 6
Strobe pulse width, $t_{W(ST)}$	2			$\mu s$	
Data set-up time, $t_{DS}$	1			$\mu s$	
Data hold time, $t_{DH}$	1			$\mu s$	
Latch address set-up time, $t_{SE}$	1			$\mu s$	
Latch address hold time, $t_{HE}$	1			$\mu s$	
Digital phase detector propagation delay		500		ns	} See note 3.
Gain programming resistor, RB	5			k	
Hold capacitor, CH			1	nF	
Output resistance, PDA			5	k	
Digital phase detector gain		0.4		V/Rad	

**NOTES**

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ , typically.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as $f_v$ phase lead increases; voltage decreases as $f_r$ phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or $f_v$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_v < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	$F_{IN}$	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	$V_{SS}$	Negative supply (ground).
6	$V_{DD}$	Positive supply.
7, 8	OSC IN/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to OSC IN. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9, 10, 11, 12	D0-D3	Data on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	NC	No connection
14	PE	This pin is used as a strobe for the data. A logic '1' on this pin transfers data from the D0-D3 pins to the internal latch addressed by the data select (DS0-DS2) pins. A logic '0' disables the data inputs.
15, 16, 17	DS0-DS2	Data select inputs for addressing the internal data latches
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\pm 128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio should be $P^2 - P$ .
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
20	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

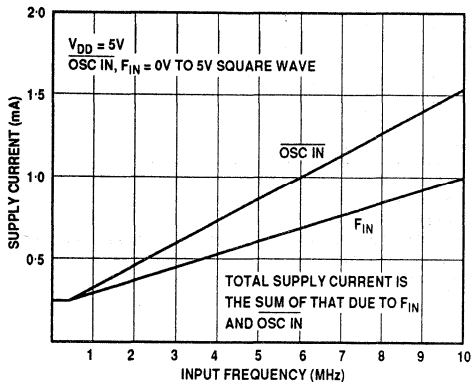


Fig. 3 Typical supply current v. input frequency

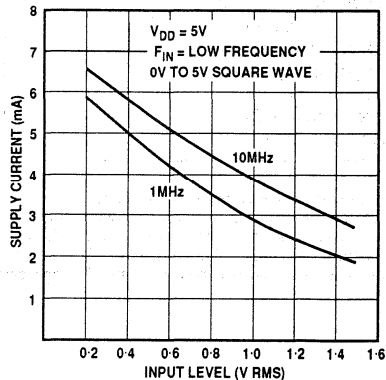


Fig. 4 Typical supply current v. input level,  $\overline{OSC IN}$

**PROGRAMMING**

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches as defined by the data map Fig. 5. The PE pin is used as a strobe for the data: taking PE high causes data to be transferred from the data pins (D0-D3) into the addressed latch. Following the falling edge of PE, the data is retained in the addressed latch and the data inputs are disabled. Data transfer from all internal latches into the counters occurs simultaneously with the transfer of data into latch 1, which would therefore normally be the last latch addressed during each channel change. Timing information for this mode of operation is given in Fig. 6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means that the synthesiser loop lock-up time is well defined and less than

10ms. If shorter lock-up times are required when making only small changes in frequency, the GPS NJ8823 (with non-resettable counters) should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

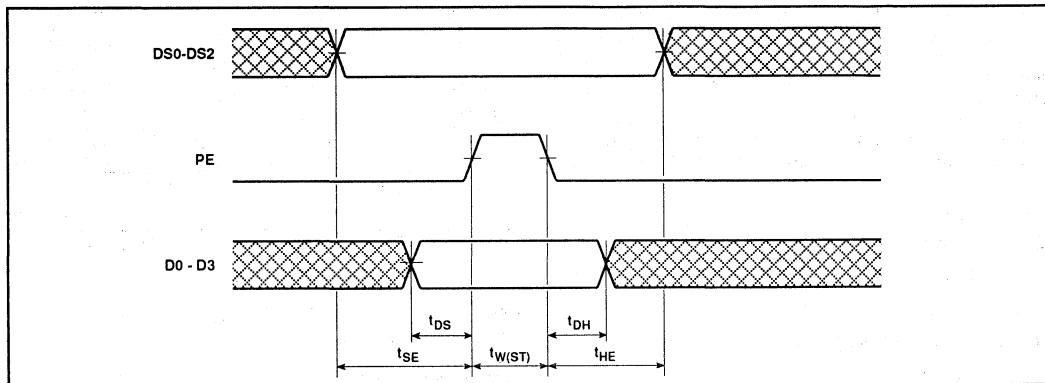


Fig. 6 Timing diagram

**PHASE COMPARATORS**

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error. The relationship between this offset and the

phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 150-270 is advised.

**PROGRAMMING/POWER UP**

Data and signal input pins should not have input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur.



# NJ88C22

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ88C22 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C22 is intended to be used in conjunction with a two-modulus prescaler such as the SP8715 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

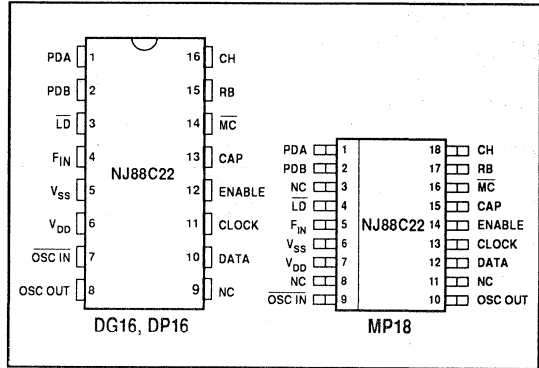


Fig.1 Pin connections - top view (not to scale)

### FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >20MHz Input Frequency
- Fast Lock-up Time

### ORDERING INFORMATION

- NJ88C22 MA DG Ceramic DIL Package
- NJ88C22 MA DP Plastic DIL Package
- NJ88C22 MA MP Miniature Plastic DIL Package

### ABSOLUTE MAXIMUM RATINGS

- Supply voltage,  $V_{DD} - V_{SS}$ : -0.75V to 7V
- Input voltage: 7V
- Open drain output,  $\overline{LD}$  pin:  $V_{SS} - 0.3V$  to  $V_{DD} + 0.3V$
- All other pins: -55°C to +125°C
- Storage temperature: -65°C to +150°C (DP and MP packages)
- 65°C to +150°C (DG package)

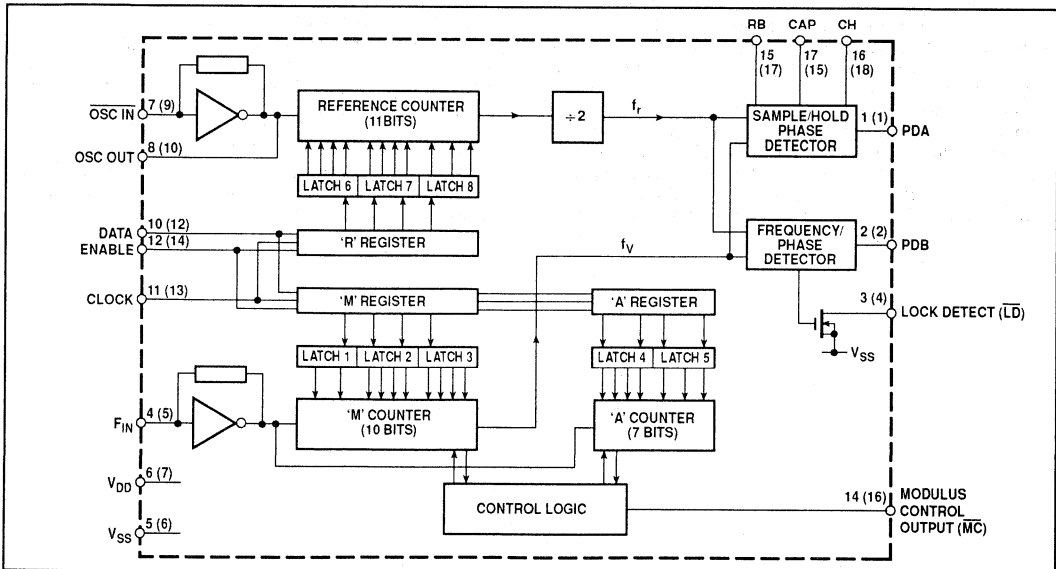


Fig.2 Block diagram (MP pinout shown in parentheses)

**ELECTRICAL CHARACTERISTICS AT  $V_{DD} = 5V$**

Test conditions unless otherwise stated:

$V_{DD}-V_{SS}=5V \pm 0.5V$ . Temperature range =  $-40^{\circ}C$  to  $+85^{\circ}C$

**DC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5.5 1.5	mA mA	$f_{OSC}, f_{FIN} = 10MHz$ $f_{OSC}, f_{FIN} = 1MHz$ } 0 to 5V square wave
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>					
High level	4.6			V	$I_{SOURCE} = 1mA$
Low level			0.4	V	
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					
Low level			0.4	V	$I_{SINK} = 4mA$
Open drain pull-up voltage			7.0	V	
<b>PDB Output</b>					
High level	4.6			V	$I_{SOURCE} = 5mA$
Low level			0.4	V	
3-state leakage current			$\pm 0.1$	$\mu A$	

**AC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$f_{IN}$ and $\overline{OSC}$ $\overline{IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave Input squarewave $V_{DD}$ to $V_{SS}$ , 25°C.
Max. operating frequency, $f_{FIN}$ and $f_{OSC}$	20			MHz	
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
<b>Programming Inputs</b>					All timing periods are referenced to the negative transition of the clock waveform
Clock high time, $t_{CH}$	0.5			$\mu s$	
Clock low time, $t_{CL}$	0.5			$\mu s$	
Enable set-up time, $t_{ES}$	0.2		$t_{CH}$	$\mu s$	
Enable hold time, $t_{EH}$	0.2			$\mu s$	
Data set-up time, $t_{DS}$	0.2			$\mu s$	
Data hold time, $t_{DH}$	0.2			$\mu s$	
Clock rise and fall times			0.2	$\mu s$	
High level threshold			$V_{DD}-0.8$	V	
Low level threshold	0.8			V	
Hysteresis	1.0			V	
<b>Phase Detector</b>					
Digital phase detector propagation delay		500		ns	See note 3
Gain programming resistor, RB	5			k	
Hold capacitor, CH			1	nF	
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	k	

**NOTES**

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ .
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.

PIN DESCRIPTIONS

Pin no.		Name	Description
DG,DP	MP		
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as $f_v$ (the output from the 'M' counter) phase lead increases; voltage decreases as $f_r$ (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD} - V_{SS})/2$ when the system is in lock.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or $f_v$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_v < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_v = f_r$ and phase error within PDA window: high impedance.
-	3	NC	Not connected.
3	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	$F_{IN}$	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	6	$V_{SS}$	Negative supply (ground).
6	7	$V_{DD}$	Positive supply (normally 5V)
-	8	NC	Not connected.
7, 8	9, 10	OSC IN/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 $\Omega$ resistor between OSC OUT and the crystal will improve stability. An external reference signal may, alternatively, be applied to OSC IN. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the total division ratio being twice the programmed number.
9	-	NC	Not connected.
10	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C22; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
11	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
13	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to $V_{SS}$ ).
14	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\pm 128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio $N$ should be: $N \geq P^2 - P$ , where $N = MP + A$ .
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
16	18	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

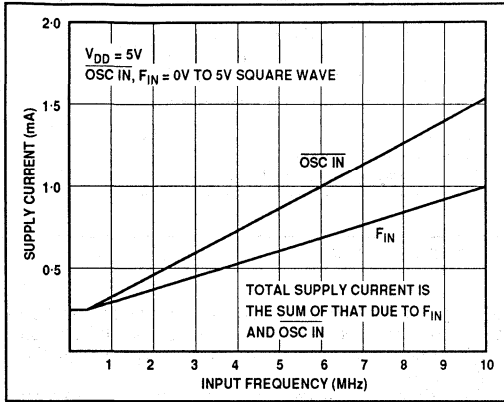


Fig. 3 Typical supply current v. input frequency

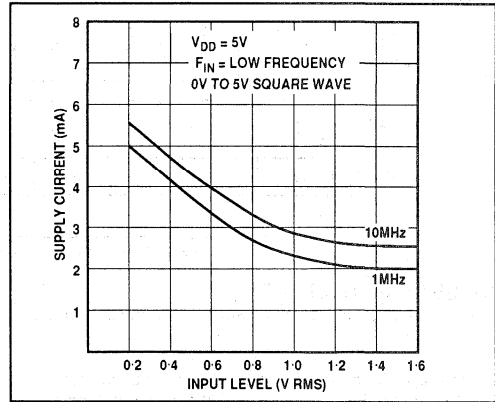


Fig. 4 Typical supply current v. input level, OSC IN

**PROGRAMMING  
Reference Divider Chain**

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,  
*fcomp* = comparison frequency,  
*R* = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be  $2 \times 400 = 800$  since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

**VCO Divider Chain**

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler ( $P/P+1$ ) and the comparison frequency.

The division ratio  $N = MP + A$ ,

where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127.

Note that  $M \geq A$  and

$$N = \frac{fvco}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now,  $N = MP + A$ , which can be rearranged as  $N/P = M + A/P$ . In our example we have  $P = 64$ , therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that  $M = 343$  and  $A/64 = 0.75$ .

Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part  $\times 64$  i.e.,  $A = 0.75 \times 64 = 48$ . **NB** The minimum ratio *N* that can be used is  $P^2 - P$  (= 4032 in our example) for all contiguous channels to be available.

To check:  $N = 343 \times 64 + 48 = 22000$ , which is the required division ratio and is greater than 4032 ( $= P^2 - P$ ).

When re-programming, a reset to zero is followed by reloading with the new counter values, which means that the loop lock-up time will be well defined and less than 10ms. If shorter lock-up times are required, when making only small changes in frequency, the non-resettable NJ88C28 should be considered.

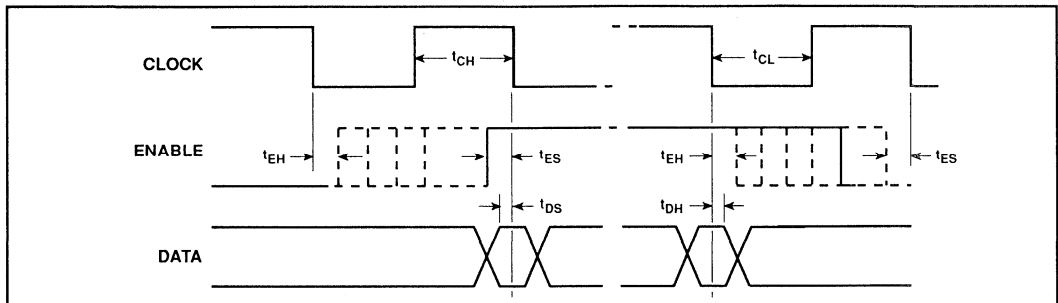


Fig. 5 Timing diagram showing timing periods required for correct operation

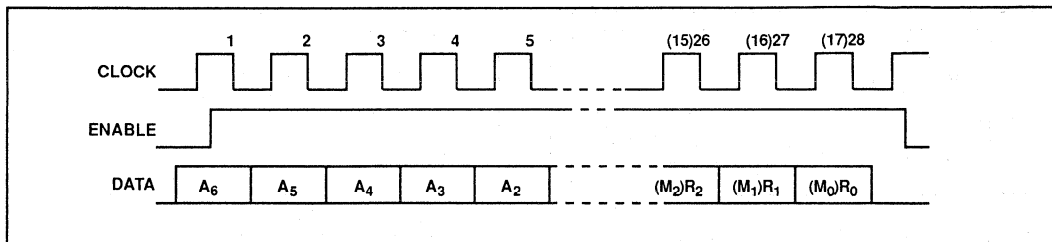


Fig.6 Timing diagram showing programming details

**PHASE COMPARATORS**

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD} K_{VCO}}{N}$$

where  $K_{PD}$  is the phase detector constant (volts/rad),  $K_{VCO}$  is the VCO constant (rad/sec/volt) and  $N$  is the overall loop division ratio. When  $N$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C22 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on  $\overline{LD}$ . The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains,

is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain,  $K_{PDA}$ , which is programmable with an external resistor,  $R_B$ , and a capacitor,  $CAP$ . An internal 50pF capacitor is used in the sample and hold comparator.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between the OSC OUT pin and the other components. A value of between 150 and 270  $\Omega$  is advised, depending on the crystal series resistance.

**PROGRAMMING/POWER UP**

Data and signal input pins should not have input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur.





# NJ8823

## FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8823 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor..

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8823 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of  $-30^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . The NJ8823MA is available only in Ceramic DIL package with operating temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### FEATURES

- Low Power Consumption
- Microprocessor Compatible
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency
- Fast Lock-up Time

### ORDERING INFORMATION

- NJ8823 BA DP** Plastic DIL Package
- NJ8823 BA MP** Miniature Plastic DIL Package
- NJ8823 MA DG** Ceramic DIL Package

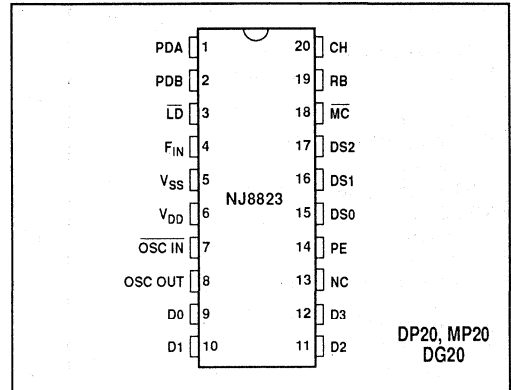


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

- Supply voltage,  $V_{DD}-V_{SS}$  -0.5V to 7V
- Input voltage 7V
- Open drain output, pin 3  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$
- All other pins -65°C to +150°C
- Storage temperature (DG package, NJ8823MA)
- Storage temperature -55°C to +125°C
- (DP and MP packages, NJ8823)

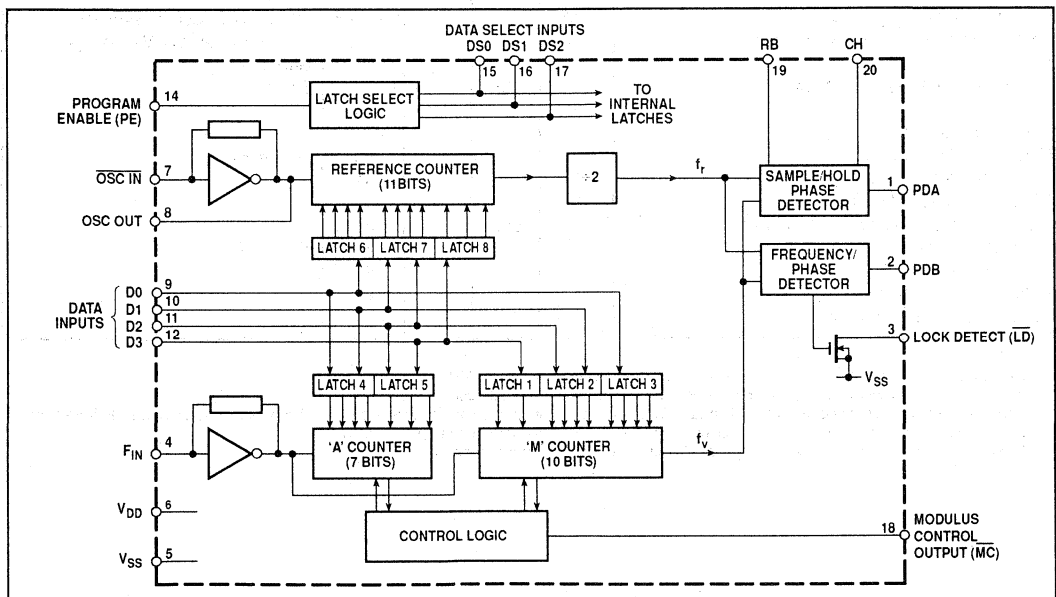


Fig.2 Block diagram

**ELECTRICAL CHARACTERISTICS AT  $V_{DD} = 5V$**

Test conditions unless otherwise stated:

$V_{DD} - V_{SS} = 5V \pm 0.5V$ . Temperature range NJ8823 BA:  $-30^{\circ}C$  to  $+70^{\circ}C$ ; NJ8823 MA:  $-40^{\circ}C$  to  $+85^{\circ}C$

**DC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	$f_{OSC}, f_{FIN} = 10MHz$ $f_{OSC}, f_{FIN} = 1.0MHz$ } 0 to 5V square wave
		0.7	1.5	mA	
<b>OUTPUT LEVELS</b>					
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>					
High level	4.6			V	$I_{SOURCE} = 1mA$ $I_{SINK} = 1mA$
Low level			0.4	V	
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					
Low level			0.4	V	$I_{SINK} = 4mA$
Open drain pull-up voltage			7	V	
<b>PDB Output</b>					
High level	4.6			V	$I_{SOURCE} = 5mA$ $I_{SINK} = 5mA$
Low level			0.4	V	
3-state leakage current			$\pm 0.1$	$\mu A$	
<b>INPUT LEVELS</b>					
<b>Data Inputs (D0-D3)</b>					
High level	4.25			V	TTL compatible See note 1
Low level			0.4	V	
<b>Program Enable Input (PE)</b>					
High level	4.25			V	
Low level			0.75	V	
<b>Data Select Inputs (DS0-DS2)</b>					
High level	4.25			V	
Low level			0.75	V	

**AC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$F_{IN}$ and $\overline{OSC}$ IN input level	200			mVRMS	10MHz AC-coupled sinewave Input squarewave $V_{DD}$ to $V_{SS}$ . See note 4.
Max. operating frequency, $f_{FIN}$ and $f_{OSC}$	10.6			MHz	
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
Strobe pulse width, $t_{W(ST)}$	2			$\mu s$	
Data set-up time, $t_{DS}$	1			$\mu s$	
Data hold time, $t_{DH}$	1			$\mu s$	
Latch address set-up time, $t_{SE}$	1			$\mu s$	
Latch address hold time, $t_{HE}$	1			$\mu s$	
Digital phase detector propagation delay		500		ns	See note 3.
Gain programming resistor, RB	5			k	
Hold capacitor, CH			1	nF	
Output resistance, PDA			5	k	
Digital phase detector gain		0.4		V/Rad	

**NOTES**

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ , typically.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as $f_v$ phase lead increases; voltage decreases as $f_r$ phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or $f_v$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_v < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	$F_{IN}$	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	$V_{SS}$	Negative supply (ground).
6	$V_{DD}$	Positive supply.
7, 8	$\overline{OSC IN}/$ $OSC OUT$	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC IN}$ . This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Data on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	NC	No connection
14	PE	This pin is used as a strobe for the data. A logic '1' on this pin transfers data from the D0-D3 pins to the internal latch addressed by the data select (DS0-DS2) pins. A logic '0' disables the data inputs.
15, 16, 17	DS0-DS2	Data select inputs for addressing the internal data latches
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\div 128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio should be $P^2 - P$ .
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
20	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

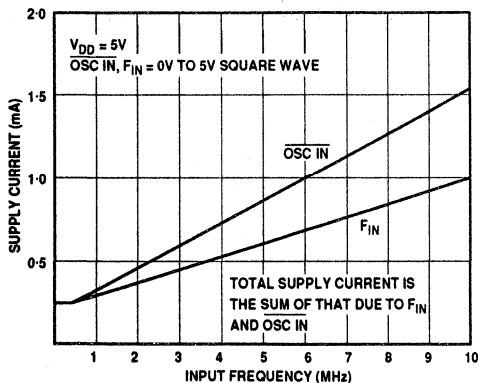


Fig. 3 Typical supply current v. input frequency

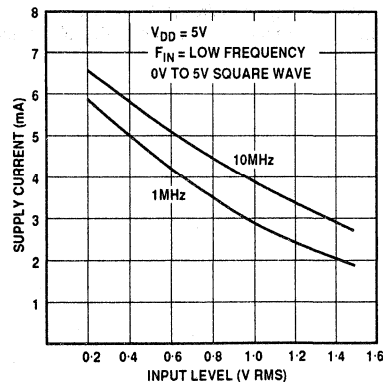


Fig. 4 Typical supply current v. input level,  $\overline{OSC IN}$

**PROGRAMMING**

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches as defined by the data map Fig.5. The PE pin is used as a strobe for the data: taking PE high causes data to be transferred from the data pins (D0-D3) into the addressed latch. Following the falling edge of PE, the data is retained in the addressed latch and the data inputs are disabled. Data transfer from all internal latches into the counters occurs simultaneously with the transfer of data into latch 1, which would therefore normally be the last latch addressed during each channel change. Timing information for this mode of operation is given in Fig. 6.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state, which means that the synthesiser loop lock-up time will be variable.

For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock-up times.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

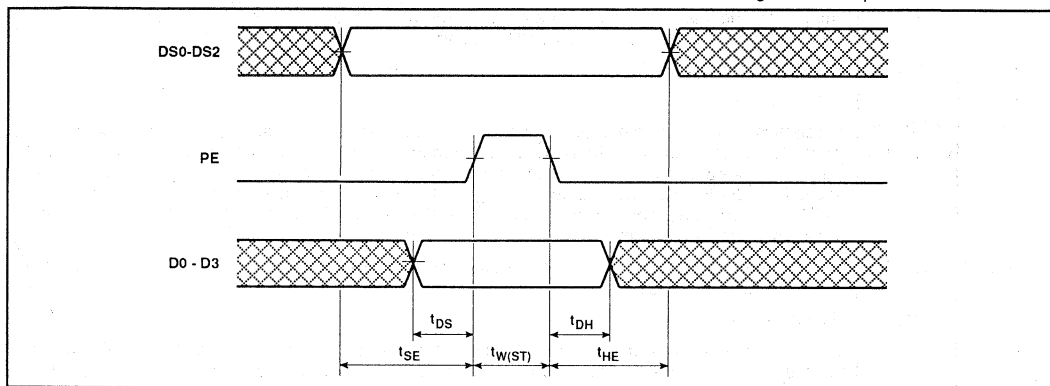


Fig. 6 Timing diagram

**PHASE COMPARATORS**

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error. The relationship between this offset and the

phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 150-270  $\Omega$  is advised.

**PROGRAMMING/POWER UP**

Data and signal input pins should not have input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur.



DS2438-2.3

# NJ88C24

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ88C24 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C24 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

### FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >20MHz Input Frequency
- Fast Lock-up Time

### ORDERING INFORMATION

- NJ88C24 MA DG Ceramic DIL Package
- NJ88C24 MA DP Plastic DIL Package
- NJ88C24 MA MP Miniature Plastic DIL Package

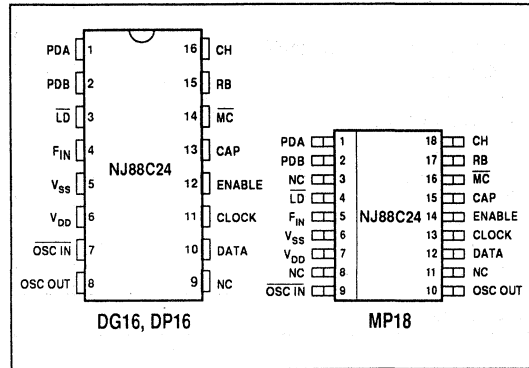


Fig. 1 Pin connections - top view (not to scale)

### ABSOLUTE MAXIMUM RATINGS

- Supply voltage,  $V_{DD}-V_{SS}$ : -0.5V to 7V
- Input voltage: 7V
- Open drain output,  $\overline{LD}$  pin:  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$
- All other pins: -55°C to +125°C
- Storage temperature: -65°C to +150°C (DP and MP packages)
- 65°C to +150°C (DG package)

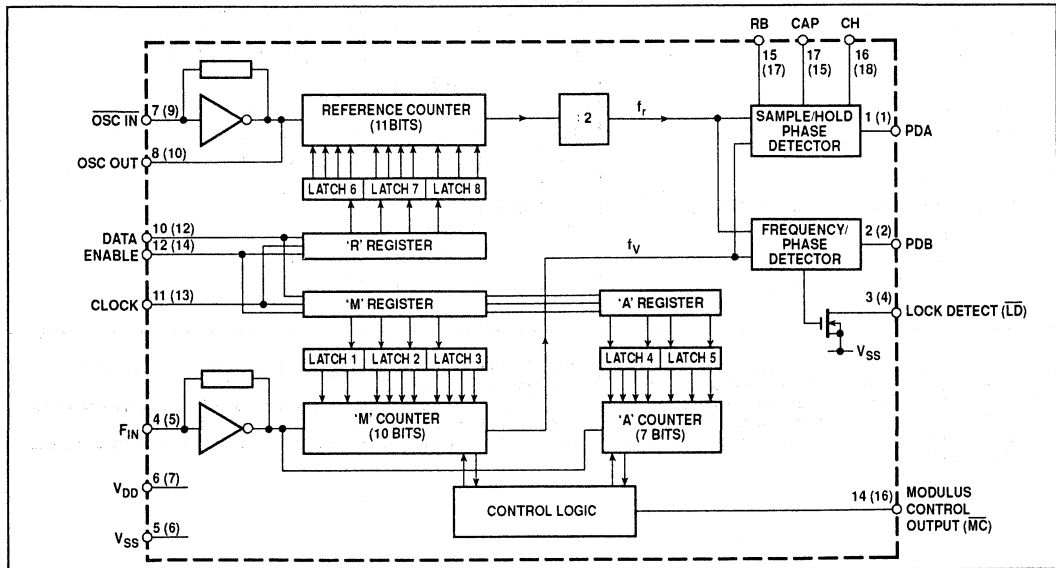


Fig. 2 Block diagram

# NJ88C24

## ELECTRICAL CHARACTERISTICS AT $V_{DD} = 5V$

Test conditions unless otherwise stated:

$V_{DD} - V_{SS} = 5V \pm 0.5V$ . Temperature range =  $-40^{\circ}C$  to  $+85^{\circ}C$

### DC Characteristics

Characteristic	Value			Units	Conditions	
	Min.	Typ.	Max.			
Supply current			5.5 1.5	mA mA	$f_{OSC}, f_{FIN} = 10MHz$ $f_{OSC}, f_{FIN} = 1MHz$	
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>	4.6					0 to 5V square wave
High level				V	$I_{SOURCE} = 1mA$ $I_{SINK} = 1mA$	
Low level			0.4	V		
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					$I_{SINK} = 4mA$	
Low level			0.4	V		
Open drain pull-up voltage			7.0	V		
<b>PDB Output</b>					$I_{SOURCE} = 5mA$ $I_{SINK} = 5mA$	
High level	4.6			V		
Low level				0.4		V
3-state leakage current				$\pm 0.1$		$\mu A$

### AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$F_{IN}$ and $\overline{OSC}$ $\overline{IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave Input square wave $V_{DD}$ to $V_{SS}$ , $25^{\circ}C$ .
Max. operating frequency, $f_{FIN}$ and $f_{OSC}$	20			MHz	
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
<b>Programming Inputs</b>					All timing periods are referenced to the negative transition of the clock waveform
Clock high time, $t_{CH}$	0.5			$\mu s$	
Clock low time, $t_{CL}$	0.5			$\mu s$	
Enable set-up time, $t_{ES}$	0.2		$t_{CH}$	$\mu s$	
Enable hold time, $t_{EH}$	0.2			$\mu s$	
Data set-up time, $t_{DS}$	0.2			$\mu s$	
Data hold time, $t_{DH}$	0.2			$\mu s$	
Clock rise and fall times			0.2	$\mu s$	
High level threshold			$V_{DD} - 0.8$	V	
Low level threshold	0.8			V	
Hysteresis	1.0			V	
<b>Phase Detector</b>					See note 1 See note 1 See note 1
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			k	
Hold capacitor, CH			1	nF	
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	k	See note 3

### NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ .
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.

PIN DESCRIPTIONS

Pin no.		Name	Description
DG,DP	MP		
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as $f_V$ (the output from the 'M' counter) phase lead increases; voltage decreases as $f_r$ (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD} - V_{SS})/2$ when the system is in lock.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or $f_V$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_V < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_V = f_r$ and phase error within PDA window: high impedance.
-	3	NC	Not connected.
3	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	$F_{IN}$	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	6	$V_{SS}$	Negative supply (ground).
6	7	$V_{DD}$	Positive supply (normally 5V)
-	8	NC	Not connected.
7, 8	9, 10	$\overline{OSC IN}$ / OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 $\Omega$ resistor between OSC OUT and the crystal will improve stability. An external reference signal may, alternatively, be applied to OSC IN. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the total division ratio being twice the programmed number.
9	-	NC	Not connected.
10	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C24; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
11	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
13	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to $V_{SS}$ ).
14	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $+128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio $N$ should be: $N \geq P^2 - P$ , where $N = MP+A$ .
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
16	18	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

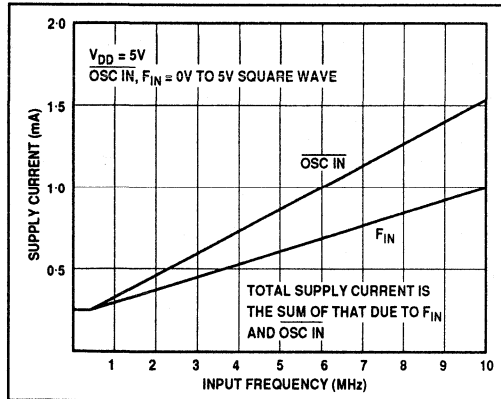


Fig. 3 Typical supply current v. input frequency

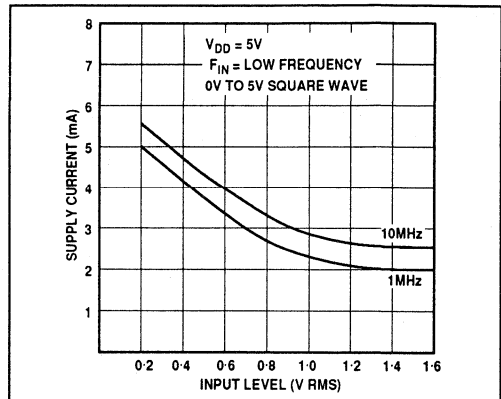


Fig. 4 Typical supply current v. input level, OSC IN

**PROGRAMMING Reference Divider Chain**

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{f_{osc}}{2 \times f_{comp}}$$

where  $f_{osc}$  = oscillator frequency,  
 $f_{comp}$  = comparison frequency,  
 $R$  = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be  $2 \times 400 = 800$  since the total division ratio of the 'R' counter plus the  $\div 2$  stage is from 6 to 4094 in steps of 2.

**VCO Divider Chain**

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler ( $P/P+1$ ) and the comparison frequency.

The division ratio  $N = MP + A$ , where  $M$  is the ratio of the 'M' counter in the range 8 to 1023 and  $A$  is the ratio of the 'A' counter in the range 0 to 127.

Note that  $M \geq A$  and

$$N = \frac{f_{VCO}}{f_{comp}}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two-modulus prescaler of  $\div 64/65$  is being used, then

$$N = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now,  $N = MP + A$ , which can be rearranged as  $N/P = M + A/P$ . In our example we have  $P = 64$ , therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that  $M = 343$  and  $A/64 = 0.75$ .

Now,  $M$  is programmed to the integer part = 343 and  $A$  is programmed to the fractional part  $\times 64$  i.e.,  $A = 0.75 \times 64 = 48$ .

**NB** The minimum ratio  $N$  that can be used is  $P^2 - P$  (=4032 in our example) for all contiguous channels to be available.

To check:  $N = 343 \times 64 + 48 = 22000$ , which is the required division ratio and is greater than 4032 ( $= P^2 - P$ ).

When re-programming, the counters are changed only at the zero state. There is no reset to zero, which means that the synthesiser loop lock-up time will be variable. When only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock-up times.

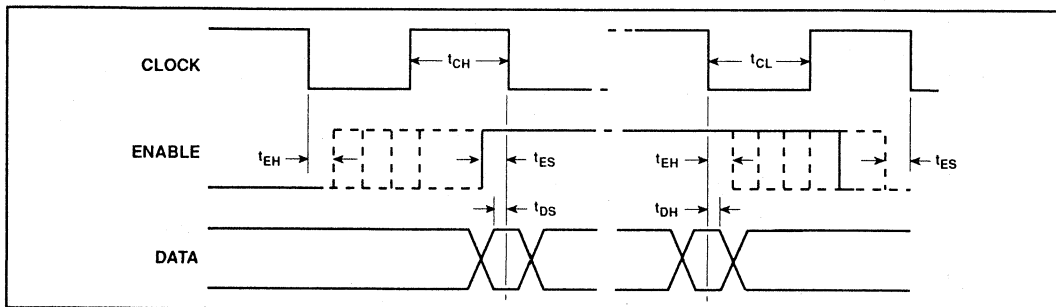


Fig. 5 Timing diagram showing timing periods required for correct operation



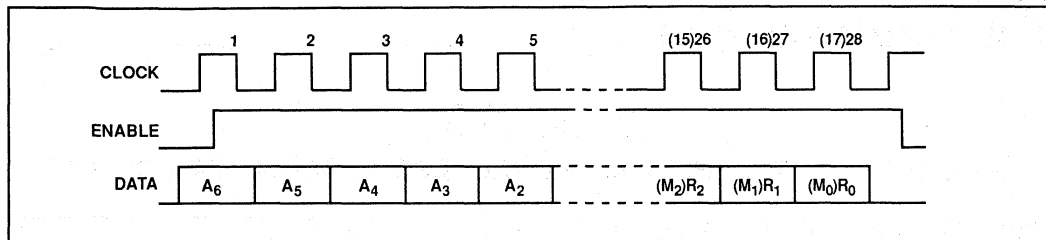


Fig.6 Timing diagram showing programming details

### PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD} K_{VCO}}{N}$$

where  $K_{PD}$  is the phase detector constant (volts/rad),  $K_{VCO}$  is the VCO constant (rad/sec/volt) and  $N$  is the overall loop division ratio. When  $N$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C24 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on  $\overline{LD}$ . The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains,

is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain,  $K_{PDA}$ , which is programmable with an external resistor,  $R_B$ , and a capacitor,  $CAP$ . An internal 50pF capacitor is used in the sample and hold comparator.

### CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between the OSC OUT pin and the other components. A value of between 150 and 270 is advised, depending on the crystal series resistance.

### PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur.

# NJ88C25

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 30 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 19 bits, when only the 'A', 'M' and 'B' counters require changing.

The NJ88C25 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

### FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature

### ORDERING INFORMATION

- NJ88C25 KA DG Ceramic DIL Package
- NJ88C25 KA DP Plastic DIL Package
- NJ88C25 KA MP Miniature Plastic DIL Package

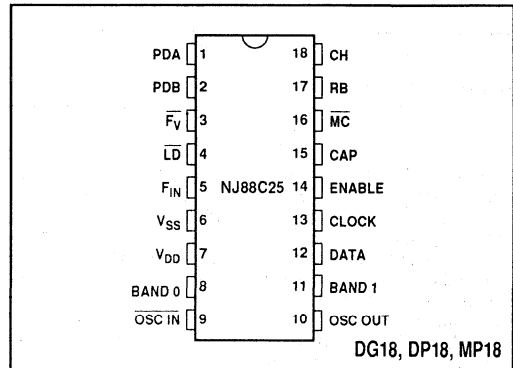


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

- Supply voltage,  $V_{DD} - V_{SS}$ : -0.5V to 7V
- Input voltage: 7V
- Open drain output, pins 3 and 4:  $V_{SS} - 0.3V$  to  $V_{DD} + 0.3V$
- All other pins: -65°C to +150°C (DG package)
- Storage temperature: -55°C to +125°C (DP and MP packages)

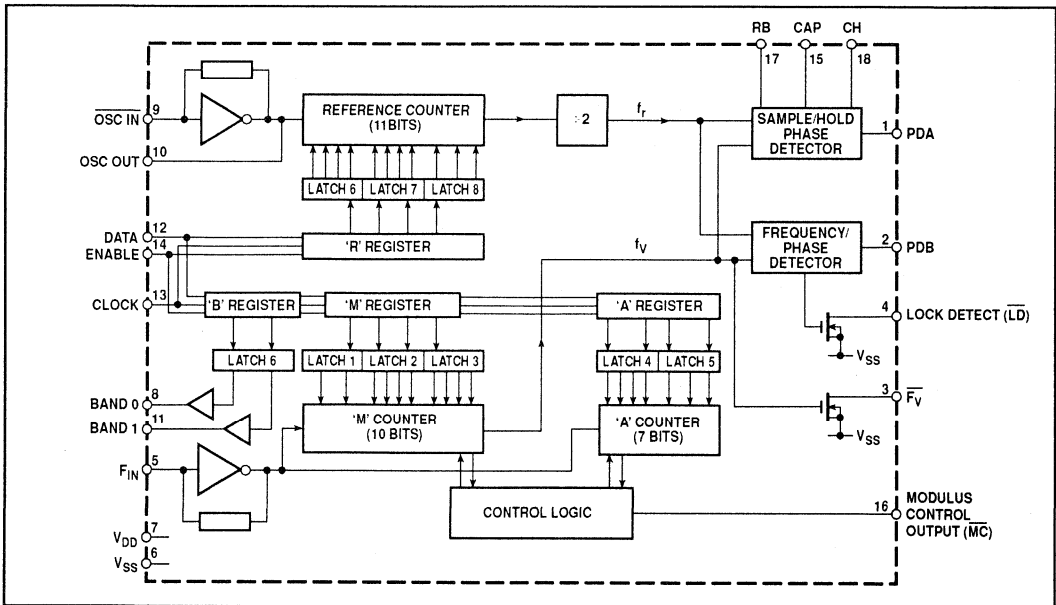


Fig.2 Block diagram

**ELECTRICAL CHARACTERISTICS AT V<sub>DD</sub> = 5V**

Test conditions unless otherwise stated:

V<sub>DD</sub>-V<sub>SS</sub>=2.7V to 5.5V. Temperature range = -30°C to +70°C

**DC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.5 0.7 3.7		mA mA mA	f <sub>OSC</sub> , f <sub>FIN</sub> = 20MHz } f <sub>OSC</sub> , f <sub>FIN</sub> = 1MHz } 0 to 5V f <sub>OSC</sub> , f <sub>FIN</sub> = 10MHz } square wave
<b>OUTPUTS</b> <b>Modulus Control (<math>\overline{MC}</math>), BAND 1 and BAND 2</b> High level Low level <b>Lock Detect: (<math>\overline{LD}</math>) and <math>\overline{FV}</math></b> Low level Open drain pull-up voltage <b>PDB</b> High level Low level 3-state leakage current	V <sub>DD</sub> -0.4		0.4 0.4 7.0 0.4 ±0.1	V V V V V V μA	I <sub>SOURCE</sub> = 1mA I <sub>SINK</sub> = 1mA I <sub>SINK</sub> = 4mA I <sub>SOURCE</sub> = 4mA I <sub>SINK</sub> = 4mA

**AC Characteristics**

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F <sub>IN</sub> and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f <sub>FIN</sub> and f <sub>OSC</sub>	20			MHz	Input squarewave V <sub>DD</sub> to V <sub>SS</sub> .
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
<b>Programming Inputs</b> Clock high time, t <sub>CH</sub> Clock low time, t <sub>CL</sub> Enable set-up time, t <sub>ES</sub> (see note 5) Enable hold time, t <sub>EH</sub> Data set-up time, t <sub>DS</sub> Data hold time, t <sub>DH</sub> Clock rise and fall times Positive threshold Negative threshold	0.5 0.5 0.2 0.2 0.2 0.2 0.2 3		t <sub>CH</sub> 2	μs μs μs μs μs μs μs V V	All timing periods are referenced to the negative transition of the clock waveform. See note 5 TTL compatible, see note 1
<b>Phase Detector</b> Digital phase detector propagation delay Gain programming resistor, RB Hold capacitor, CH Programming capacitor, CAP Output resistance, PDA		500 5		ns k nF nF k	See note 3

**NOTES**

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5μs.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the  $\overline{OSC\ IN}$  and F<sub>IN</sub> inputs.
5. Clock to enable set-up time (t<sub>ES</sub>) is variable, dependent on f<sub>OSC</sub>. It needs to be specified in terms of f<sub>OSC</sub>, clock high time (t<sub>CH</sub>) and clock low time (t<sub>CL</sub>) and must meet the following conditions:  $4 \times 1/f_{OSC} \leq t_{ES} \leq (t_{CH} + t_{CL})$ .

# NJ88C25

## PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as $f_V$ (the output from the 'M' counter) phase lead increases; voltage decreases as $f_r$ (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD} - V_{SS})/2$ when the system is in lock.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or $f_V$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_V < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_V = f_r$ and phase error within PDA window: high impedance.
3	$\overline{F_V}$	This pin is an open drain output from the 'M' counter.
4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	$F_{IN}$	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	$V_{SS}$	Negative supply (ground).
7	$V_{DD}$	Positive supply (normally 5V)
9,10	$\overline{OSC IN}$ / OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 $\Omega$ resistor between OSC OUT and the crystal will improve stability. An external reference signal may, alternatively, be applied to OSC IN. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the total division ratio being twice the programmed number.
8, 11	BAND 0/1	Two latch outputs, providing an output of the data from the 'B' register.
12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are four data words which control the NJ88C25; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 30 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'B', 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to $V_{SS}$ ).
16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. MC then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\pm 128/129$ . The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$ . Where every possible channel is required, the minimum total division ratio $N$ should be: $N \geq P^2 - P$ .
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ .
18	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

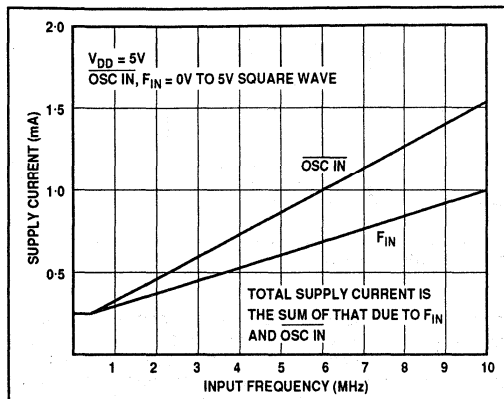


Fig. 3 Typical supply current v. input frequency

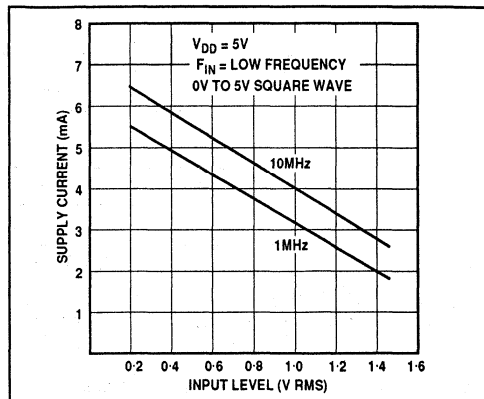


Fig. 4 Typical supply current v. input level, OSC IN

**PROGRAMMING Reference Divider Chain**

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,  
*fcomp* = comparison frequency,  
*R* = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be  $2 \times 400 = 800$  since the total division ratio of the 'R' counter plus the  $\div 2$  stage is from 6 to 4094 in steps of 2.

**VCO Divider Chain**

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler ( $P/P+1$ ) and the comparison frequency.

The division ratio  $N = MP + A$ , where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127. Note that  $M \geq A$  and

$$N = \frac{fvco}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two-modulus prescaler of  $\div 64/65$  is being used, then

$$N = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now,  $N = MP + A$ , which can be rearranged as  $N/P = M + A/P$ . In our example we have  $P = 64$ , therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that  $M = 343$  and  $A/64 = 0.75$ . Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part  $\times 64$  i.e.,  $A = 0.75 \times 64 = 48$ . **NB** The minimum ratio *N* that can be used is  $P^2 - P (= 4032$  in our example) for all contiguous channels to be available.

To check:  $N = 343 \times 64 + 48 = 22000$ , which is the required division ratio and is greater than 4032 ( $= P^2 - P$ ).

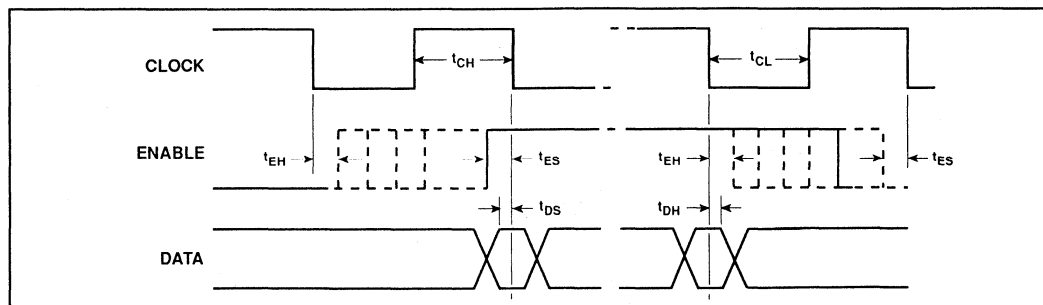


Fig. 5 Timing diagram showing timing periods required for correct operation

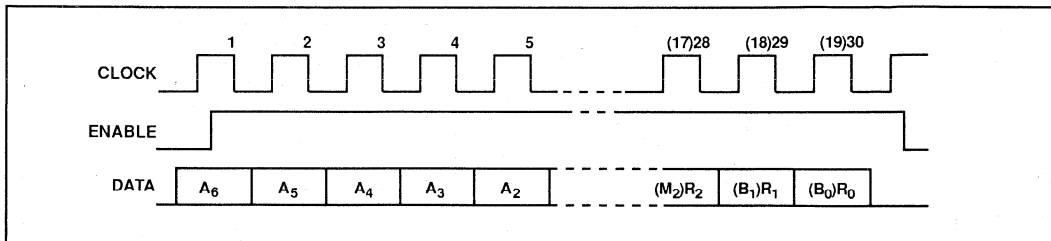


Fig.6 Timing diagram showing programming details

**PHASE COMPARATORS**

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD} K_{VCO}}{N}$$

where  $K_{PD}$  is the phase detector constant (volts/rad),  $K_{VCO}$  is the VCO constant (rad/sec/volt) and  $N$  is the overall loop division ratio. When  $N$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C25 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the

sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at  $(V_{DD} - V_{SS})/2$  and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain,  $K_{PDA}$ , which is programmable with an external resistor,  $R_B$ , and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator.

# NJ88C28

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

(Supersedes version in May 1992 Personal Communications IC Handbook)

The NJ88C28 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C28 is intended to be used in conjunction with a two-modulus prescaler such as the SP8715 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

### FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- 5V Operation
- Fast Lock Up Time
- SSOP Package Option

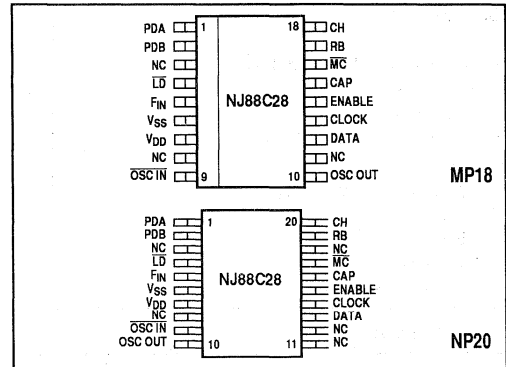


Fig. 1 Pin connections - top view (not to scale)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage,  $V_{DD}-V_{SS}$  -0.75V to 7V  
 Input voltage 7V  
 Open drain output, pin 4 7V  
 All other pins  $V_{SS}-0.3V$  to  $V_{DD}+0.3V$   
 Storage temperature -55°C to +125°C

### ORDERING INFORMATION

NJ88C28 IG MPES Miniature Plastic DIL Package  
 NJ88C28 IG NPAS Shrunken Miniature Plastic DIL Package

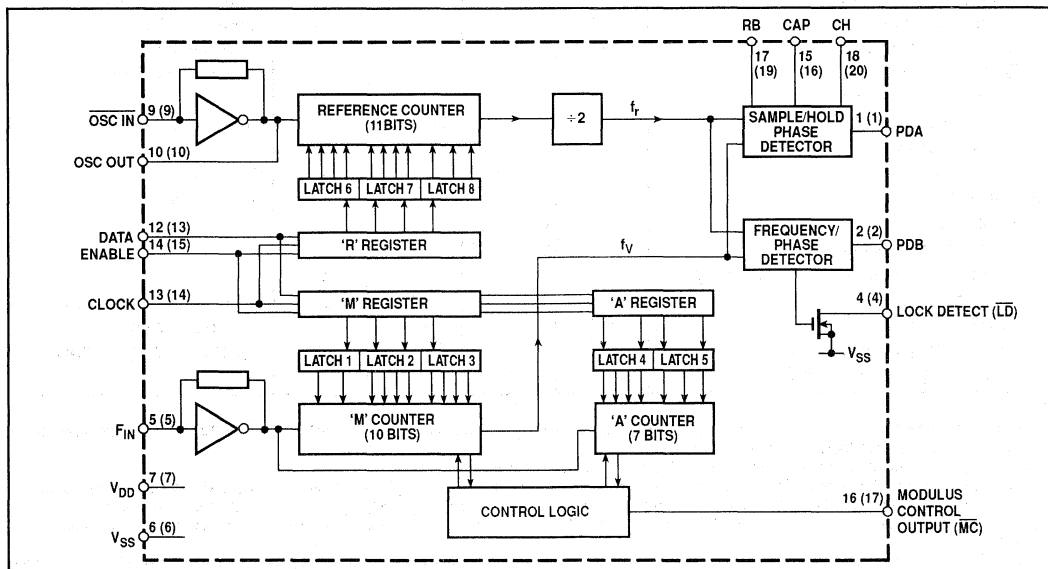


Fig. 2 block diagram (NP pinout shown in brackets)

# NJ88C28

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions, unless otherwise stated:

$$V_{DD}-V_{SS}=5V \pm 0.5V. \text{ Temperature range} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$$

### DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.3	7.0	mA	$f_{OSC}, f_{FIN} = 10\text{MHz}$ $f_{OSC}, f_{FIN} = 4.096\text{MHz}$
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>		0.9	1.4	mA	
High level	4.6			V	$I_{SOURCE} = 1\text{mA}$ $I_{SINK} = 1\text{mA}$
Low level			0.4		
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>					$I_{SINK} = 4\text{mA}$
Low level			0.4	V	
Open drain pull-up voltage			7.0	V	
<b>PDB Output</b>					$I_{SOURCE} = 5\text{mA}$ $I_{SINK} = 5\text{mA}$
High level	4.6			V	
Low level			0.4	V	
3-state leakage current			$\pm 100$	nA	

### AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$F_{IN}$ and $\overline{OSC}$ $\overline{IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, $F_{IN}$ and $\overline{OSC}$ $\overline{IN}$ inputs	20			MHz	
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
<b>Programming Inputs</b>					
Clock high time, $t_{CH}$	0.5			$\mu\text{s}$	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, $t_{CL}$	0.5			$\mu\text{s}$	
Enable set-up time, $t_{ES}$	0.2		$t_{CH}$	$\mu\text{s}$	
Enable hold time, $t_{EH}$	0.2			$\mu\text{s}$	
Data set-up time, $t_{DS}$	0.2			$\mu\text{s}$	
Data hold time, $t_{DH}$	0.2			$\mu\text{s}$	
Clock rise and fall times			0.2	$\mu\text{s}$	
High level threshold			$V_{DD}-0.8$	V	See note 1
Low level threshold	0.8			V	See note 1
Hysteresis	1.0	2.0		V	See note 1
<b>Phase Detector</b>					See note 3
Positive going threshold, $V_{T+}$		$V_{DD}-1.25$		V	Set by external conditions. Over RB current range. $C_{int}$ plus packaging strays.
Negative going threshold, $V_{T-}$		$V_{SS}+1.05$		V	
Digital phase detector propagation delay		500		ns	
RB current, $I_{RB}$	1		600	$\mu\text{A}$	
CAP/RB current gain, $\alpha$	6.9	7.8	9.0		
Programming capacitor, CAP		53		pF	
Output resistance, PDA, PDB		80		$\Omega$	

### NOTES

- Data, Clock and Enable inputs are high impedance Schmitt buffers with typical thresholds of  $V_{SS}+0.8V$  and  $V_{DD}-0.8V$ . These inputs do not have pull-up resistors and are therefore not TTL compatible.
- All counters have outputs directly synchronous with their respective clock rising edges.
- The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu\text{s}$ , typically; 1 $\mu\text{s}$  for the sample and hold amplifier.
- The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.
- The CAP reset device limits the minimum  $f_{IN}$  period due to its time constant formed by the CAP pin's capacitance value. A typical  $R_{DS(ON)}$  is about 1k $\Omega$ . Refer to AN112 for further details.



PIN DESCRIPTIONS

Pin no.		Name	Description
NP	MP		
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as $f_v$ (the output from the 'M' counter) phase lead increases; voltage decreases as $f_r$ (the output from the 'R' counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). This pin is at $(V_{DD} - V_{SS})/2$ when the system is in lock, for an external loop filter amplifier biased to $(V_{DD} - V_{SS})/2$ . Ideally, $V_{BIAS}$ should be chosen such that the PDA window is centred between the thresholds, typically at $0.55(V_{DD} - V_{SS})$
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or $f_v$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_v < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_v = f_r$ and phase error within PDA window: high impedance. (Minimum, $M = 3$ for correct function of PDB).
3	3	NC	Not connected..
4	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	5	$F_{IN}$	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	6	$V_{SS}$	Negative supply (ground).
7	7	$V_{DD}$	Positive supply.
8	8	NC	Not connected.
9,10	9,10	$\overline{OSC IN}/$ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 2-2k $\Omega$ resistor between pin 10 and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC IN}$ . This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the total division ratio being twice the programmed value i.e., 6 to 4094 in steps of 2.
11	11	NC	Not connected.
12	-	NC	Not connected.
13	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C28; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
14	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
15	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
16	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to $V_{SS}$ ).
17	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$ , where $P$ and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $\div 128/129$ . The programming range of the 'M' counter is 3-1023 but $M \geq 8$ for correct PDA operation and, for correct operation with a prescaler, $M \geq A$ . Where every possible channel is required, the minimum total division ratio $N$ should be: $N \geq P^2 - P$ , where $N = MP + A$ .
18	-	NC	Not connected

Continued...

# NJ88C28

## PIN DESCRIPTIONS (continued)

Pin no.		Name	Description
NP	MP		
19	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and $V_{SS}$ . $I_{RB} < 600\mu A$ at $V_{DD} = 5V$ .
20	18	CH	An external hold capacitor should be connected between this pin and $V_{SS}$ .

## PROGRAMMING Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{f_{osc}}{2 \times f_{comp}}$$

where  $f_{osc}$  = oscillator frequency,  
 $f_{comp}$  = comparison frequency,  
 $R$  = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be  $2 \times 400 = 800$  since the total division ratio of the 'R' counter plus the  $\div 2$  stage is from 6 to 4094 in steps of 2.

## VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler ( $P/P+1$ ) and the comparison frequency.

The division ratio  $N = MP + A$ ,

where  $M$  is the ratio of the M counter in the range 3 to 1023 and  $A$  is the ratio of the 'A' counter in the range 1 to 127.

Note that  $M \geq A$  and

$$N = \frac{f_{vco}}{f_{comp}}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two-modulus prescaler of  $\div 64/65$  is being used, then

$$N = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now,  $N = MP + A$ , which can be rearranged as  $N/P = M + A/P$ . In our example we have  $P = 64$ , therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that  $M = 343$  and  $A/64 = 0.75$ .

Now,  $M$  is programmed to the integer part = 343 and  $A$  is programmed to the fractional part  $\times 64$  i.e.,  $A = 0.75 \times 64 = 48$ . **NB** The minimum ratio  $N$  that can be used is  $P^2 - P$  (4032 in our example) for all contiguous channels to be available.

To check:  $N = 343 \times 64 + 48 = 22000$ , which is the required division ratio and is greater than 4032 ( $= P^2 - P$ ).

When re-programming, the counters are changed only at the zero state. There is no reset to zero, which means that the synthesiser loop lock up time will be variable with respect to the programming sequence timing. When only small changes in frequency are required, the NJ88C28 non-resettable synthesiser should achieve the shortest loop lock up times.

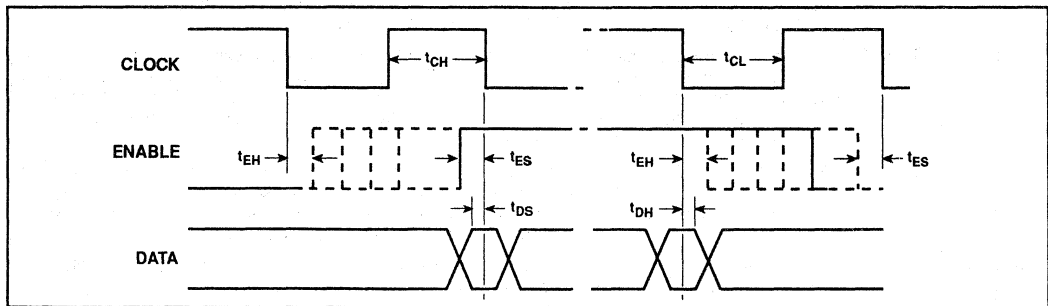


Fig. 3 Timing diagram showing timing periods required for correct operation

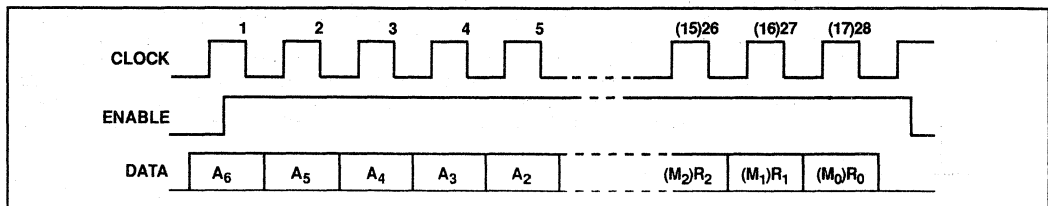


Fig. 4 Timing diagram showing programming details

**PHASE COMPARATORS**

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD} K_{VCO}}{N}$$

where  $K_{PD}$  is the phase detector constant (volts/rad),  $K_{VCO}$  is the VCO constant (rad/sec-volt) and  $N$  is the overall loop division ratio. When  $N$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C28 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at the bias voltage set by the external loop filter amplifier; any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain,  $K_{PDA}$ , which is programmable with an external resistor,  $R_B$ , and a capacitor,  $CAP$ . An internal 50pF capacitor is used in the sample and hold comparator. Typically, the gain is given by:

$$K_{PDA} = \frac{\alpha I_{RB}}{2\pi C_{CAP} f_{comp}}$$

where  $C_{CAP}$  = internal 50pF +  $C_{EXT}$ . Application Note AN112 deals with this further.

A hold capacitor (CH) of non-critical value, which might be typically 470pF, is connected from pin 18 to  $V_{SS}$ . A smaller value

is sufficient if the required sideband performance is not high. The output from the sample and hold phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO. The PDB gain is:

$$K_{PDB} = \frac{V_{DD}}{4\pi}$$

The stated minimum of 3 for the 'M' counter is true for the PDB output only. To avoid race conditions in the internal phase comparator counter for controlling the PDA timing, the minimum division ratio for the 'M' counter should be 8 or more. Fig. 6 shows a typical NJ88C28 application.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 10 (OSC OUT) and the other components, as shown in Fig. 5. A value of between 220Ω and 2.2kΩ is advised, depending on the crystal series resistance.

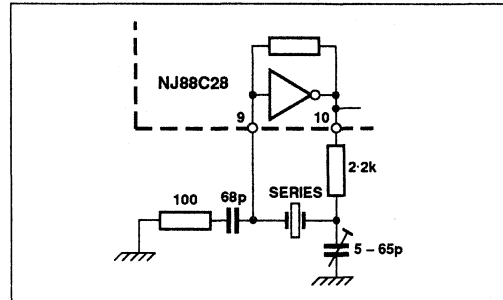


Fig. 5 Suggested crystal oscillator circuit

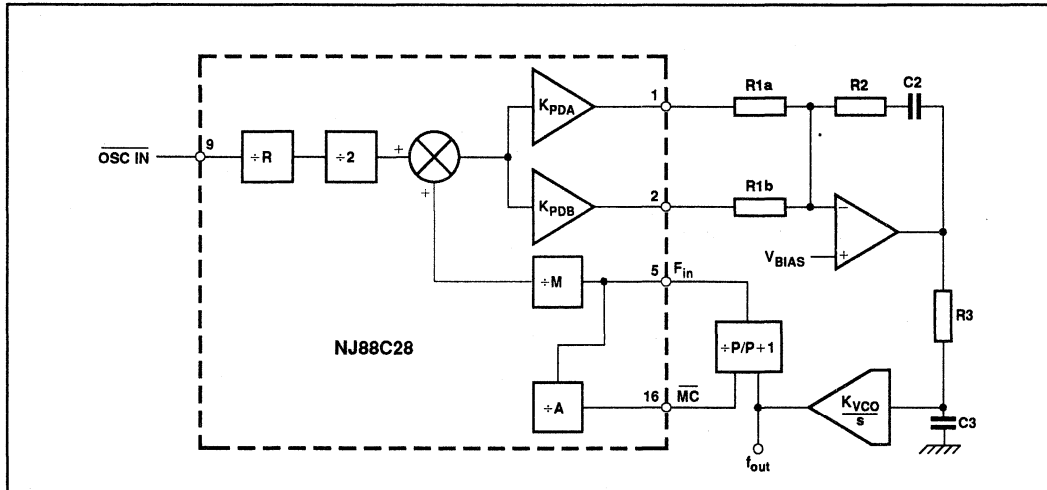


Fig. 6 NJ88C28 application circuit

## NJ88C28

### PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur. When programming the device, DATA, ENABLE and CLOCK pins must not exceed  $V_{DD}$  as lock up times may be compromised. A suggested interface to prevent this situation is shown in Fig. 7.

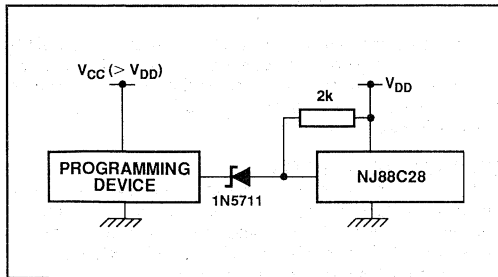


Fig. 7 Suggested programming circuit

### LOOP EQUATIONS

$$\omega_0 = \left[ \frac{K_{VCO} K_{PD}}{N R C_2 C_3 R_3} \right]^{\frac{1}{3}}$$

$$\zeta = \left[ (K_{VCO} K_{PD} R_2) / \{ (N C_3 R_3 \omega_0^2) - 1 \} \right] / 2R$$

$$C_3 R_3 = [\omega_0 (2\zeta + R)]^{-1}$$

$$R_2 = \frac{N \omega_0 (1 + 2\zeta R)}{K_{VCO} K_{PD} (R + 2\zeta)}$$

$$C_2 = \frac{K_{VCO} K_{PD} (2\zeta + R)}{N R \omega_0^2}$$

where  $\omega_0$  = loop natural frequency

$\zeta$  = damping factor

$R$  = ratio of real pole to  $\omega_0$

$N = MP + A$

$K_{PD} = K_{PDA} / R_{1a}$

or  $K_{PD} = K_{PDB} / R_{1b}$

provided  $R_{1a} \gg R_{1b}$

$$\text{PDA window} = \frac{V_{DD} - [(V_{T+}) + (V_{T-})] N f_{comp}}{2\pi K_{PDA}}$$

Further details are to be found in Application Note AN112.

# NJ88C29

## FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ88C29 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C29 is intended to be used in conjunction with a two-modulus prescaler such as the SP8715 series to produce a universal binary coded synthesiser for up to 1100MHz operation. Operation from a 3.8V supply is also supported.

### FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- 3.8V Operation
- Fast Lock Up Time
- SSOP Package

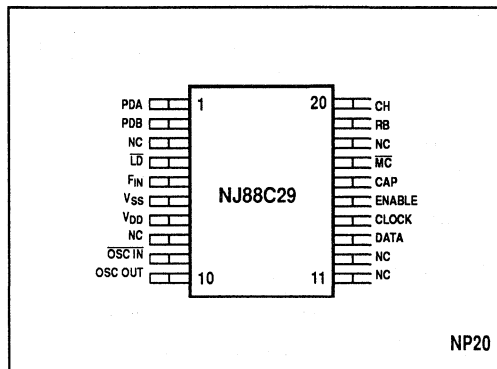


Fig.1 Pin connections - top view (not to scale)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	-0.75V to 7V
Input voltage	
Open drain output, pin 4	7V
All other pins	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage temperature	-55°C to +125°C

### ORDERING INFORMATION

NJ88C29 KG/NPAS Shrunken Miniature Plastic DIL Package

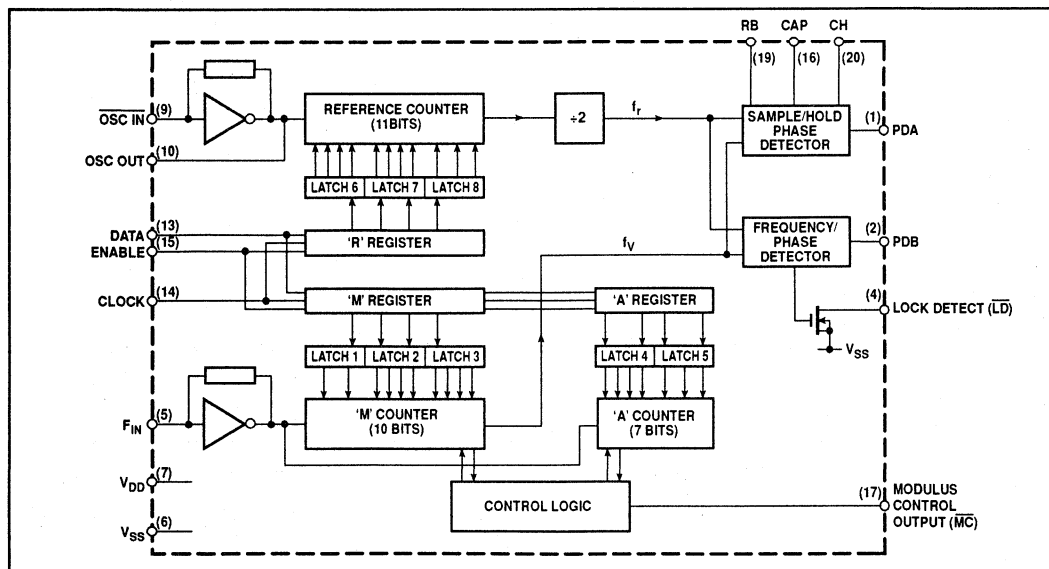


Fig.2 block diagram

# NJ88C29

## ELECTRICAL CHARACTERISTICS AT $V_{DD} = 3.8V$

These characteristics are guaranteed over the following conditions, unless otherwise stated:

$V_{DD} - V_{SS} = 3.8V \pm 0.4V$ . Temperature range =  $-15^{\circ}C$  to  $+70^{\circ}C$

### DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.0	5.0	mA	$f_{OSC}, f_{FIN} = 10MHz$ $f_{OSC}, f_{FIN} = 4.096MHz$ } 0 to 3.8V square wave
		0.6	0.94	mA	
<b>Modulus Control Output (<math>\overline{MC}</math>)</b>	2.5			V	$I_{SOURCE} = 1mA$ $I_{SINK} = 1mA$
High level				V	
Low level			0.4	V	
<b>Lock Detect Output (<math>\overline{LD}</math>)</b>				V	$I_{SINK} = 4mA$
Low level			0.4	V	
Open drain pull-up voltage			7.0	V	
<b>PDB Output</b>	2.5			V	$I_{SOURCE} = 3mA$ $I_{SINK} = 3mA$
High level				V	
Low level				0.4	
3-state leakage current			$\pm 100$	nA	

### AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$\overline{OSC}$ IN input level and $F_{IN}$ input level	200			mV RMS	12.8MHz AC-coupled sinewave
Max. operating frequency, $F_{IN}$ and $\overline{OSC}$ IN inputs	20			MHz	See note 4 Input squarewave $V_{DD}$ to $V_{SS}$ , 25°C. See note 5.
Propagation delay, $F_{IN}$ to modulus control $\overline{MC}$		30	50	ns	See note 2
<b>Programming Inputs</b>					All timing periods are referenced to the negative transition of the clock waveform See note 4
Clock high time, $t_{CH}$		0.5		$\mu s$	
Clock low time, $t_{CL}$		0.5		$\mu s$	
Enable set-up time, $t_{ES}$		0.2	$t_{CH}$	$\mu s$	
Enable hold time, $t_{EH}$		0.2		$\mu s$	
Data set-up time, $t_{DS}$		0.2		$\mu s$	
Data hold time, $t_{DH}$		0.2		$\mu s$	
Clock rise and fall times			0.2	$\mu s$	
High level threshold			$V_{DD} - 0.24$	V	See note 1
Low level threshold	0.4			V	See note 1
Hysteresis	1.23	1.8		V	See note 1
<b>Phase Detector</b>					See note 3
Positive going threshold, $V_{T+}$		1.12		V	
Negative going threshold, $V_{T-}$		$V_{DD} - 0.9$		V	
Digital phase detector propagation delay		500		ns	
RB current, $I_{RB}$	5		300	$\mu A$	Set by external conditions.
CAP/RB current gain, $\alpha$	6.3	7.0	7.8		Over RB current range.
Programming capacitor, CAP		100		pF	$C_{int}$ plus packaging strays.
Output resistance, PDA, PDB		80		$\Omega$	

### NOTES

- Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
- All counters have outputs directly synchronous with their respective clock rising edges.
- The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5 $\mu s$ , typically; 1 $\mu s$  for the sample and hold amplifier.
- The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.
- The minimum  $F_{in}$  period is governed by a time constant determined by the capacitance value on the CAP pin and the internal CAP discharge resistance. Depending on the value of CAP, PLL performance may be degraded at frequencies below 20MHz - see AN112 for further details.

## PIN DESCRIPTIONS

Pin no. NP	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as $f_v$ (the output from the 'M' counter) phase lead increases; voltage decreases as $f_r$ (the output from the 'R' counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). This pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock, for an external loop filter amplifier biased to $(V_{DD}-V_{SS})/2$ . Ideally, $V_{BIAS}$ should be chosen such that the PDA window is centred between the thresholds, typically at $0.55(V_{DD}-V_{SS})$ .
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v \geq f_r$ or $f_v$ leading: positive pulses with respect to the bias point $V_{BIAS}$ $f_v < f_r$ or $f_r$ leading: negative pulses with respect to the bias point $V_{BIAS}$ $f_v = f_r$ and phase error within PDA window: high impedance. (Minimum, $M = 3$ for correct function of PDB).
3	NC	Not connected.
4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	$F_{IN}$	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	$V_{SS}$	Negative supply (ground).
7	$V_{DD}$	Positive supply.
8	NC	Not connected.
9,10	$\overline{OSC IN}/$ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a $2.2k\Omega$ resistor between pin 10 and the crystal will improve stability. An external reference signal may, alternatively, be applied to OSC IN. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the total division ratio being twice the programmed value i.e., 6 to 4094 in steps of 2.
11	NC	Not connected.
12	NC	Not connected.
13	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C29; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
14	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
15	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
16	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to $V_{SS}$ ).
17	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $M \cdot P^2 - A$ , where $P$ and $P - 1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including $+ 128/129$ . The programming range of the 'M' counter is 3-1023 but $M \geq 8$ for correct PDA operation and, for correct operation with a prescaler, $M \geq A$ . Where every possible channel is required, the minimum total division ratio $N$ should be: $N \geq P^2 - P$ , where $N = M \cdot P^2 - A$ .
18	NC	Not connected

PIN DESCRIPTIONS (continued)

Pin no. NP	Name	Description
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V <sub>SS</sub> . I <sub>RB</sub> 300µA at V <sub>DD</sub> = 3.8V.
20	CH	An external hold capacitor should be connected between this pin and V <sub>SS</sub> .

**PROGRAMMING**  
**Reference Divider Chain**

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{f_{osc}}{2 \times f_{comp}}$$

where *f<sub>osc</sub>* = oscillator frequency,  
*f<sub>comp</sub>* = comparison frequency,  
*R* = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2X400 = 800 since the total division ratio of the 'R' counter plus the ÷ 2 stage is from 6 to 4094 in steps of 2.

**VCO Divider Chain**

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P/P-1*) and the comparison frequency.

The division ratio  $N = MP^2A$ , where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the 'A' counter in the range 1 to 127.

Note that  $M \geq A$  and

$$N = \frac{f_{vco}}{f_{comp}}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two-modulus prescaler of ÷ 64/65 is being used, then

$$N = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now,  $N = MP^2A$ , which can be rearranged as  $N/P = M^2A/P$ . In our example we have  $P = 64$ , therefore

$$\frac{22 \times 10^3}{64} = M^2 \frac{A}{64}$$

such that  $M = 343$  and  $A/64 = 0.75$ .

Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part x64 i.e.,  $A = 0.75 \times 64 = 48$ . **NB** The minimum ratio *N* that can be used is  $P^2 - P$  (4032 in our example) for all contiguous channels to be available.

To check:  $N = 343 \times 64^2 \times 48 = 22000$ , which is the required division ratio and is greater than 4032 ( $= P^2 - P$ ).

When re-programming, the counters are changed only at the zero state. There is no reset to zero, which means that the synthesiser loop lock up time will be variable with respect to the programming sequence timing. When only small changes in frequency are required, the NJ88C29 non-resettable synthesiser should achieve the shortest loop lock up times.

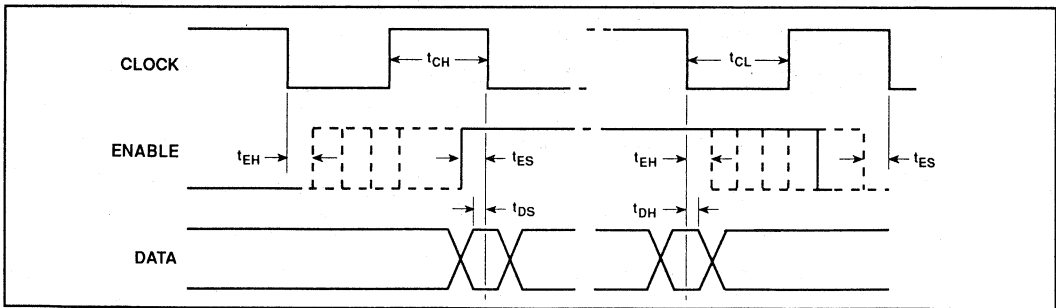


Fig. 3 Timing diagram showing timing periods required for correct operation

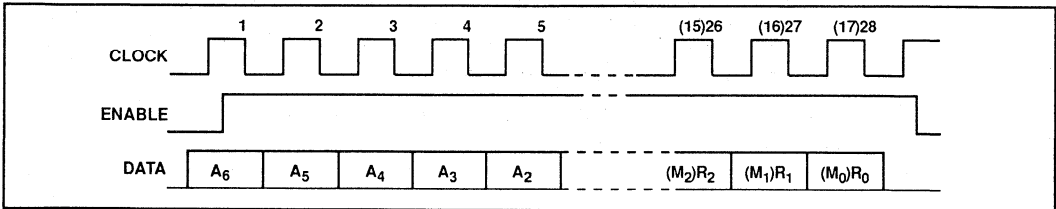


Fig. 4 Timing diagram showing programming details



**PHASE COMPARATORS**

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD} K_{VCO}}{N}$$

where  $K_{PD}$  is the phase detector constant (volts/rad),  $K_{VCO}$  is the VCO constant (rad/sec-volt) and  $N$  is the overall loop division ratio. When  $N$  is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C29 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at the bias voltage set by the external loop filter amplifier; any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain,  $K_{PDA}$ , which is programmable with an external resistor,  $R_B$ , and a capacitor,  $CAP$ . An internal 100pF capacitor is used in the sample and hold comparator. Typically, the gain is given by:

$$K_{PDA} = \frac{\alpha I_{RB}}{2\pi C_{CAP} f_{comp}}$$

where  $C_{CAP}$  = internal 100pF  $C_{EXT}$ . Application Note AN112 deals with this further.

A hold capacitor (CH) of non-critical value, which might be typically 470pF, is connected from pin 18 to  $V_{SS}$ . A smaller value

is sufficient if the required sideband performance is not high. The output from the sample and hold phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO. The PDB gain is:

$$K_{PDB} = \frac{V_{DD}}{4\pi}$$

The stated minimum of 3 for the 'M' counter is true for the PDB output only. To avoid race conditions in the internal phase comparator counter for controlling the PDA timing, the minimum division ratio for the 'M' counter should be 8 or more. Fig. 6 shows a typical NJ88C29 application.

**CRYSTAL OSCILLATOR**

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 10 (OSC OUT) and the other components, as shown in Fig. 5. A value of between 220Ω and 2.2kΩ is advised, depending on the crystal series resistance.

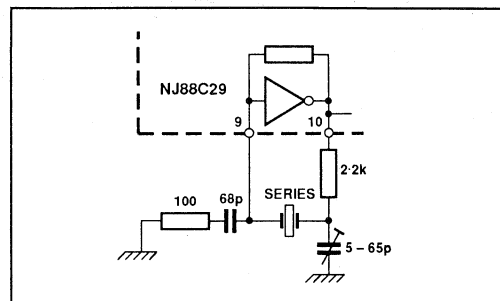


Fig. 5 Suggested crystal oscillator circuit

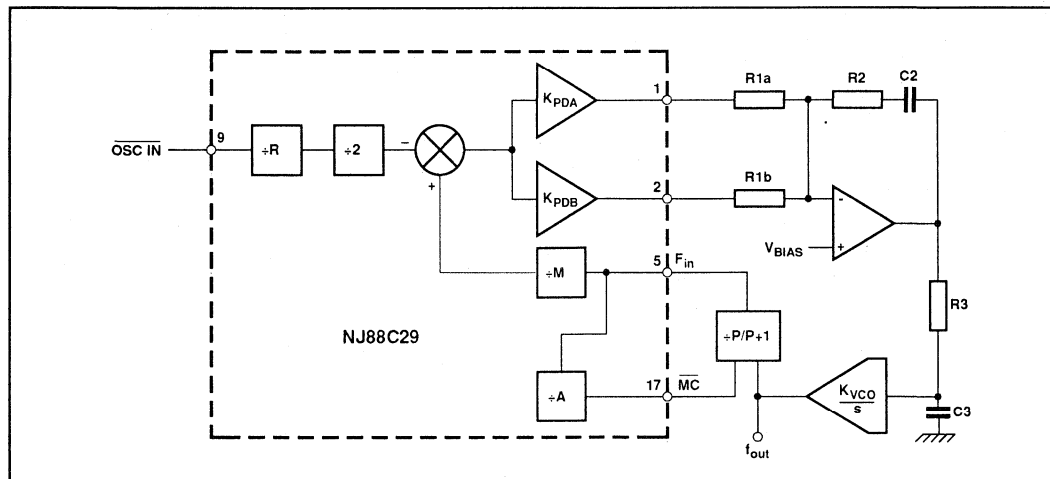


Fig.6 NJ88C29 application circuit

# NJ88C29

## PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of  $V_{DD}$ , as otherwise latch-up may occur. When programming the device, DATA, ENABLE and CLOCK pins must not exceed  $V_{DD}$  as lock up times may be compromised. A suggested interface to prevent this situation is shown in Fig. 7.

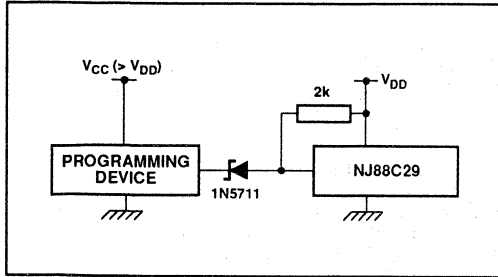


Fig. 7 Suggested programming circuit.

## LOOP EQUATIONS

$$\varphi_0 = \left[ \frac{K_{VCO} K_{PD}}{N R C_2 C_3 R_3} \right]^{\frac{1}{3}}$$

$$\zeta = \frac{\Sigma K_{VCO} K_{PD} R_2 || (\Sigma N C_3 R_3 \omega_0^2 || -1) \theta}{2 R}$$

$$C_3 R_3 = [ \omega_0 \Sigma 2 \zeta + R ]^{-1}$$

$$R_2 = \frac{N \omega_0 \Sigma 1 + 2 \zeta R}{K_{VCO} K_{PD} \Sigma R^{-2} \zeta ||}$$

$$C_2 = \frac{K_{VCO} K_{PD} \Sigma 2 \zeta R ||}{N R \omega_0^2}$$

where  $\omega_0$  = loop natural frequency

$\zeta$  = damping factor

$R$  = ratio of real pole to  $\omega_0$

$N = M P^{-1} A$

$K_{PD} = K_{PDA} / R_{1a}$

or  $K_{PD} = K_{PDB} / R_{1b}$

provided  $R_{1a} \gg R_{1b}$

$$PDA \text{ window} = \frac{V_{DD} \equiv \Sigma V_T \Gamma \Sigma V_T^{-1} \Gamma^{-1} \theta N f_{comp}}{2 \pi K_{PDA}}$$

Further details are to be found in Application Note AN112.

# NJ88C30

## VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the GPS high performance, small geometry CMOS process. The circuit contains a reference oscillator and divider, a two-modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

### FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

### APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

### ORDERING INFORMATION

**NJ88C30 KA DP** Plastic DIL Package  
**NJ88C30 KA MP** Miniature Plastic DIL Package

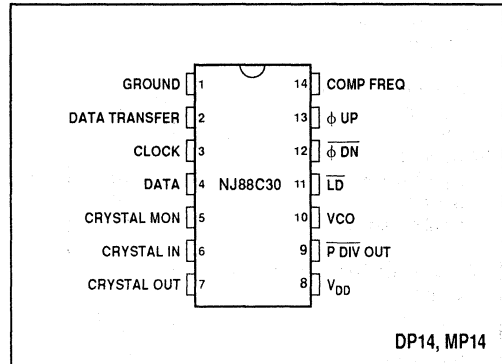


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}$	-0.3V to 6V
Voltage on any pin	-0.3V to $V_{DD}+0.3V$
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

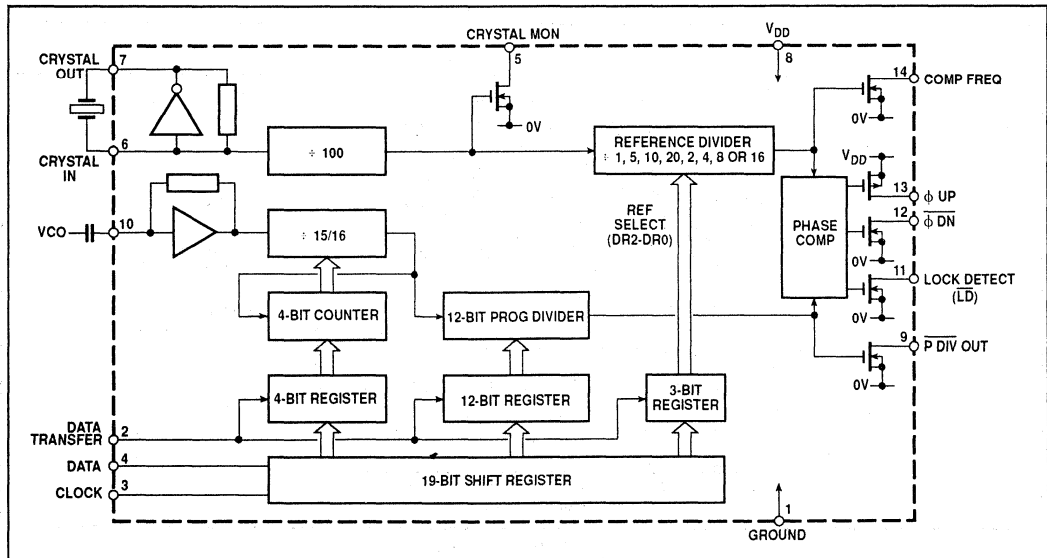


Fig.2 Block diagram

# NJ88C30

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$$T_{AMB} = -30^{\circ}\text{C to } +70^{\circ}\text{C}, V_{DD} = 5\text{V} \pm 0.5\text{V}$$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		4	7	mA	1VRMS VCO input at 200MHz and $f_{XTAL} = 10\text{MHz}$
<b>Crystal Oscillator</b>						
Frequency	6, 7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			Vrms	AC coupled
High level	6	$V_{DD}-1$			V	DC coupled
Low level	6			1	V	DC coupled
<b>VCO Input</b>						
Input sensitivity	10	1			Vrms	At 200MHz, see Fig. 3
Slew rate	10	4			V/ $\mu\text{s}$	
Input impedance	10		5pF// 10k			
<b>DATA, DATA TRANSFER and CLOCK Inputs</b>						
High level	2, 3, 4	$V_{DD}-1$			V	See Fig. 4
Low level	2, 3, 4			1	V	
Rise, fall time	2, 3			200	ns	
Data set-up time	3, 4	200			ns	
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
<b>CRYSTAL MONITOR Output</b>						
Current sink	5	0.8			mA	$V_{OUT} = 0.5\text{V}$
<b>COMP FREQ, LD, P DIV</b>						
Current sink	9, 11, 14	1.6			mA	$V_{OUT} = 0.5\text{V}$
$\phi$ UP / $\phi$ DN						
Current sink	12	0.8			mA	$V_{OUT} = 0.5\text{V}$
Current source	13	0.8			mA	$V_{OUT} = V_{DD}-0.5\text{V}$

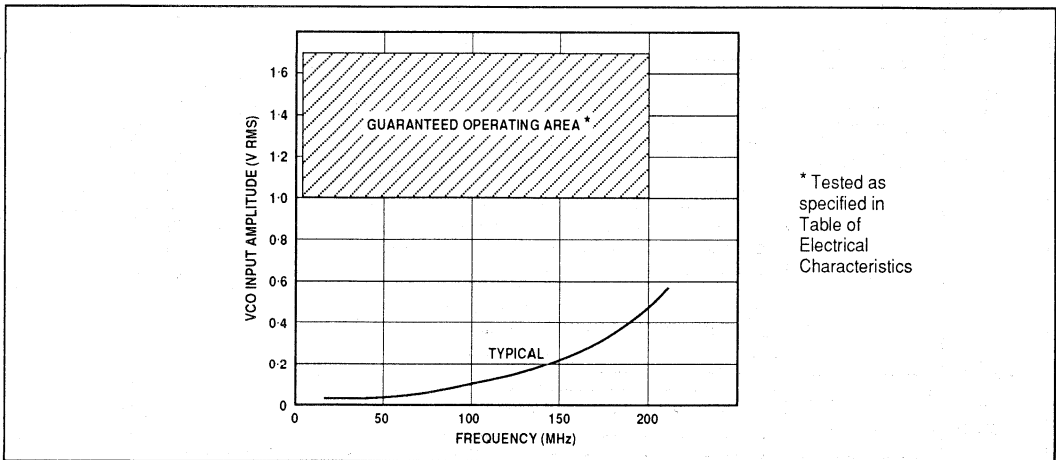


Fig. 3 Input sensitivity

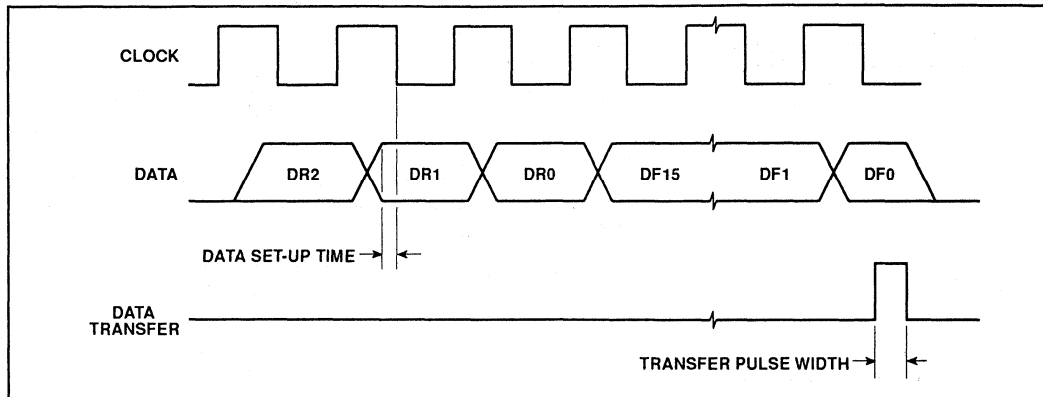


Fig. 4 Input data timing diagram

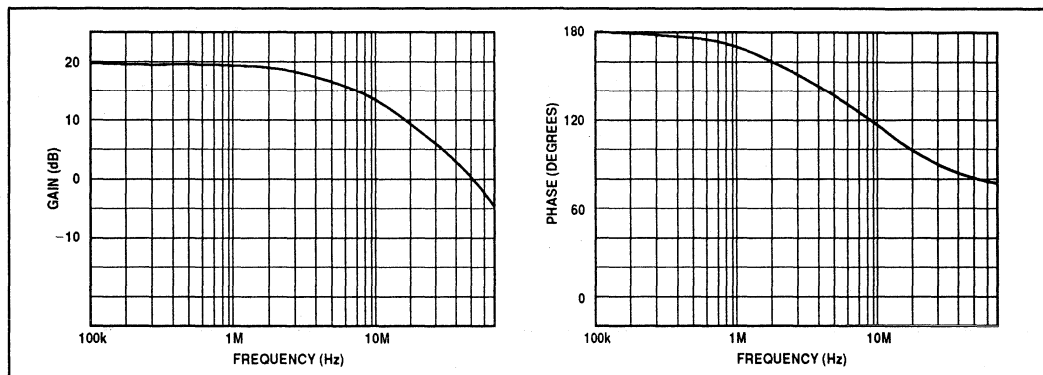


Fig. 5 Gain and phase characteristics of reference oscillator inverter

**CIRCUIT DESCRIPTION**

**Crystal Oscillator and Reference Divider**

The Reference oscillator consists of a Pierce type oscillator intended for use with a parallel resonant fundamental crystal. Typical gain and phase characteristics for the oscillator inverter are shown in Fig 5. An external reference oscillator may be used by either capacitively coupling a 1V RMS sinewave into CRYSTAL IN (pin 6) or, if CMOS levels are available, by direct connection to CRYSTAL IN.

The reference oscillator drives a ÷100 prescaler followed by a reference divider to provide a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies (channel spacing) if a 10MHz crystal is used are shown in Table 1.

DR2	DR1	DR0	Total division ratio	Comparison frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Table 1 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 5

**Programmable Divider**

The programmable divider consists of a ÷15/16 two modulus prescaler with a 4-bit control register, followed by a 12-bit programmable divider. A 1V RMS sinewave should be capacitively coupled from the VCO to the divider input VCO pin (pin 10).

The overall division ratio is selected by a single 16-bit word (DF15 to DF0), loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

**Phase Comparator**

The phase comparator consists of a digital type phase comparator with open drain  $\phi$  UP and  $\phi$  DN outputs and an open drain LOCK DETECT (LD) output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.6. The duty cycle of  $\phi$  UP and  $\phi$  DN versus phase difference are shown in Fig. 7. The phase comparator is linear over a  $\pm 2$  range and if the phase gains or slips by more than 2, the phase comparator outputs repeat with a 2 period.

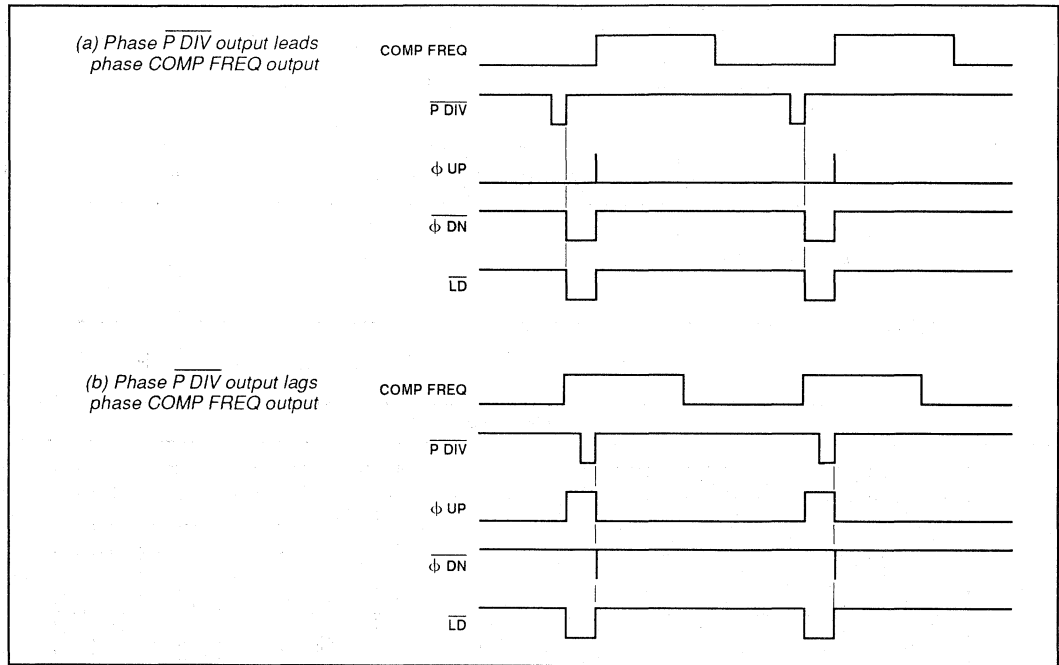


Fig. 6 Phase comparator waveforms

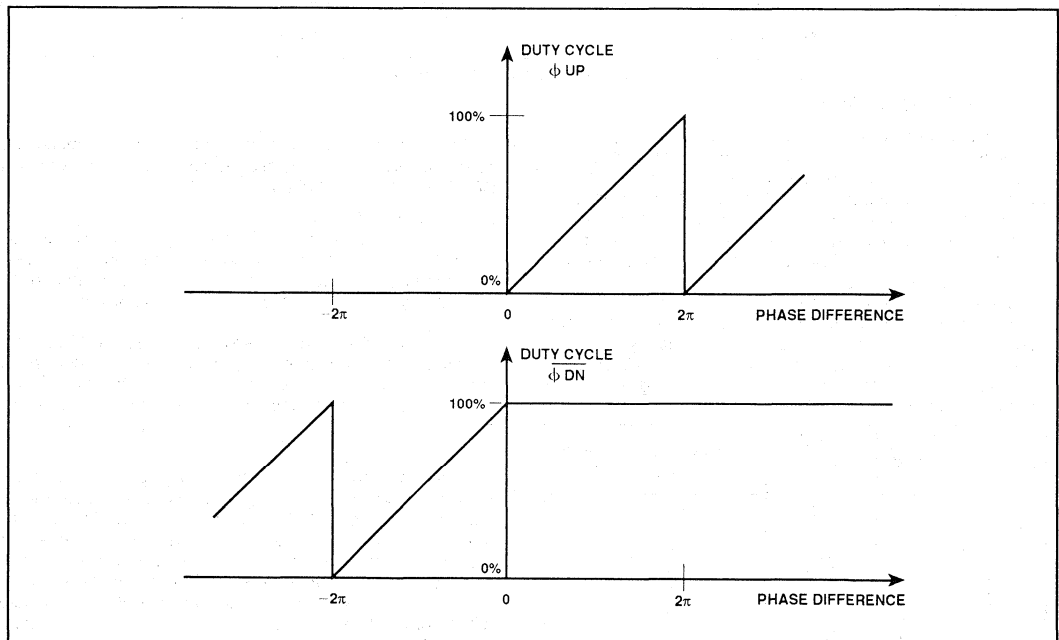


Fig. 7 Phase comparator output characteristics

Once the phase difference exceeds 2, the comparator will gain or slip one cycle and then try to lock on to the new zero phase difference. Note that very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output, as shown in Fig. 6.

**Data Input and Control Register**

To control the synthesiser a simple three-line serial input is used with DATA, CLOCK and DATA TRANSFER signals. The data consists of 19 bits; the first three, DR2, DR1 and DR0, control the reference divider while the following sixteen, DF15

to DF0, control the prescaler and programmable divider. Until the synthesiser receives the DATA TRANSFER pulse, it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

**APPLICATIONS**

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig. 8. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig. 8 is required.

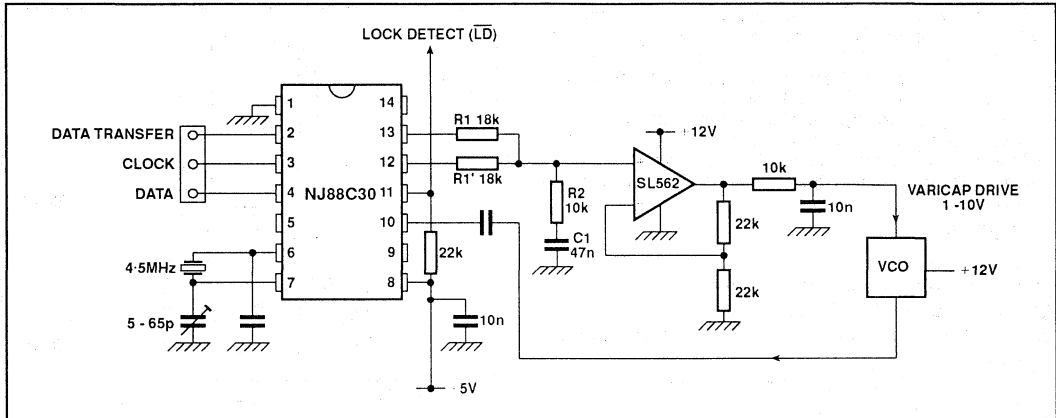


Fig.8. Typical application

**PROGRAMMING EXAMPLE**

**1. Maximum Frequency**

For a channel spacing (comparison frequency,  $f_{comp}$ ) of 5kHz when using a 10MHz crystal oscillator, the reference divider ratio will need to be 2000 (see Table 1) This is programmed as binary 100 (= 4<sub>HEX</sub>) in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is } 9C40_{HEX}$$

The program word would then be as shown in Table 2.

	DR			DF																
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0
Hex	4			9						C				4			0			

Table 2 Maximum VCO frequency programming ( $f_{XTAL} = 10\text{MHz}$ ,  $f_{comp} = 5\text{kHz}$ )

**2. Minimum Frequency**

Using the same crystal frequency and channel spacing (10MHz, 5kHz), the lower limit of programmable divider ratio of

$240 = F0_{HEX}$  gives a minimum programmable VCO frequency of  $240 \times 5 \times 10^3 = 1.2\text{MHz}$ . The program word for this frequency is therefore as shown in Table 3.

	DR			DF																
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
Hex	4			0						0				F			0			

Table 3 Minimum VCO frequency programming ( $f_{XTAL} = 10\text{MHz}$ ,  $f_{comp} = 5\text{kHz}$ )

# NJ88C33

## FREQUENCY SYNTHESISER (I<sup>2</sup>C BUS PROGRAMMABLE) WITH CURRENT SOURCE PHASE DETECTOR OUTPUTS

(Supersedes September 1991 edition)

The NJ88C33 is a synthesiser circuit fabricated on GPS's 1.4 micron CMOS process, assuring very high performance. It is I<sup>2</sup>C compatible and can also be programmed at up to 5MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to improve control voltage range to the VCO when operating at low supply voltages.

### FEATURES

- Easy to Use
- Low Power Consumption (15 mW)
- Single Supply 2.5V to 5.5V
- Digital Phase Comparator with Current Source Outputs
- Serial (I<sup>2</sup>C Compatible) Programming, 5MHz max;
- Channel Loading in 8 $\mu$ s
- 150MHz Input Frequency Without Prescaler at 4.5V (52MHz at 2.7V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

### APPLICATIONS

- Cordless Telephones (CT2, DECT)
- Cellular Telephones (GSM, PCN, ETACS)
- Hand Held Marine Radios
- Sonarbuoys
- Video Clock generators

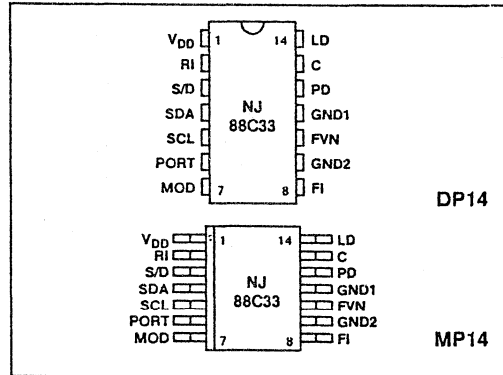


Fig.1 Pin connections (not to scale) - top views

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, V <sub>DD</sub>	-0.3V to 7V
Input voltage, V <sub>IM1</sub>	-0.3V to V <sub>DD</sub> + 0.3V
Output voltage on pin 13, V <sub>IM2</sub>	-V <sub>DD</sub> to 0V
Storage temperature, T <sub>stg</sub>	-55°C to +125°C

### ORDERING INFORMATION

- NJ88C33 MA DP (Industrial - Plastic DIL package)
- NJ88C33 MA MP (Industrial - Miniature Plastic DIL package)

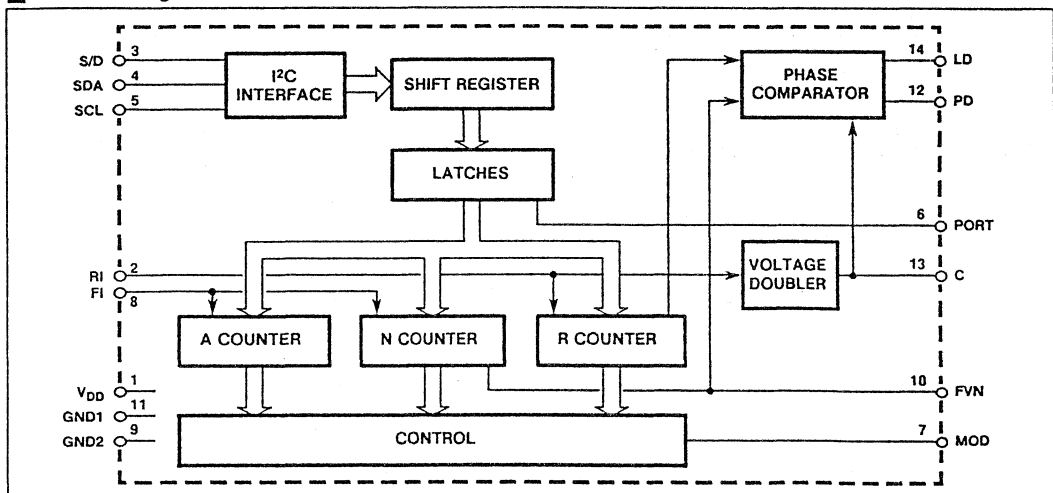


Fig.2 Simplified block diagram of NJ88C33



**PIN DESIGNATIONS**

Pin No.	Pin Name	Description
1	V <sub>DD</sub>	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I <sup>2</sup> C bus data input pin. It is also an open-drain output for generating I <sup>2</sup> C bus acknowledge pulses.
5	SCL	I <sup>2</sup> C bus clock input. It can be clocked at up to 5MHz.
6	PORT	Output control pin, which can be programmed via the I <sup>2</sup> C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A=0; MOD then remains high until N=0, when both counters are reloaded. It can be programmed via the I <sup>2</sup> C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I <sup>2</sup> C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I <sup>2</sup> C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservoir capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

**OPERATING RANGE**

Test conditions (unless otherwise stated):  
 PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V <sub>DD</sub>	2.5	5	5.5	V	FI = 50MHz, V <sub>FI</sub> = 150mVrms, N,R > 1000 without voltage doubler, V <sub>DD</sub> = 5V, T <sub>amb</sub> = 25°C
Ambient temperature	T <sub>amb</sub>	-40		+85	°C	
<b>Supply current</b>						
Single modulus	I <sub>DD</sub>		2.1	3.0	mA	
Dual modulus	I <sub>DD</sub>		2	3.0	mA	
Standby mode	I <sub>DD</sub>			1	µA	FI = 50MHz, V <sub>FI</sub> = 150mVrms, preamp off, divider off, V <sub>DD</sub> = 5V, T <sub>amb</sub> = 25°C
Standby mode	I <sub>DD</sub>		1.0	1.5	mA	FI = 50MHz, V <sub>FI</sub> = 150mVrms, preamp on, divider off, V <sub>DD</sub> = 5V, T <sub>amb</sub> = 25°C

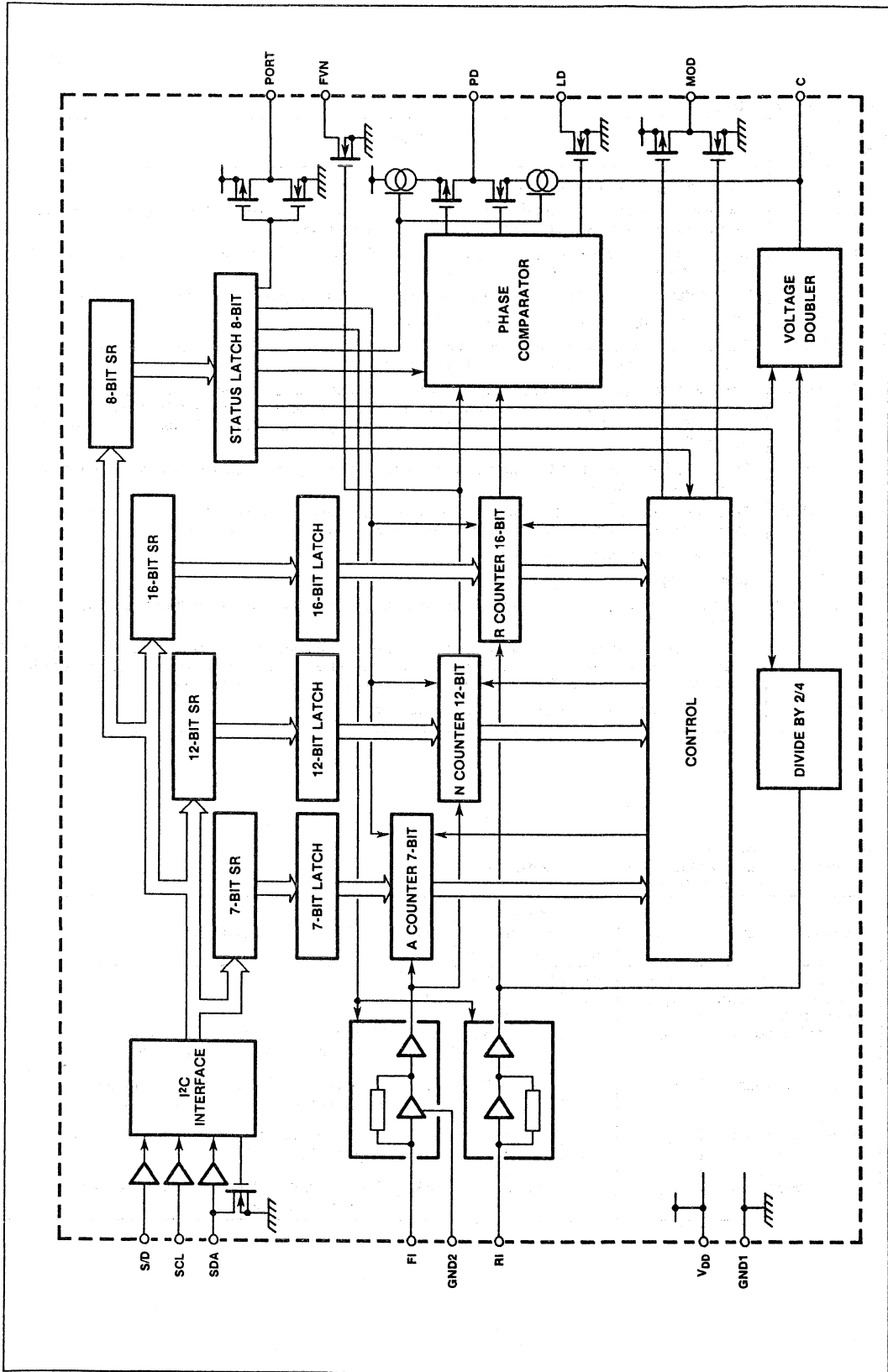


Fig.3 Functional block diagram

**ELECTRICAL CHARACTERISTICS**

Operating conditions (unless otherwise stated):

$V_{DD} = 4.5V$  to  $5.5V$ ,  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

**INPUT SIGNALS**

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
<b>Input Signals SDA, SCL, S/D</b>						
Input voltage high	$V_{IH}$	$0.7V_{DD}$		$V_{DD}$	V	$V_{IN} = V_{DD} = 5.5V$
Input voltage low	$V_{IL}$	0		$0.3V_{DD}$	V	
Input capacitance	$C_I$			10	pF	
Input current	$I_{IN}$			10	$\mu A$	
<b>Input Signal RI</b>						
Input frequency	$f_{max}$	100		52	MHz	Sinewave input Note 1, 2
Input voltage	$V_{IRMS}$			10	mV	
Input capacitance	$C_I$			10	pF	$V_{IN} = V_{DD} = 5.5V$
Input current	$I_{IN}$			10	$\mu A$	
<b>Input Signal FI</b>						
Input frequency	$f_{max}$	50		52	MHz	Dual modulus operation Sinewave input Note 1, 2
Input voltage	$V_{IRMS}$			10	mV	
Input capacitance	$C_I$			10	pF	$V_{IN} = V_{DD} = 5.5V$
Input current	$I_{IN}$			10	$\mu A$	
<b>Input Signal FI</b>						
Input frequency	$f_{max}$	30		150	MHz	Single modulus operation Sinewave input FI = 0-70MHz Note 1, 2
Input voltage	$V_{IRMS}$	100		200	mV	
	$V_{IRMS}$	200			mV	FI = 70-120MHz Note 1, 2
	$V_{IRMS}$				mV	FI = 120-150MHz Note 1, 2
Input capacitance	$C_I$			10	pF	$V_{IN} = V_{DD} = 5.5V$
Input current	$I_{IN}$			10	$\mu A$	

Note. 1 Lowest noise floor achieved at 10dB above this level with I<sup>2</sup>C bus operating. The source impedance should be less than 2k $\Omega$ .

Note. 2 DC coupled input amplitude  $V_{IRMS} > 0.8 V_{DD}$ .

**OUTPUT SIGNALS**

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
<b>Output Signals SDA, LD</b>						
Output voltage low	$V_{OL}$			0.4	V	Open drain, $I_{OL} = 3mA$
<b>Output Signal PD</b>						
High current mode (see Fig.4)	$I_{HU}$	1.9	2.5	3.1	mA	$C_L = 400pF$ , tristate output $0 < V_{PD} < 4.5$ , $V_{DD} = 5V$ , $T = 25^{\circ}C$ Note 1 $0.4 < V_{PD} < 5$ , $V_{DD} = 5V$ , $T = 25^{\circ}C$ Note 1 $0 < V_{PD} < 4.6$ , $V_{DD} = 5V$ , $T = 25^{\circ}C$ Note 1 $0.4 < V_{PD} < 5$ , $V_{DD} = 5V$ , $T = 25^{\circ}C$ Note 1 $T_{amb} = -25^{\circ}C$ to $+60^{\circ}C$
	$I_{HD}$	-1.9	-2.5	-3.1	mA	
Low current mode	$I_{LU}$	0.475	0.625	0.775	mA	
	$I_{LD}$	-0.475	-0.625	-0.775	mA	
Tristate	$I_Z$		50		nA	
<b>Output Signal FVN</b>						
Output voltage low	$V_{OL}$			0.4	V	Open drain output $I_{OL} = 1mA$ $C_L = 30pF$
Output low pulse width	$t_{WL}$			1/FI		
<b>Output Signals MOD, PORT</b>						
Output voltage high	$V_{OH}$	$V_{DD}-0.4$			V	Push-pull output $I_{OH} = 0.5mA$ $I_{OL} = 0.5mA$
Output voltage low	$V_{OL}$			0.4	V	
<b>Output Signal LD</b>						
Output voltage low	$V_{OL}$			0.4	V	Open drain output $I_{OL} = 3mA$ , $C_L = 30pF$ Loop locked Loop not locked FVN = FI/N $f_C = RI/R$
Output low pulse width	$t_{WL}$		10	1/FVN 1/ $f_C$	ns	

Note 1 Temperature coefficient for current is typically  $-0.7\%/^{\circ}C$

NJ88C33

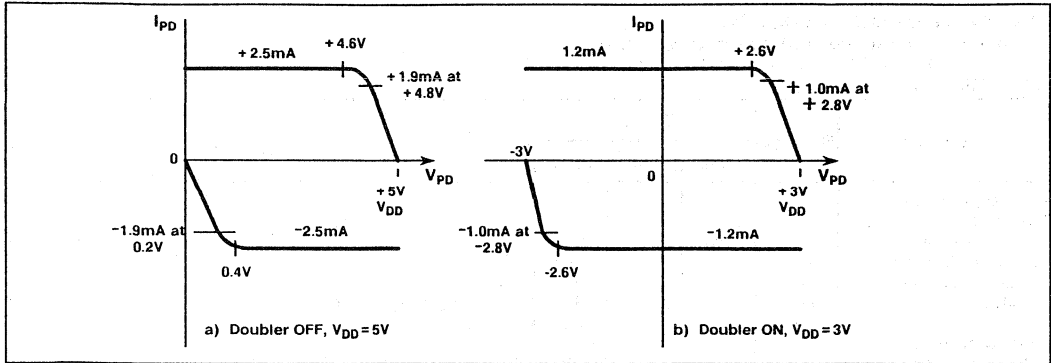


Fig.4 Typical output signal PD, high current mode

VOLTAGE DOUBLER  $V_{DD} \leq 3V$

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C Output voltage	$V_C$	$-V_{DD}$		$-V_{DD} + 0.8V$	V	$f_{VD} = 2MHz, I_{OC} = 0\mu A, V_{DD} = 3V$ $f_{VD} = 2MHz, I_{OC} = 100\mu A, V_{DD} = 3V$
		$-V_{DD}$		$-V_{DD} + 1.5V$	V	
Current Consumption	$I_D$			100	$\mu A$	$f_{VD} = 2MHz, I_{OC} = 0\mu A, V_{DD} = 3V$

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI Input frequency Input frequency Rise time Fall time Slew rate	$f_{max}$	0		52	MHz	$V_{DD} = 2.7V$
	$f_{max}$	0		10	MHz	
	$t_R$			1.5	$\mu s$	
	$t_F$			1.5	$\mu s$	
		3			$V/\mu s$	
Input Signal FI Input frequency Input frequency Rise time Fall time Slew rate	$f_{max}$	0		52	MHz	Dual modulus $V_{DD} = 2.7V$
	$f_{max}$	0		20	MHz	
	$t_R$			1.5	$\mu s$	
	$t_F$			1.5	$\mu s$	
		3			$V/\mu s$	
Input Signal FI Input frequency Input frequency Rise time Fall time Slew rate	$f_{max}$			150	MHz	Single modulus $V_{DD} = 2.7V$
	$f_{max}$	0		52	MHz	
	$t_R$	0		1.5	$\mu s$	
	$t_F$			1.5	$\mu s$	
		3			$V/\mu s$	
Output Signal PORT Rise time Fall time	$t_R$			1	$\mu s$	$C_L = 30pF$ $C_L = 30pF$
	$t_F$			1	$\mu s$	
Output Signal FVN Fall time	$t_F$		20		ns	$C_L = 30pF$
Output Signal MOD Rise time Fall time Delay time (L-H) Delay time (H-L)	$t_R$			10	ns	$C_L = 30pF$ $C_L = 30pF$ $C_L = 30pF$ Measured from +Ve edge of FI $C_L = 30pF$ Measured from +Ve edge of FI
	$t_F$			10	ns	
	$t_{DLH}$			15	ns	
	$t_{DHL}$			15	ns	

**PHASE COMPARATOR**

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency ( $f_C = R1/R$ ), and  $f_{VN}$ , the divided-down VCO frequency ( $F1/N$ ).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When  $f_C$  leads  $f_{VN}$  the PD output goes high; when  $f_{VN}$  leads  $f_C$  it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO.

No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between  $f_C$  and  $f_{VN}$ .

When the phase difference between  $f_C$  and  $f_{VN}$  is too small to be resolved by the phase detector then no current pulses are produced. In this region the loop does not reduce the close-in noise on the VCO output. This can be overcome using a very high value resistor to leak a few nanoAmps of current from the filter and keep the loop on the edge of the region.

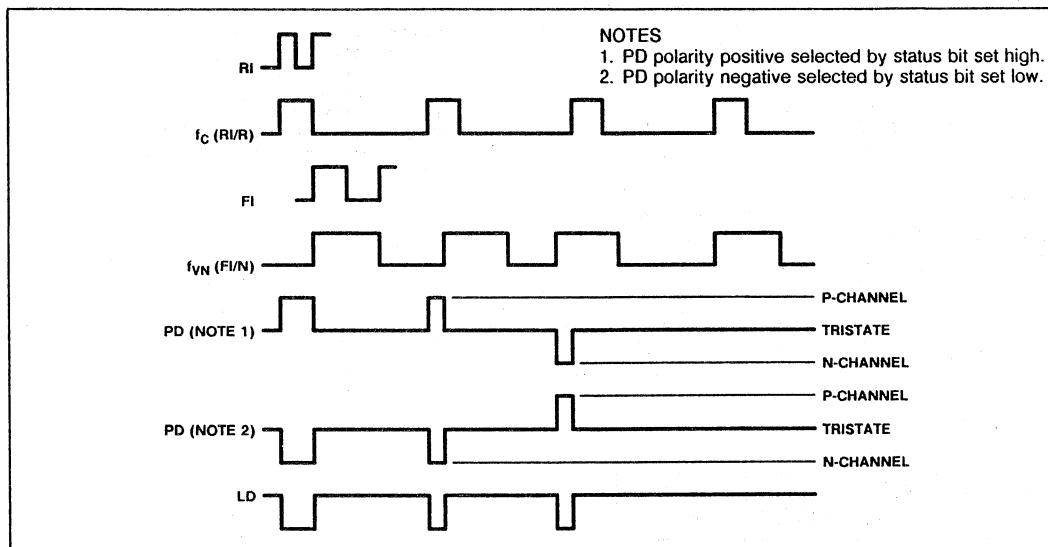


Fig.5 Phase comparator phase diagram

**PROGRAMMING**

**Transmission Protocol**

I<sup>2</sup>C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line, SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

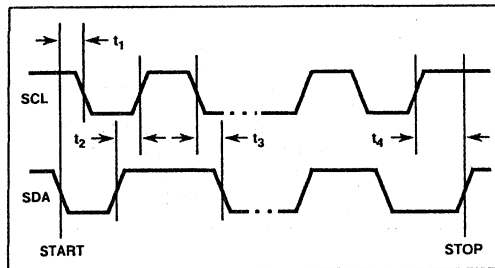


Fig.6 I<sup>2</sup>C timing diagram

**I<sup>2</sup>C TIMING INFORMATION**

VDD = 4.5V to 5.5V, Tamb = -40°C to +85°C

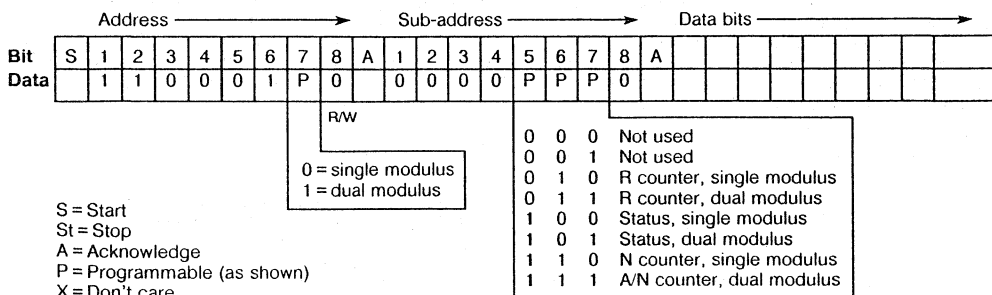
Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	$f_{SCL}$		5	MHz
SCL hold after START	$t_1$	20		ns
Data set-up time	$t_2$	20		ns
Data hold after SCL low	$t_3$	0		ns
SCL set-up before STOP	$t_4$	20		ns

# NJ88C33

## Address and Sub-Address Formats

The correct addressing sequence for the NJ88C33 is shown below. The START condition is followed by the address byte, the acknowledge from the NJ88C33, the sub-

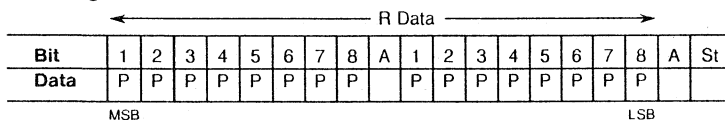
address byte, another acknowledge then the associated data. The correct values for each address and sub-address are listed, together with the message selection options.



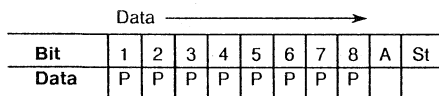
## Data Formats

Each of the data formats should be preceded contiguously by the addressing sequence given above.

**R counter : single or dual modulus**



**Status : single or dual modulus**

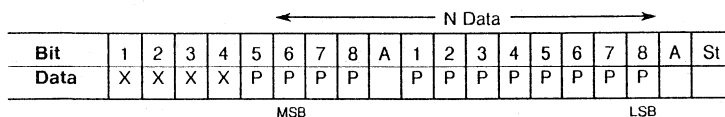


Status Byte		
Bit	0	1
1	PORT = low	PORT = high
2	Counters off <sup>(1)</sup>	Counters on
3	FI and RI off <sup>(2)</sup>	FI and RI on
4	PD = polarity negative	PD = polarity positive
5	PD bias = 0.625mA	PD bias = 2.5mA
6	$f_{VD} = RI/2$	$f_{VD} = RI/4$
7	Doubler off	Doubler on <sup>(3)</sup>
8	MOD = push-pull	MOD = open drain

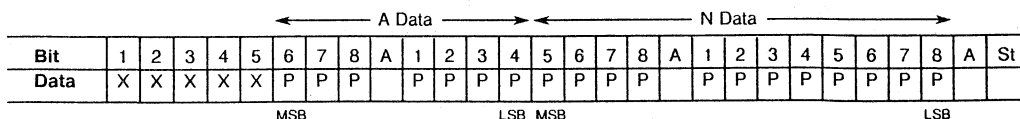
## NOTES

1. In this standby mode the counters are disabled but the voltage doubler and I<sup>2</sup>C interface can both function.
2. In this standby mode the FI and RI preamplifiers are disabled, which stops the counters and the voltage doubler. The I<sup>2</sup>C interface still operates.
3. The voltage doubler should only be used when V<sub>DD</sub> ≤ 3.0V

**N counter : single modulus**



**A/N counters : dual modulus**



**APPLICATION CIRCUITS**

**Single Modulus**

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency  $f_c$ . When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop filter to produce the VCO voltage drive. When the VCO loop is locked,  $F1/N = f_c$  i.e., the VCO frequency is  $N \times f_c$ .

Using a prescaler with a division ratio P, the smallest VCO output frequency step is  $Pf_c$  and the VCO frequency is  $PNf_c$ .

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

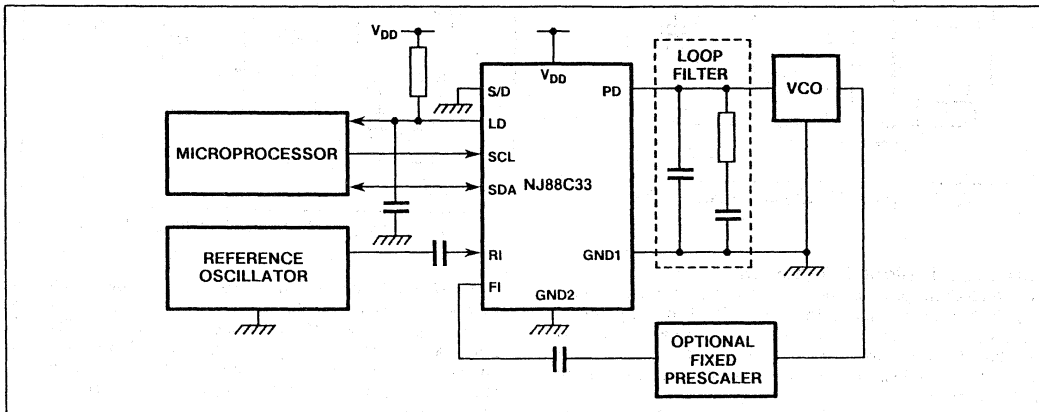


Fig.7 Single modulus application

**Dual Modulus**

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size,  $f_c$ . In this mode, a dual modulus prescaler (with ratios P and P+1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P+1 for A cycles of F1. The VCO frequency is given by  $PNf_c + Af_c$ . Note that programming A=0 produces a count of 128 cycles.

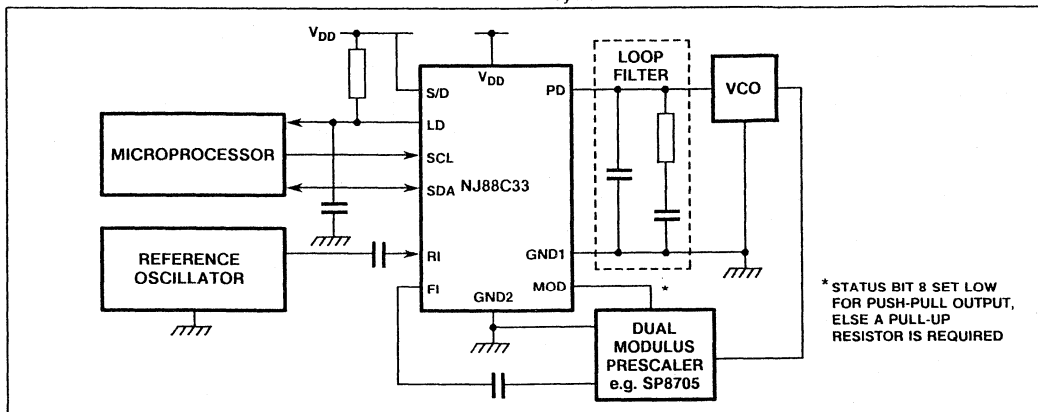


Fig.8 Dual modulus application

## NJ88C33

### VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

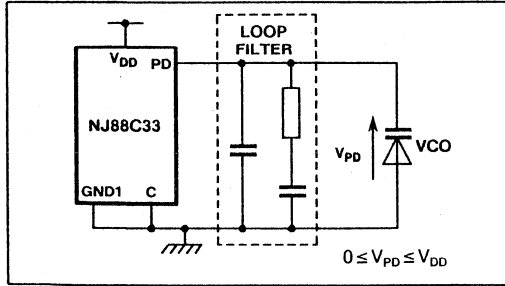


Fig.9 Driving a VCO without voltage doubler

### Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I<sup>2</sup>C bus rate of 100kHz or at 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

### VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1 $\mu$ F be connected from C to GND1.

The voltage doubler is designed to boost VCO drive in low voltage applications.

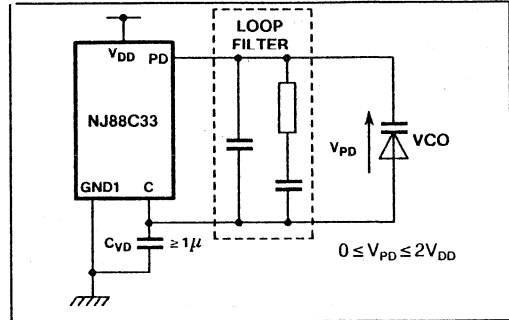


Fig.10 Driving a VCO using the voltage doubler

The NJ88C33 evaluation board (Fig. 11) demonstrates the preferred layout technique - providing a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN94, 'Using the NJ88C33 PLL Synthesiser' explains the design equations and demonstrates the use of the device, and is available from your local GPS customer service centre.



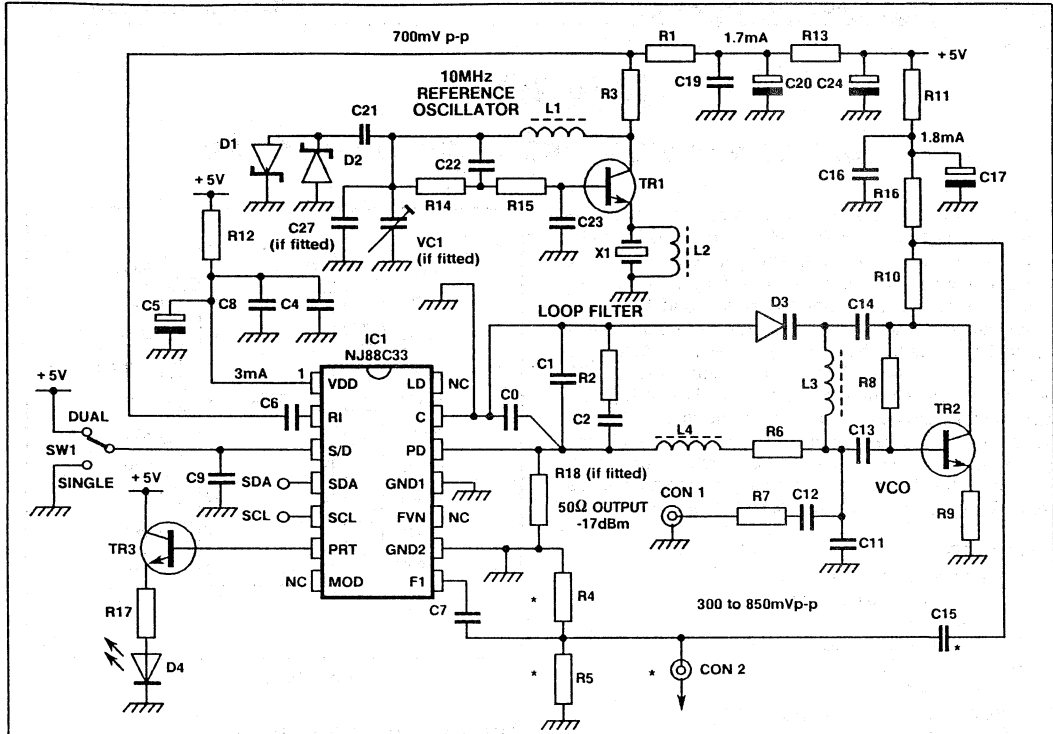


Fig.11 Typical applications circuit

\* Insert C15, delete R4 and R5 if CON2 is to be used to monitor the VCO. Delete C15 insert R4 and R5 if CON is to provide an external source, otherwise short C15 and delete R4, R5 and CON2.

**COMPONENT LIST FOR FIG.11**

Capacitors		Resistors	Inductors	Miscellaneous					
C0	1nF 10%	C17	22μF/35V Elect.	R1	270Ω	L1	15μH 10%	IC1	NJ88C33
C1	100nF 10%	C19	10nF 10%	R2	470Ω	L2	220μH 10%	X1	10.00MHz 5ppm series
C2	1μF Tant.	C20	22μF/35V Elect.	R3	330Ω	L3	180nH 20%	SW1	Miniature slide switch
C4	10nF 10%	C21	10nF 10%	R4	100Ω	L4	470μH 10%	CON1	SMC socket
C5	22μF/35V Elect.	C22	10nF 10%	R5	100Ω	<b>Diodes</b>		CON2	SMC socket
C6	10nF 10%	C23	22pF 5% NPO	R6	1kΩ			D1	1N6263 Schottky
C7	1nF 10%	C24	22μF/35V Elect.	R7	120Ω	D2	1N6263 Schottky		
C8	1nF 10%	C27	22pF 5% NPO	R8	27kΩ	D3	BBY40 varicap		
C9	1nF 10%	VC1	3p5-22p	R9	Link	D4	5mm red LED		
C11	150pF 5% NPO			R10	1kΩ	<b>Transistors</b>			
C12	1nF 10%			R11	10Ω			TR1	BFS17 RF NPN
C13	1nF 10%			R12	10Ω	TR2	BFS17 RF NPN		
C14	2p7 ± 0.5pF NPO			R13	10Ω	TR3	2N3904 Switching		
C15	10nF 10%			R14	22kΩ				
C16	10nF 10%			R15	2.7kΩ				
				R16	330R				
				R17	100Ω				
				R18	33MΩ				

**NOTES**

1. With the exception of electrolytics, all capacitors are surface mount types
2. All resistors are 0.25W, ±2%
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.
4. R18 may be required to optimise VCO close in noise performance.

# NJ88C50

## DUAL LOW POWER FREQUENCY SYNTHESISER

The NJ88C50 is a low power integrated circuit, designed as the heart of a fast locking PLL subsystem in a mobile radio application. It is manufactured on GEC Plessey Semiconductors 1.4 micron double polysilicon CMOS process, which ensures that low power and low noise performance is achieved. The device contains two synthesisers, one for the generation of VHF signals up to 125MHz and a second for UHF (when used with a mult modulus prescaler such as the SP8713/14/15). The main synthesiser has the capability of driving a dual speed loop filter and also can perform Fractional-N interpolation. Both synthesisers use current source outputs from their phase detectors to minimise external components. Various sections may be powered down for battery economy.

### FEATURES

- 30MHz main synthesiser
- 125MHz auxiliary synthesiser
- Programmable output current from phase detector - up to 10mA
- High input sensitivity
- Fractional-N interpolator
- Supports up to 4 modulus prescalers
- SSOP package

### APPLICATIONS

- NMT, AMPS, ETACS cellular
- GSM, IS-54, RCR-27 cellular
- DCS1800 microcellular
- DLMR, DSRR, TETRA
- DECT, PHP cordless telephones

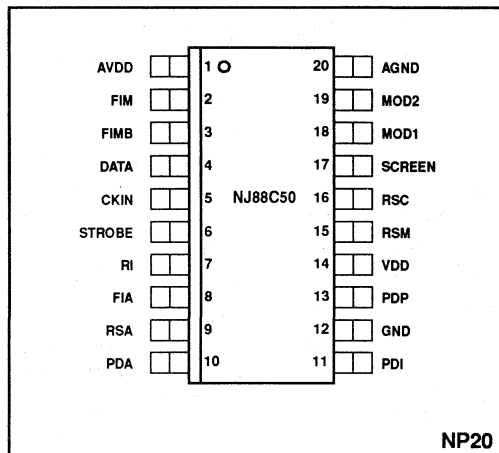


Fig.1 Pin assignment

### ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +150°C
Operating temperature	-40°C to +85°C
Supply voltage	-0.5 to 7.0V
Voltage on any pin	-0.3V to (VDD + 0.3V)

### ORDERING INFORMATION

NJ88C50\IG\NPAS - (Industrial temp range in SSOP package)

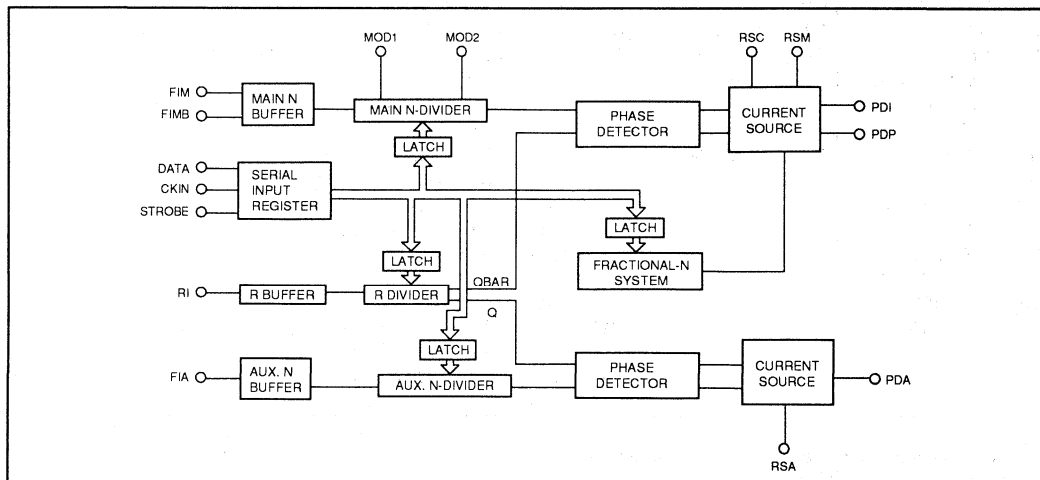


Fig.2 Simplified block diagram

**ARCHITECTURE**

Fig.2 shows a simplified block diagram of the NJ88C50, a more detailed description of each block and its function is given later in this datasheet.

The synthesiser consists of the following blocks

- 35MHz reference frequency input buffer
- 35MHz programmable reference divider
- 125MHz Auxiliary synthesiser input buffer
- 125MHz Auxiliary synthesiser programmable divider
- Auxiliary synthesiser phase detector with current source outputs
- 30MHz main synthesiser input buffer (differential inputs)
- 30MHz main synthesiser programmable divider and control logic
- Main synthesiser Fractional-N interpolation system
- Main synthesiser phase detector with dual current source outputs

**PIN DESCRIPTION**

Pin	Name	Function
1	AVDD	Analog supply pin (nominally 5V).
2	FIM	Main synthesiser balanced input buffer, may be used with single ended prescaler output if Fimb is biased.
3	FIMB	Main synthesiser balanced input buffer, may be used with balanced prescaler output, or biased for single ended operation.
4	DATA	Serial input for programming data.
5	CKIN	Serial clock input for programming bus.
6	STROBE	Program enable pin, active low.
7	RI	Master reference frequency input, should be a.c coupled from an accurate source.
8	FIA	Auxiliary synthesiser frequency input, should be a.c coupled.
9	RSA	Current setting resistor connection defining auxiliary phase detector output current.
10	PDA	Tristate current output from auxiliary phase detector.
11	PDI	Tristate current output from the main synthesiser's phase detector giving integral control.
12	GND	Digital ground supply pin.
13	PDP	Tristate current output from the main synthesiser's phase detector giving proportional control.
14	VDD	Digital supply pin (nominally 5V).
15	RSM	Current setting resistor connection defining main synthesiser's phase detector output currents.
16	RSC	Current setting resistor connection defining the compensation current for fractional-N ripple elimination in the main synthesiser's current source outputs.
17	SCREEN	To be connected to ground to provide isolation of the modulus control pins from RF interference.
18	MOD1	Modulus control pin (see truth table).
19	MOD2	Modulus control pin (see truth table).
20	AGND	Analog ground supply pin.

It is recommended that power supply pins are well decoupled to minimise power rail born interference.

## NJ88C50

### FUNCTIONAL DESCRIPTION

The NJ88C50 has been designed using a modular concept, and its operation can be best summarised as these component blocks.

#### Reference divider

The reference divider is used to provide the reference signals needed for both the main and auxiliary synthesiser phase detectors. The divider allows for a twelve bit number to be loaded, via the serial bus, to select the required division ratio. Division ratios of 3 to 4095 can be used.

The reference divider input stage will accept a low level, AC coupled, sinewave input. It is anticipated that in most systems this will be provided by a stable reference source up to 35MHz, and so encompasses all the common TCXO (temperature controlled crystal oscillator) frequencies, such as 9.6, 12.8, 13.0, 19.44 and 26MHz.

A standby mode is supported so that the reference divider can be powered down, this is achieved using two of the serial program control bits.

To reduce the possibility of unwanted interaction between the main and auxiliary synthesisers, the charge pumps do not take current at the same time. To achieve this the output of the reference divider has a duty factor of approximately 50:50, which then allows the Q and QBAR taps to be used for the auxiliary and main synthesisers respectively. By doing this the current pulses can be taken alternatively, minimising modulation of the power supply rails as current is drawn.

The reference divider consists of a 12 bit programmable divider followed by a 4 bit binary counter. This 4 bit counter gives a choice of divide by M, 2M, 4M or 8M.

A pair of programmable control bits are used to determine which of the divide by M, 2M, 4M or 8M outputs is supplied to the auxiliary synthesiser's phase detector and a further pair of control bits are used to determine which are supplied to the main synthesiser's phase detector.

#### Auxiliary synthesiser

The auxiliary synthesiser operates over an input frequency range from 1 to 125MHz, without the use of an external prescaler. The synthesiser consists of a 12 bit N divider and a digital phase comparator with current source outputs. The reference frequency is supplied by the shared reference divider. Current source outputs allow a passive loop filter to be used.

When the auxiliary synthesiser is not in use, a standby mode is supported so that power consumption is reduced. This is achieved using one of the serial program control bits.

The divider is programmed with a 12 bit word allowing division ratios of 3 to 4095 to be used.

The auxiliary phase detector consists of the 2 D-type phase and frequency detector shown in Figure.3 below, the high and low outputs of which drive on-chip, opposing complementary charge pumps. This type of phase detector design eliminates non linearity or deadband around the zero phase error (locked) condition.

The charge pump output current level is set by an external resistor on the RSA pin (pin 9) up to a limit of  $250\mu\text{A} \pm 10\%$ . A pull up current pulse will indicate that the VCO frequency must be increased, whilst a pull down pulse indicates that the frequency must be decreased.

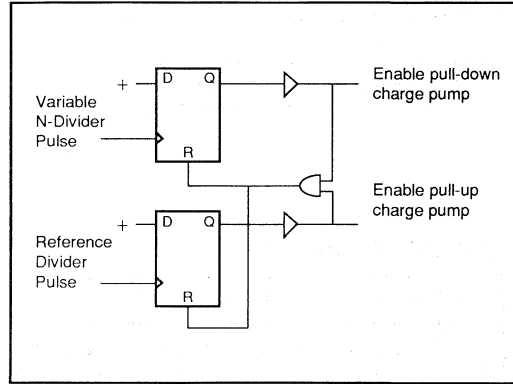


Fig.3 Auxiliary phase detector

#### Main Synthesiser

The main synthesiser is capable of operating at frequencies up to 30MHz. The synthesiser uses the 12 bit reference divider, shared with the auxiliary synthesiser, a 12 bit up/down N divider and a digital phase comparator with current source outputs.

The device also has a number of features which increase the design flexibility and performance of the synthesiser. These include fractional-N operation, speed up mode and support of 2, 3 and 4 modulus prescalers. A description of the operation and advantages of each of these features is given.

The main N divider input buffer will accept inputs from an external prescaler, either as balanced (2 wire) ECL levels at frequencies up to 30MHz, or DC coupled to a single ended prescaler output. Single ended operation requires the other buffer input (pin 3) to be externally biased to the correct slicing voltage for the prescaler and also externally decoupled.

If the inputs are in the form of balanced ECL levels, there must not be a skew of greater than 2ns between one input changing and the second input changing. The relationship of the signals is shown below in Fig.4.

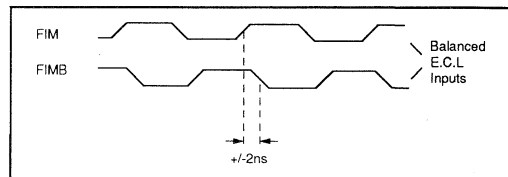


Fig.4 Maximum input skew

The main N divider is programmable so that it can determine how many cycles of each division ratio the external prescaler will perform.

The total division ratio of the output from the system VCO by the synthesiser's phase detector may be expressed as  $N_{TOT}$  and R1, R2, R3 and R4 are the available prescaler ratios and N1, N2, N3 and N4 are the corresponding number of cycles for each ratio selected, within one complete division cycle.

The divider is programmed via the serial data bus and the values needed to be programmed for each of the possible prescaler ratios are as follows:-

In 2 modulus mode (division ratios R1, R2)

$$N_{TOT} = N1.R1 + N2.R2$$

Programmed values needed:

N1 - a 12 bit value giving the number of times R1 is to be used  
N2 - a 8 bit value giving the number of times R2 is to be used

In 3 modulus mode (division ratios R1, R2, R3)

$$N_{TOT} = N1.R1 + N2.R2 + N3.R3$$

Programmed values needed:

N1 - a 12 bit value giving the number of times R1 is to be used  
N2 - a 4 bit value giving the number of times R2 is to be used  
N2+N3 - a 4 bit value where N3 is the number of times R3 is to be used and (N2+N3) is modulo-16 addition

In 4 modulus mode (division ratios R1, R2, R3, R4)

$$N_{TOT} = N1.R1 + N2.R2 + N3.R3 + N4.R4$$

Programmed values needed:

N1 - a 12 bit value giving the number of times R1 is to be used  
N2 - a 4 bit value giving the number of times R2 is to be used  
N2+N3 - a 4 bit value where N3 is the number of times R3 is to be used.  
N2+N3+N4 - a 4 bit value where N4 is the number of times R4 is to be used. (N2+N3) and (N2+N3+N4) are modulo-16 addition.

To facilitate the use of multimodulus prescalers the N divider is based upon a twelve bit up/down counter which functions as follows

The first value, N1, is loaded into the counter which then counts down from N1 to zero. During this time, the modulus ratio R1 is selected.

When the counter reaches zero modulus R2 is selected and the counter then counts up to the N2 value. If 2 modulus operation is chosen, the counter is then reloaded with N1 and the count is repeated.

For operation with 3 or 4 modulus devices, the counter continues to count up once it has reached the N2 value. The count continues to the N2+N3 value and during this time the R3 ratio is selected. In the 3 modulus case, when the N2+N3 value is reached the counter is then reloaded with the N1 value and the modulus ratio R1 is selected.

For 4 modulus operation the counter will continue its count up to the N2+N3+N4 value before reloading the N1 value. During this time the R4 modulus is selected.

If N2, N3, or N4 are set to zero this will give a full count of 16 for the corresponding modulus.

The N divider block also has a special control line from the Fractional-N logic. When required this control will cause the total division ratio to be increased from N to N+1. This is achieved by forcing a cycle which would have normally used a prescaler ratio R1 to use ratio R2 instead. R1 and R2 are chosen so that R2 equals R1+1.

Further explanation of the operation of the synthesiser when using 2, 3 or 4 modulus prescaler is given in the section on multimodulus division (page 8).

The phase detector used on the main synthesiser is similar to the type used on the auxiliary synthesiser (Figure.3). In this case, however, the detector will drive two pairs of complimentary charge pumps, one of which is intended to drive the loop integrator capacitor to provide integral control, whilst the other provides proportional control for the VCO. This system is shown in Fig 5, and has applications where fast locking of the loop is required.

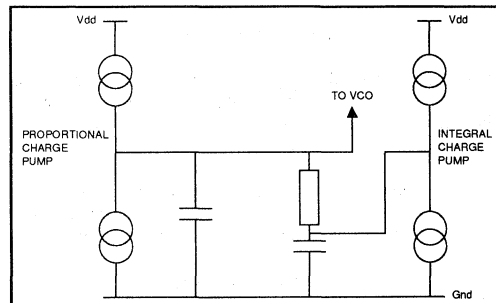


Fig.5 Loop filter using both charge pumps

## MODES OF OPERATION

### Normal Mode

The synthesiser will operate in normal mode while the strobe line of the serial data bus is low. In this mode the following current levels are produced. The charge pump providing the proportional feedback term will have a normal current level designated by  $I_{prop}(0)$ , that is set by an external bias resistor, RSM.  $I_{prop}(0)$  will vary when different N-divider ratios are programmed, so that it is proportional to the total division ratio. To avoid the necessity of computing the total division ratio on chip, an eight bit number representing the most significant bits of  $N_{tot}$  will be loaded via the serial data bus.  $I_{prop}(0)$  is therefore given by

$$I_{prop}(0) = CN.I_{bo}$$

where CN is the loaded eight bit number and the value  $I_{bo}$  is scaled from the external current setting resistor RSM where  $I_{bo} = I_{rsm}/32$ . Typically  $I_{bo} = 1\mu A$ , and therefore  $I_{prop}(0)$  will have a maximum value equal to  $255\mu A$ .

## NJ88C50

The normal value of  $I_{prop}$ ,  $I_{prop}(0)$ , is obtained while the strobe line of the serial programming bus is held low. In this condition, the second charge pump providing the integral feedback term is inactive.

### Speed up Mode

In speed up mode the loop bandwidth during switching is increased to allow faster initial frequency acquisition. This is done by using the dual phase detector outputs (PDP and PDI) connected to a standard passive loop filter as shown in fig.5. The effect of this is to increase the loop gain and hence the bandwidth while maintaining a constant phase margin when switching between speed up mode and normal mode.

The synthesiser operates in speed up mode when the strobe line goes high loading either word A or word A2 (see programming section Page 8-Page 9) and it will stay in this mode until the strobe line goes low. In this mode the following current levels are produced. The charge pump providing the proportional feedback will increase its current from  $I_{prop}(0)$  to a value  $I_{prop}(1)$ , where

$$I_{prop}(1) = 2^{L-1} \cdot I_{prop}(0)$$

where L is a two bit number loaded as part of the serial programming data.  $I_{prop}(1)$  will therefore be 2, 4, 8 or 16 times  $I_{prop}(0)$ . The charge pump supplying  $I_{prop}$  is specified up to a value of 1mA.

Also when the strobe line goes high loading word A or word A2, the charge pump providing the integral feedback term becomes active at a current level  $I_{int}$  given by

$$I_{int} = K \cdot I_{prop}(1)$$

where K is a four bit number loaded as part of the serial programming data. Although  $I_{int}$  can be programmed to be 240 times greater than  $I_{prop}(0)$ , the charge pump supplying  $I_{int}$  is only specified up to a value of 10mA.

For all charge pumps, a pull-up current indicates the VCO frequency should be increased while a pull-down current indicates the VCO frequency should be decreased.

For the proportional and integral charge pumps, the selected pulse current levels will remain substantially constant over the charge pumps output voltage ranges tabulated in the electric characteristics. "Substantially constant" means that the current will not have changed by more than 10% of the value measured at 2.5 volts on the output.

## FRACTIONAL-N OPERATION

Conventional, non fractional-N synthesisers have a frequency resolution or step size equal to the phase detector comparison frequency. Fractional-N refers to a technique which allows finer frequency steps to be obtained.

The synthesised frequency with a conventional synthesiser is equal to N times the phase detector comparison frequency, where N is the programmable integer loop divide

ratio. Using fractional-N the value of N is alternated between N and N+1 in order to simulate a fractional part. For example 9000.375 would be simulated by alternating between 9000 and 9001 in the pattern

9000, 9000, 9001, 9000, 9000, 9001, 9000, 9001 (mean value of 9000.375).

On the NJ88C50 the fractional-N circuit consists of an accumulator which can be set to overflow at a value of 5 or 8 (FMOD in programming word D, see page 9). The value in the accumulator, A, is incremented once every comparison cycle of the main phase detector and every time the accumulator overflows the total division ratio of the synthesiser and prescaler is increased from N to N+1. To obtain the pattern described above N=9000 and FMOD would be set to mod8 and the incremental value, NF(programmed in word A) would be set to 3. The accumulator would then behave as shown below.

Increment Value	Accumulator Value	Total Division Ratio
3	3	9000
3	6	9000
3	1	9001
3	4	9000
3	7	9000
3	2	9001
3	5	9000
3	0	9001

Varying NF allows different fractions to be obtained. If NF=1 and FMOD=8 the accumulator would overflow once in every 8 cycles giving a value of 9000.125. Similarly if NF=4 the accumulator overflows every other cycle giving 9000.5.

For a given step size this increase in resolution means a higher comparison frequency at the phase detector, and therefore a lower overall division ratio. For example,

$$\begin{aligned} \text{with a step size} &= 200\text{kHz} \\ \text{and carrier frequency} &= 900\text{MHz} \end{aligned}$$

Non fractional-N synthesiser  
Comparison frequency=200kHz  
Division ratio=900MHz=4500  
200kHz

Fractional-N synthesiser (using 5ths)  
Comparison frequency=1MHz  
Division ratio=900MHz=900  
1MHz

In most applications the phase noise is proportional to the overall division ratio. Therefore fractional-N gives lower phase noise. This higher comparison frequency and lower phase noise allows circuits to be built with wider loop bandwidths while keeping the same stability. This means that phase locked loops (PLLs) can be made to either switch faster for a given phase noise or be quieter for a given switching speed, compared to conventional designs.

However the alternation between the N and N+1 values causes a ripple in the output frequency. This ripple is not desirable in radio frequency synthesisers. This ripple or jitter waveform is predictable from the pattern of N and N+1 values and so can be cancelled.

The instantaneous accumulator value, A, is proportional to the cumulative frequency error caused by ignoring the fractional part during the periods of the divide by N. The accumulator value, A, may therefore be used to generate a waveform corresponding to the jitter waveform, that is then used to cancel the jitter out of the phase detector. This jitter compensation current pulse is equal to A.Icomp where Icomp represents the step size as A is incremented.

Corresponding to the two alternative values of Iprop, Iprop(0) and Iprop(1), Icomp will take the values Icomp(0) and Icomp(1). Icomp is always pull-up, and the magnitude of its steps for perfect jitter compensation are related to the value of Iprop by the factors

$$0, 1/Q.Ntot, 2/Q.Ntot, 3/Q.Ntot \dots\dots Q-1/Q.Ntot$$

where Q = accumulator modulus in use (5 or 8)

Since

$$Iprop(0) = CN.Ibo$$

and CN is an approximation to Ntot apart from a scaling factor, the value of Icomp(0) required becomes independent of Ntot and its steps are

$$0, 1/Q, 2/Q, 3/Q \dots\dots Q-1/Q \text{ times } Ibo.(\text{scaling factor})$$

where scaling factor =  $\frac{\text{Max. value of CN to be used}}{\text{Corresponding max. value of Ntot}}$

$$\text{therefore } Ico = 1 \times \frac{CN(\text{max})}{Q \cdot Ntot(\text{max})} \times Ibo$$

$$\text{and } Icomp(0) = A.Ico$$

where Ico is scaled from the external current setting resistor RSC.

$$Ico = Irsc/128.$$

Typically Ntot(max) might be 10000, with CN(max)=250 and Q=8, so the current step will be of magnitude Ibo/320. Since Ibo is only 1 uA, this is a very small value; however this value only applies if Icomp is a continuous current. Icomp however will be a short current pulse coincident with the Iprop pulse, in order to cancel jitter components over the widest possible frequency range.

When the duty factor of Icomp is taken into account, its pulse value may be increased accordingly. Icomp is therefore generated as a pulse of fixed width equal to two periods of the input reference clock frequency, with a timing that straddles the active edge of the reference divider output pulse supplied to the main phase detector, as shown below: (Fig 6).

Since the duty factor of Icomp is 2/M and depends on the value of M programmed, it is possible to set the peak pulse value of Icomp(0) by means of the external current setting resistor RSC to correspond with the value of M intended, the value of 'scaling factor' defined above, the accumulator modulus Q and the value of Ibo set by the other current setting resistor.

$$\text{therefore } Ico = 1 \times \frac{Nmax}{Q \cdot Ntot(\text{max})} \times \frac{M}{2} \times Ibo$$

This gives a typical value for Ico of 0.1µA.

The two values of Icomp, Icomp(0) and Icomp(1) are related by

$$Icomp(1) = 2^{L-1} \cdot Icomp(0)$$

Icomp(0) occurring when the strobe line is low and Icomp(1) occurring when the strobe line is high loading either WORDA or WORDA2 (see programming section, page 8 and 9).

Corresponding to the pull-up pulse Icomp(1) that is added to the proportional charge pump pulse Iprop(1), there is also a pull-up current pulse Icomp2 which is added to the integral charge pump pulse lint. This pulse Icomp2 only applies when the strobe line is high (loading either WORDA or WORDA2). When the strobe line is low there will be no lint or Icomp2 pulses. The value of Icomp2 is given by

$$Icomp2 = Icomp(1).K$$

where K is a four bit number entered as part of the serial programming data.

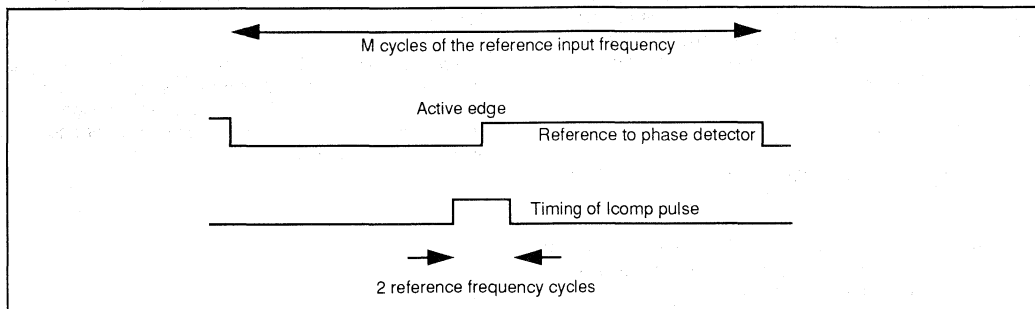


Fig.6

## NJ88C50

### MULTIMODULUS DIVISION

The NJ88C50 supports the use of 2, 3 and 4 modulus prescalers. Two modulus prescalers such as the SP8714/15 are commonly used in PLLs. Additional information on using 2 modulus prescalers can be found in application note AN132 in the GEC Plessey Semiconductors Personal Communications handbook (May 1992).

When using a 2 modulus prescaler ( $R/R+1$ ) the minimum division ratio above which all channels can be synthesised is given by

$$\text{Minimum division ratio} = R(R-1)$$

eg. for a 64/65 prescaler such as the SP8714/15

$$\text{Minimum division ratio} = 64(64-1) = 4032$$

When fractional-N operation is being used higher comparison frequencies are used, which are obtained by using lower division ratios. Use of a 3 or 4 modulus prescaler allows the minimum division ratio to be lowered.

For a 3 modulus prescaler ( $R/R+1/R+A$ )

$$\text{Minimum division ratio} = \frac{R(R+A+1)+A}{A}$$

eg. for a 64/65/72 prescaler such as the SP8713

$$\text{Minimum division ratio} = \frac{64(64+8+1)+8}{8} = 1096$$

For a 4 modulus prescaler ( $R/R+1/R+A/R+B$ )

$$\text{Minimum division ratio} = \frac{R(A+B+R+1)+A+B}{A \ B}$$

eg. for a 64/65/68/80 prescaler

$$\text{Minimum division ratio} = \frac{64(4+16+64+1)+4+16}{4 \ 16} = 852$$

An example of where three modulus division would be implemented is given below.

The system in which the synthesiser is to operate has a lowest carrier frequency of 900MHz and a channel spacing of 30kHz. However due to the lock up time requirements fractional-N operation is being used in its 8ths mode (see section on fractional-N operation), giving a comparison frequency of  $30\text{kHz} \times 8 = 240\text{kHz}$ .

Therefore,

$$\text{Minimum division ratio required} = \frac{900 \times 10^6}{240 \times 10^3} = 3750$$

If a 64/65 prescaler is used not all the channels will be selectable as the minimum required division ratio is less than the minimum allowable division ratio (4032).

If a 64/65/72 prescaler is used all the channels will now be selectable as the minimum required division ratio will now be greater than the minimum allowable division ratio (1096).

### SERIAL DATA BUS

The data needed to program the synthesiser is entered via a high speed (10MBit/s) 3-wire bus, with serial data, serial clock and strobe pins. The input data is partitioned so that after initial programming the output frequency can be changed by re-programming only 24 or 32 bits. The timing diagram for the bus is given in Fig. 7.

The data is programmed as either four twenty-four bit words or three twenty-four bit words and one thirty-two bit word. When initially programmed words A, B, C and D are loaded, though if the auxiliary synthesiser is disabled C is not needed. Following the initial programming the frequency can be subsequently shifted in one of the following ways:

- If a 2 or 3 ratio prescaler is being used and CN does not need to be reprogrammed word A should be loaded.
- If a 2 or 3 ratio prescaler is being used and CN does need to be reprogrammed word A2 should be loaded. In wide frequency band systems CN must be reprogrammed for best performance every time the frequency is changed.
- If a four ratio prescaler is being used word A and word B should be loaded

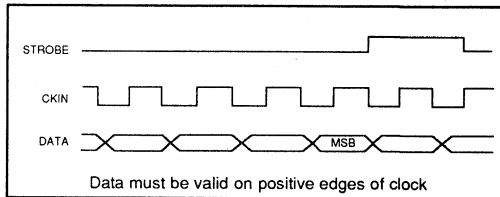


Fig. 7

A strobe pulse occurs at the end of each word and loads the contents of the input shift register into the working registers, except when word B is being loaded, in which case the shift register contents are loaded into a temporary register and then loaded into the working register when either word A or A2 is loaded. The information is transferred on the rising edge of the strobe pulse which should occur one half clock period after the clock edge on which the MSB of a word is shifted in.

If word A or word A2 is being loaded, when the strobe goes high the main synthesiser will be put into speed-up mode. This mode will be maintained while the strobe remains high. During this time any pulses on the clock input will not affect the function of the synthesiser.



The information contained within each word is given below. Data bits are shifted in on the leading clock edge, with the least significant bit(LSB) of the word first and the MSB of the word last. (Note that individual sections of data within a word are loaded with the MSB of that section first. An example of this is given after this description of Word A)

Word Format

MSB.....LSB

Word A

|0| NF | N1 | N2 or N2 and N2+N3|  
 |3 bits| 12 bits | 8 bits |

NF = Fractional-N incremental value. (MSB first)  
 N1 = Number of cycles prescaler ratio R1 is used. (MSB first)  
 N2 = Number of cycles prescaler ratio R2 is used. (MSB first)  
 N3 = Number of cycles prescaler ratio R3 is used. (MSB first)  
 If a two modulus prescaler is being used N2= 8 bits.  
 If a three or four modulus prescaler is being used  
 N2 = 4 bits and N2+N3= 4 bits(modulo-16 addition).

Therefore if the following values are required NF=3  
 N1=51 N2=25 the input word would be

0            110   110011000000   10011000  
               NF            N1                    N2

Word A2

|0| NF | N1 | N2 or N2 and N2+N3 | CN |  
 |3 bits| 12 bits | 8 bits | 8 bits |

CN = Scaling factor for current setting. (MSB first)

Word B

|1000| N2+N3+N4| CN | K | L | P1,P2 |  
 | 4 bits | 8 bits|4 bits|2 bits| 2 bits |

N4 = Number of cycles prescaler ratio R4 is used and  
 (N2+N3+N4) is modulo-16 addition. (MSB first)  
 CN = Scaling factor for current setting. (MSB first)  
 K = Acceleration factor for integral charge pump. (MSB first)  
 L = Acceleration factor for proportional charge pump.  
 (MSB first)  
 P1,P2 = Number of modulii of prescaler.

No. of modulii	P2	P1
Two	0	0
Three	0	1
Four	1	0

Word C

|1001| NA |  
 | 12 bits | 8 bits free |

NA = Variable frequency for auxiliary synthesiser.  
 (MSB first)

Word D

|1010| NR | SM1,SM2| DM | SA1,SA2| DA|FMOD|LONG|  
 |12 bits| 2 bits | 1 bit | 2 bits | 1 bit| 1 bit | 1 bit |

NR = Reference frequency division value. (MSB first)  
 SM1,SM2 = Main reference source select (Rmain).

SM1	SM2	RMAIN
0	0	M
0	1	2M
1	0	4M
1	1	8M

SA1,SA2 = Auxiliary reference source select (Raux).

SA1	SA2	RAUX
0	0	M
0	1	2M
1	0	4M
1	1	8M

FMOD = Fractional-N modulus select (5 or 8).

FMOD	MODULUS
0	5
1	8

DA = Disable auxiliary synthesiser.

DA=1-disabled  
 DA=0-enabled

DM = Disable main synthesiser.

DM=1-disabled  
 DM=0-enabled

LONG = Word A or A2 select.

LONG=0 Word A selected  
 LONG=1 Word A2 selected

# NJ88C50

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

$V_{dd} = 5V \pm 10\%$ ,  $T_{amb} = -40$  to  $+85^{\circ}C$

#### Static

Parameter	Min	Typ	Max	Unit	Condition
Supply voltage	4.5	5.0	5.5	V	Both synthesisers on (Fia = 125MHz, Fim = 30MHz, Ri = 35MHz) Both synthesisers on (Fia = 10MHz, Fim = 10MHz, Ri = 10MHz) Main on, Auxiliary in stand-by (Fim=30MHz, Ri=35MHz) Main on, Auxiliary in stand-by (Fim=10MHz, Ri =10MHz) Auxiliary on, Main in stand-by (Fia=125MHz, Ri=35MHz) Auxiliary on, Main in stand-by (Fia=10MHz, Ri=10MHz) Main and auxiliary in standby
Supply current		6		mA	
		3	5	mA	
		4		mA	
		2	3	mA	
		4		mA	
		2	3	mA	
		10		$\mu A$	

#### DYNAMIC

### AC Characteristics

$V_{dd} = 5V \pm 10\%$ ,  $T_{amb} = -40$  to  $+85^{\circ}C$

#### Input signals - RF

Parameter	Min	Typ	Max	Unit	Condition
<b>Input-RI</b>					
Reference input - Ri	10		35	MHz	sinewave input, Note 1 pulse input, Note 1
Rise time	1		35	MHz	
Fall time			20	ns	
Input voltage - Ri	0.1		1	$V_{pk-pk}$	Ri = 20-35MHz, Note 1
	0.25		1	$V_{pk-pk}$	Ri = 10-19MHz, Note 1
Input capacitance			10	pF	
Large signal input impedance	200			$k\Omega$	Note 2
Source impedance $Z_s$			1.5	$k\Omega$	Note 3
<b>Aux synthesiser input -FIA</b>					
Input frequency - Fia	20		125	MHz	sinewave input, Note 1 pulse input, Note 1
Rise time	1		125	MHz	
Fall time			10	ns	
Input voltage	0.35		1	$V_{pk-pk}$	Fia = 20-49MHz, Note 1
	0.1		1	$V_{pk-pk}$	Fia = 50-99MHz, Note 1
	0.35		1	$V_{pk-pk}$	Fia = 100-125MHz, Note 1
Input capacitance			10	pF	
Large signal input impedance	200			$k\Omega$	Note 2
Source impedance			1.5	$k\Omega$	Note 3
<b>Main synthesiser input -FIM</b>					
Input frequency - Fim	10		30	MHz	sinewave input pulse input
Rise time	1		30	MHz	
Fall time			50	ns	
Input voltage	0.2		50	ns	
Common mode input DC voltage range	2.8		1	$V_{pk-pk}$	Single ended input
Input capacitance			$V_{dd-1}$	V	
Input impedance			10	pF	
Input Current	100			$M\Omega$	
			10	$\mu A$	

**Notes**

1. Source impedance = 50Ω
2. Virtual earth input amplifier, therefore low impedance for small signals. Impedance is high once signal amplitude exceeds typically ±0.125V.
3. Input amplifier may become unstable for higher values of  $Z_s$ .

**DYNAMIC**

**AC Characteristics**

$V_{dd} = 5V \pm 10\%$ ,  $T_{amb} = -40$  to  $+85^\circ C$

**Input signals - Logic and current defining pins**

Parameter	Min	Typ	Max	Unit	Condition
<b>Data and strobe</b> Input voltage high Input voltage low Input capacitance Input current	$V_{dd}-0.8$ 0		$V_{dd}$ 0.8 10 10	V V pF μA	
<b>Clock</b> Input voltage high Input voltage low Input capacitance Input current Input frequency	$V_{dd}-0.8$ 0		$V_{dd}$ 0.8 10 10 10	V V pF μA MHz	
<b>Current setting pins</b> Input Signal RSA Input current Input Signal RSM Input current Input Signal RSC Input current		80 32 12.8		μA μA μA	Notes 1, 4 Notes 2, 4 Notes 3, 4

**Notes**

1. The current set on pin RSA will be scaled up on chip by a factor of 3 to give the value of the auxiliary phase detector output.
2. The current set on pin RSM will be scaled down on chip by a factor of 32 to provide the current  $I_{bo}$  to the main phase detector which gives the outputs  $I_{prop}$  and  $I_{int}$ .
3. The current set on pin RSC will be scaled down on chip by a factor of 128 to provide the current  $I_{co}$  to the main phase detector which gives the outputs  $I_{comp}$  and  $I_{comp2}$ .
4. The voltage on each of the three current setting pins (RSA, RSM, RSC) is approximately 4V. Therefore to give a typical current of 32μA on RSM for example, a 125kΩ resistor connected between the pin and GND would be required.

## NJ88C50

### DYNAMIC

$V_{dd} = 5V \pm 10\%$ ,  $T_{amb} = -40$  to  $+85^{\circ}C$

#### Output signals

Parameter	Min	Typ	Max	Unit	Condition
<b>Modulus control - MOD1 MOD2</b>					
Output voltage high	$V_{dd}-0.4$		$V_{dd}$	V	Push-Pull output $I_{OH} = 0.5mA$
Output voltage low	0		0.4	V	$I_{OL} = 0.5mA$

#### Modulus output truth table

MOD2	MOD1	Prescaler modulus
0	1	R1
0	0	R2
1	0	R3
1	1	R4

### DYNAMIC

$V_{dd} = 5V$ ,  $T_{amb} = -40$  to  $+85^{\circ}C$

#### Output signals - Auxiliary synthesiser

Parameter	Min	Typ	Max	Unit	Condition
<b>Output signal - PDA</b>					
Up current - See Note 5	-10%	$I_{pda}$	+10%	$\mu A$	$0 < V_{PD} < 4.35V$
Down current - See Note 5	-10%	$I_{pda}$	+10%	$\mu A$	$0.65 < V_{PD} < 5V$
Tristate			10	nA	

### DYNAMIC

$V_{dd} = 5V$ ,  $T_{amb} = -40$  to  $+85^{\circ}C$

#### Output signals - Main synthesiser, proportional output

Parameter	Min	Typ	Max	Unit	Condition
<b>Output signal - PDP</b>					
$I_{prop(0)}$ Up <i>see notes 1, 3 &amp; 4</i>	-10%	$+I_{bo.CN}$	+10%	$\mu A$	$0 < V_{PD} < 4.55V$ , Strobe=0V
$I_{prop(0)}$ Down <i>see notes 1, 3 &amp; 4</i>	-10%	$-I_{bo.CN}$	+10%	$\mu A$	$0.45 < V_{PD} < 5V$ , Strobe=0V
$I_{prop(1)}$ Up <i>see notes 2&amp;3</i>	-10%	$+I_{bo.CN.2L+1}$	+10%	$\mu A$	$0 < V_{PD} < 4.55V$ , Strobe=5V
$I_{prop(1)}$ Down <i>see notes 2&amp;3</i>	-10%	$-I_{bo.CN.2L+1}$	+10%	$\mu A$	$0.45 < V_{PD} < 5V$ , Strobe=5V
Tristate			50	nA	

#### Notes

- The typical value of  $I_{PROP(0)}$  is set by the programmed value of **CN** and the current  $I_{RSM}$  set by the external resistor RSM, where  $I_{bo} = I_{RSM} / 32$ .  $I_{RSM}$  is typically  $32\mu A$ .
- The typical value of  $I_{PROP(1)}$  is set by the value of  $I_{PROP(0)}$  and the programmed value of **L**.
- The current output  $I_{PROP}$  is specified between  $100\mu A$  and  $1mA$ .
- The output current is monotonic over the CN range 128-255. In standard operation CN is set at a value  $> 128$ .
- Where  $I_{pda}$  depends on the value of current setting resistor on RSA pin (9).  $I_{pda} \max = 250\mu A$

**DYNAMIC**

V<sub>dd</sub> = 5V, T<sub>amb</sub> = -40 to +85°C

**Output signals - Main synthesiser, integral output**

Parameter	Min	Typ	Max	Unit	Condition
<b>Output signal - PDI</b>					
I <sub>INT</sub> Up (1mA - 5mA) <i>see notes 1&amp;2</i>	-10%	+I <sub>BO</sub> .CN.2 <sup>L</sup> +1.K	+10%	mA	0<V <sub>PD</sub> <4.45V, Strobe=5V
I <sub>INT</sub> Down (1mA - 5mA) <i>see notes 1&amp;2</i>	-10%	-I <sub>BO</sub> .CN.2 <sup>L</sup> +1.K	+10%	mA	0.35<V <sub>PD</sub> <5V, Strobe=5V
I <sub>INT</sub> Up (5mA - 10mA) <i>see notes 1&amp;2</i>	-10%	+I <sub>BO</sub> .CN.2 <sup>L</sup> +1.K	+10%	mA	0<V <sub>PD</sub> <4.3V, Strobe=5V
I <sub>INT</sub> Down (5mA - 10mA) <i>see notes 1&amp;2</i>	-10%	-I <sub>BO</sub> .CN.2 <sup>L</sup> +1.K	+10%	mA	0.5<V <sub>PD</sub> <5V, Strobe=5V
Tristate			50	nA	

**Notes**

1. The typical value of *I<sub>INT</sub>* is set by the value of *I<sub>PROP</sub>(1)* and the programmed value of *K*.
2. The current output *I<sub>INT</sub>* is specified between 1mA and 10mA.

**DYNAMIC**

V<sub>dd</sub> = 5V, T<sub>amb</sub> = -40 to +85°C

**Output signals - Main synthesiser, under Fractional-N control**

Parameter	Min	Typ	Max	Unit	Condition
<b>Output signal - PDP</b>					
I <sub>COMP</sub> (0) <i>see notes 1&amp;3</i>	-10%	I <sub>CO</sub> .Acc.	+10%	µA	0<V <sub>PD</sub> <4.55V, Strobe=0V
I <sub>COMP</sub> (1) <i>see notes 2&amp;3</i>	-10%	I <sub>CO</sub> .Acc.2 <sup>L</sup> +1.	+10%	µA	0<V <sub>PD</sub> <4.55V, Strobe=5V
<b>Output signal - PDI</b>					
I <sub>COMP</sub> 2 <i>see notes 4&amp;5</i>	-10%	I <sub>CO</sub> .Acc.2 <sup>L</sup> +1.K	+10%	µA	0<V <sub>PD</sub> <4.55V, Strobe=5V

**Notes**

1. The typical value of *I<sub>COMP</sub>(0)* is set by the fractional-N accumulator value *Acc* and the current *I<sub>RSC</sub>* set by the external resistor *RSC*, where *I<sub>CO</sub>*=*I<sub>RSC</sub>*/128. *I<sub>RSC</sub>* is typically 12.8µA.
2. The typical value of *I<sub>COMP</sub>(1)* is set by the value of *I<sub>COMP</sub>(0)* and the programmed value of *L*.
3. The current output *I<sub>COMP</sub>* is specified up to 12µA.
4. The typical value of *I<sub>COMP</sub>2* is set by the value of *I<sub>COMP</sub>(1)* and the programmed value of *K*.
5. The current output *I<sub>COMP</sub>2* is specified up to 180µA.

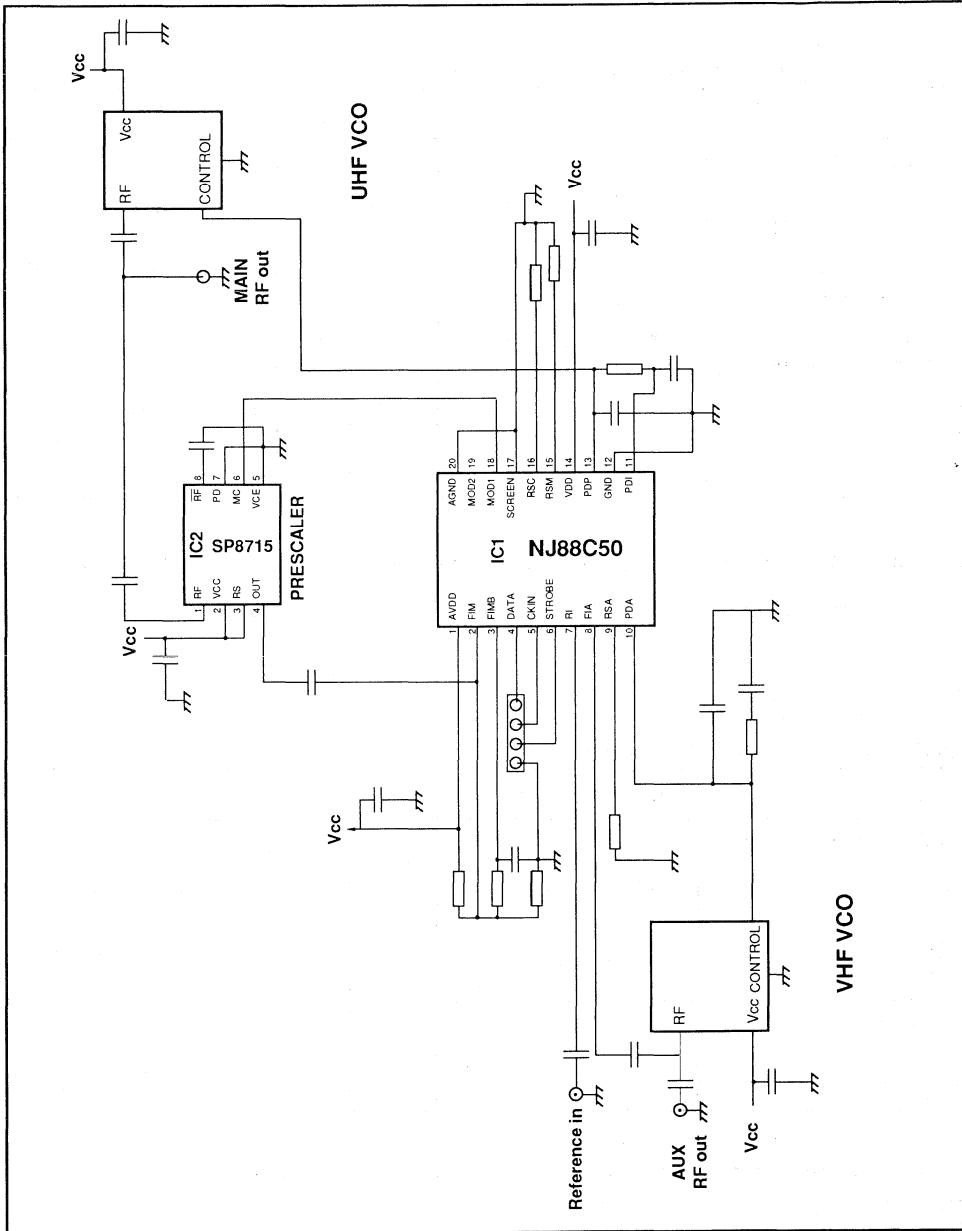


Fig. 8 Typical application

Fig.8 shows a typical application, using the NJ88C50 to generate both VHF and UHF signals. External components are kept to a minimum, requiring only bias, loop filter and decoupling components. In many applications the UHF VCO is a pre-assembled and tested module to suit the end equipment use, whereas the VHF design is likely to be discrete. The circuit shown is suitable for operation up to 1.1GHz and uses

a low power prescaler, the SP8715, feeding the NJ88C50 in single ended mode. This requires a biasing network around the differential input of the NJ88C50 to be used (pins 2 and 3).

Power supply and ground rails must have adequate decoupling otherwise overall performance may be impaired.

# Section 2

## IF Products









# SL6601C

## FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz; there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

### FEATURES

- High Sensitivity 2 $\mu$ V Typical
- Low Power: 2.3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

### APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

### QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

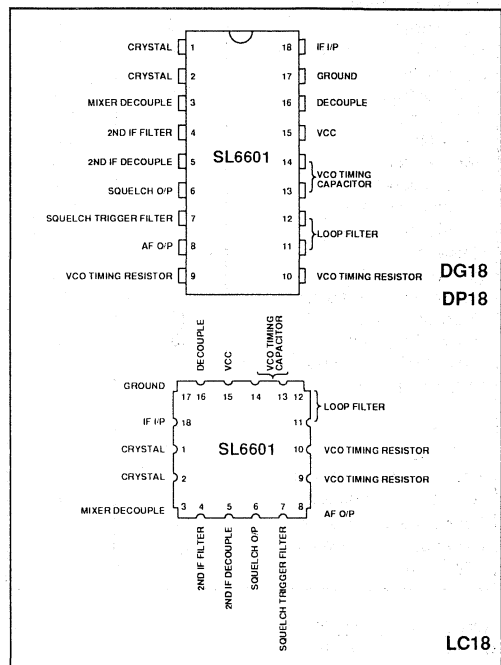


Fig. 1 Pin connections - top view

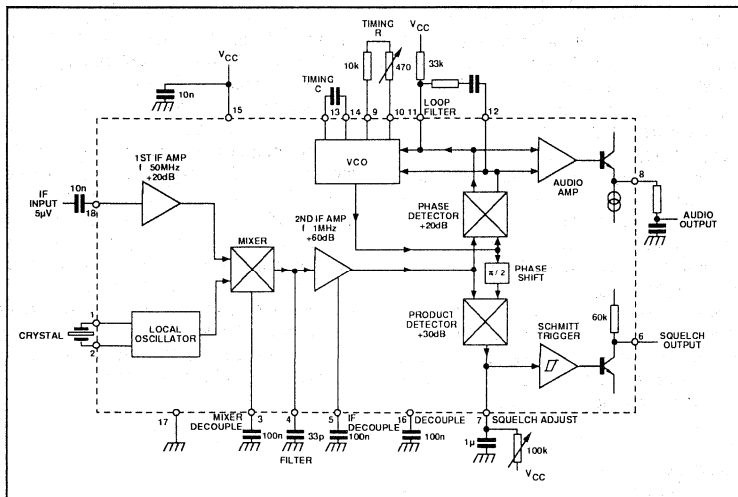


Fig. 2 SL6601C block diagram

## SL6601C

### ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage  $V_{cc}$ : 7V

Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a  $\pm 2.5$ kHz frequency deviation

Ambient temperature:  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ; IF = 100kHz; AF bandwidth = 15kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	$\Omega$	Source impedance = 200 $\Omega$
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		$\mu\text{V rms}$	At pin 18 for S + N/N = 20dB
Audio output	30	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100 $\mu\text{V rms}$ input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20 $\mu\text{V rms}$ input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3 $\mu\text{V}$ input at pin 18
Noise figure		6		dB	50 $\Omega$ source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		$\mu\text{V rms}$	Pin 18 to pin 4, 1dB compression
Squelch output load	250			k $\Omega$	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input 390pF timing capacitor 390pF timing capacitor
Grade 2	95		110	kHz	
Grade 3	105		120	kHz	
Source impedance (pin 4)		25	40	k $\Omega$	
AF output impedance		4	10	k $\Omega$	
Lock-in dynamic range	$\pm 8$			kHz	20 $\mu\text{V}$ to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	$\Omega$	10.8MHz

## APPLICATION NOTES

### IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IFs; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01 $\mu\text{F}$  capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

### Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external

capacitor equal to  $(40 \pm 7)/f$  pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins: a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

### VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601 C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1	85 - 100kHz (or uncoded)
/2	95 - 110kHz
/3	105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

### Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO: when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 101F can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 518dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig. 4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended

### Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

### Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

## LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choice of  $f_n$ , the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio  $f_m/f_n$  highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_{eIN}}{\Delta f}$$

can be established for the desired damping factor.

$\Phi_e$  - peak phase error  
 $f_n$  - loop natural frequency  
 $\Delta f$  - maximum deviation of the input signal

and as  $f_n$  and  $\Delta f$  are known,  $\Phi_e$  is easily calculated. Values for  $\Phi_e$  should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at  $\pm\pi/2$  radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of  $\Phi_e$  achieved is far removed from this value, a new value of  $f_n$  should be chosen and the process repeated.

With  $f_n$  and  $D$  established, the time constants are derived from

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$K_o K_D$  is  $0.3f_o$ , where  $f_o$  is the operating frequency of the VCO.  $t_1$  is fixed by the capacitor and an internal 20kΩ resistor:  $t_2$  is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t_2 \times 20 \times 10^3}{2C \times 10^3}$$

In order that standard values may be used, it is better to establish a value of  $C$  and use the next lowest standard value e.g.  $C_{calc} = 238\text{pF}$ , use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of  $R_{ext}$  is then 'rounded up' by a similar process. It is, however, better to increase  $R_{ext}$  to the nearest preferred value as loop bandwidth is proportional  $(R_{ext})^{1/2}$  while damping factor is proportional to  $R$ : thus damping factor is increasing more quickly which gives a more level response.

## SL6601C

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let  $f_n = 6\text{kHz}$  and  $D = 0.5$

Then from the graph

$$\frac{\Phi_{\text{effN}}}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase  $f_n$  e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \frac{\Phi_{\text{effN}}}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set  $f_n = 7.5\text{kHz}$

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_{\text{effN}}}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$K_o K_D = 0.3f_o$  where  $f_o$  is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu\text{s}$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu\text{s}$$

$$t_1 = 22.5\mu\text{s}$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4\text{k}\Omega \text{ (use 3.9k}\Omega\text{)}$$

Actual loop parameters can now be recalculated

$$t_1 = 20\mu\text{s} \quad t_2 = 3.9\mu\text{s}$$

$$2\pi f_n = \frac{(K_o K_D)}{(t_1 \times t_2)} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} = 7.97\text{kHz}$$

$$D = f_n(t_2 + \frac{1}{K_o K_D}) = 0.515$$

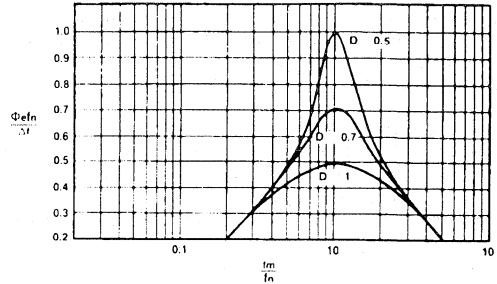


Fig. 3 Damping factor

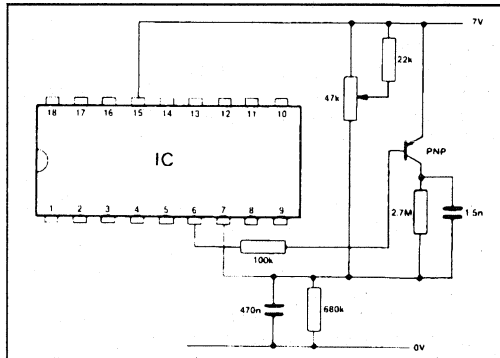


Fig. 4 Using an external PNP in squelch circuit

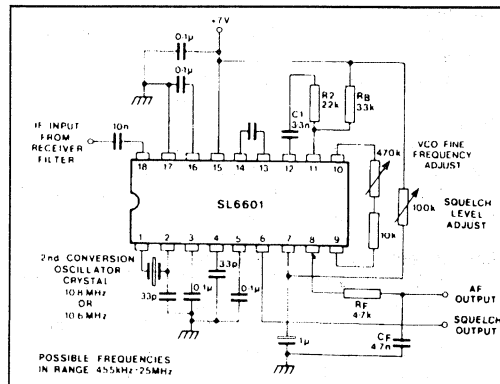


Fig. 5 SL6601 application diagram  
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

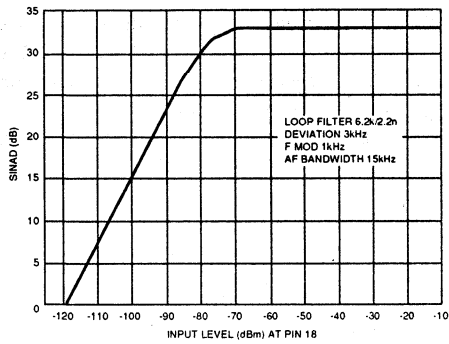


Fig. 6 Typical SINAD (signal + noise + distortion/noise + distortion)

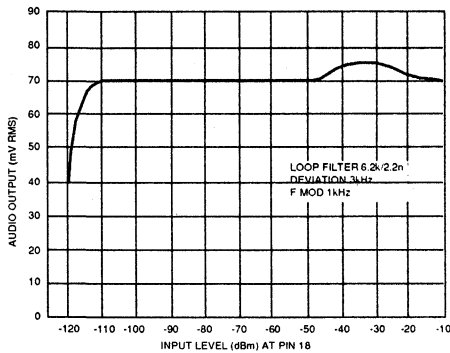


Fig. 7 Typical recovered audio v. input level (3kHz deviation)

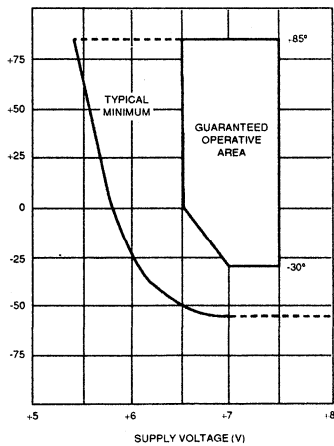


Fig. 8 Supply voltage v. temperature

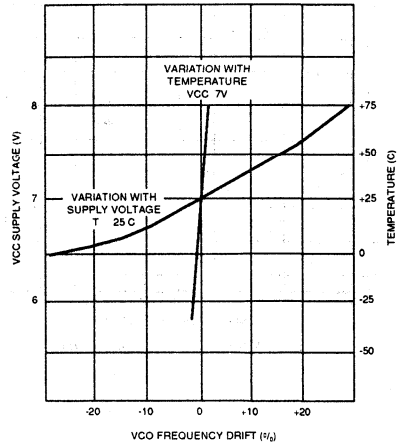


Fig. 9 Typical VCO characteristics

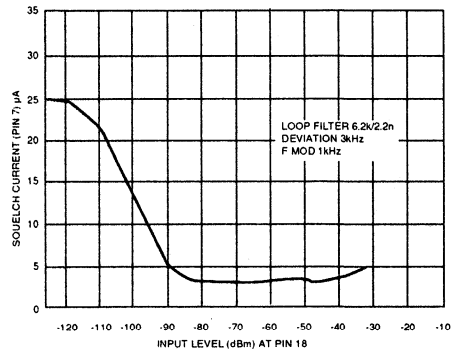


Fig. 10 Typical squelch current v. input level

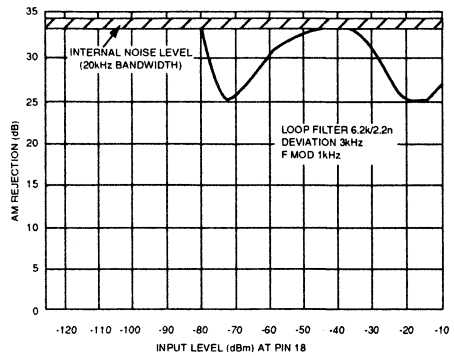


Fig. 11 Typical AM rejection

(the ratio between the audio output produced by:  
 (a) a 3kHz deviation 1kHz modulation FM signal and  
 (b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

# SL6601C

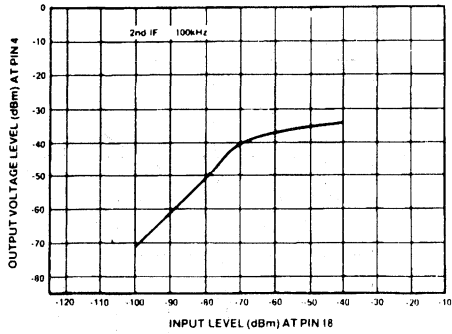


Fig. 12 Typical conversion gain (to pin 4)

## ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55°C to +125°C (DP package) -55°C to +150°C (DG)
Operating temperature (see Electrical Characteristics)	-55°C to +125°C
Input voltage	1V RMS at pin 18



# SL6652

## LOWER POWER IF/AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

### FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

### APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

### QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3µV
- Co-Channel Rejection 7dB

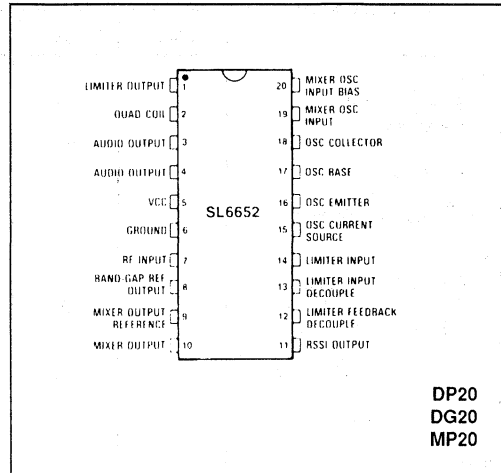


Fig. 1 Pin connections (top view)

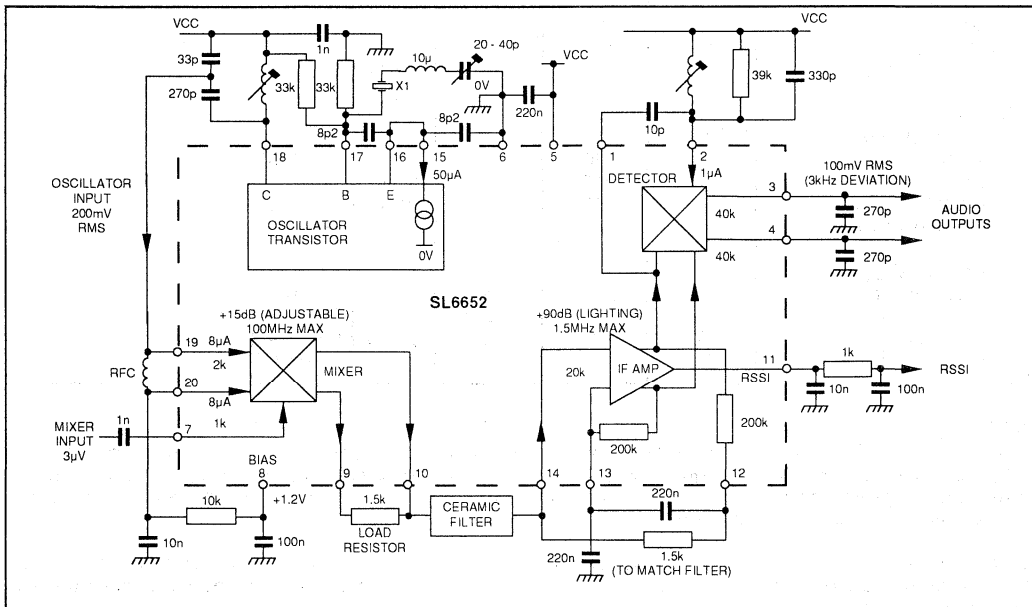


Fig. 2 block diagram

**SL6652**  
**ABSOLUTE MAXIMUM RATINGS**

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):

$V_{cc} = 2.5V$  to  $7.5V$ ,  $T_{amb} = -30°C$  to  $+85°C$ ,  $IF = 455kHz$ ,  $RF = 50MHz$ , Quad Coil Working  $Q = 30$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
<b>Overall</b>					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	$\mu V$	20dB SINAD
		3		$\mu V$	12dB SINAD
AM rejection		40		dB	RF input <500 $\mu V$
$V_{bias}$	1.0	1.2	1.4	V	$T_{amb} = 25°C$
Co-channel rejection		7		dB	See Note 2
<b>Mixer</b>					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		$\mu A$	At $V_{bias}$
Mixer gain		15		dB	Load = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
<b>Oscillator</b>					
Current sink	40		70	$\mu A$	$T_{amb} = 25°C$
$H_{fe}$	30				40 ... 70 $\mu A$
$f_T$		500		MHz	40 ... 70 $\mu A$
<b>IF Amplifier</b>					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
<b>Detector</b>					
Audio output level	75		125	mV	} 5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
<b>RSSI Output (<math>T_{amb} = +25°C</math>)</b>					
Output current			20	$\mu A$	No input pin 14
Output current	50		80	$\mu A$	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	$\mu A/dB$	See Note 1
Linear dynamic range	70			dB	See Note 1

**NOTES**

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1 kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.



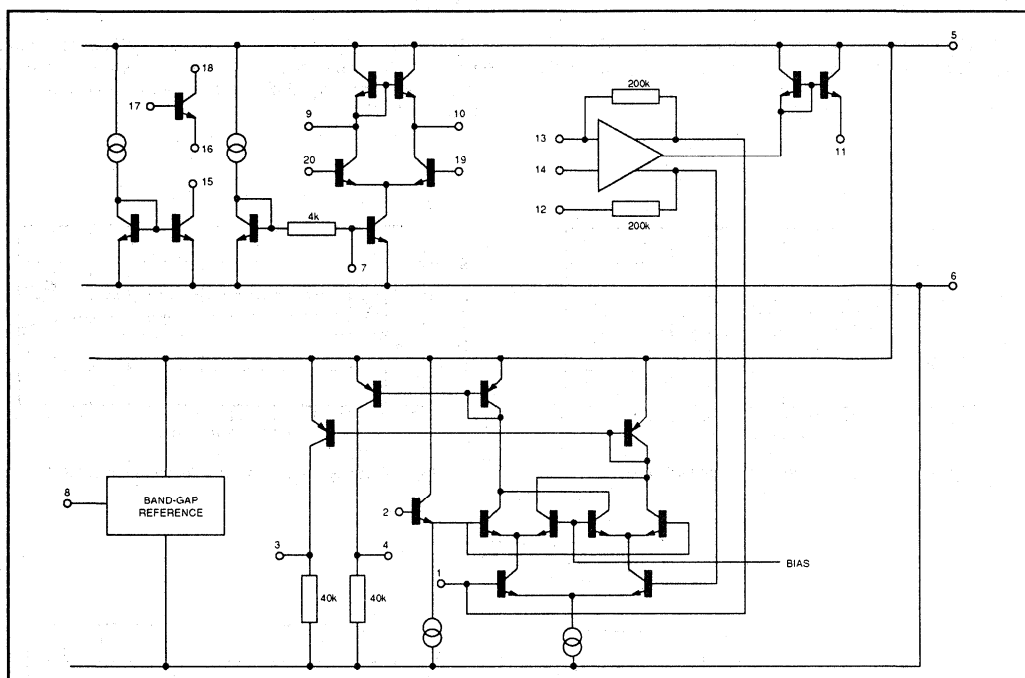


Fig. 3 Internal schematic

## GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

### Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically  $300\mu\text{A}$ . The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

### Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design

of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

### IF amplifier

The limiting amplifier is capable of operation to at least 1 MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

### Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

### RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

# SL6652

## Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

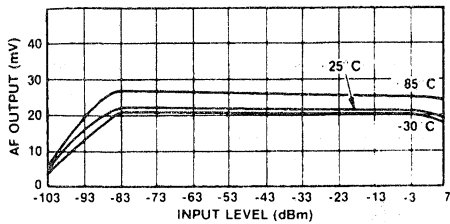


Fig. 4 Audio output vs input and temperature at 2.5V

## Detector

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

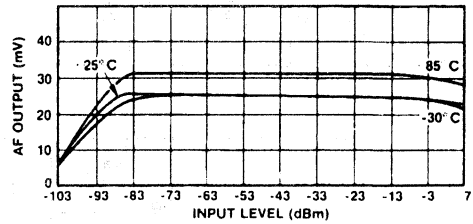


Fig. 5 Audio output vs input and temperature at 5.0V

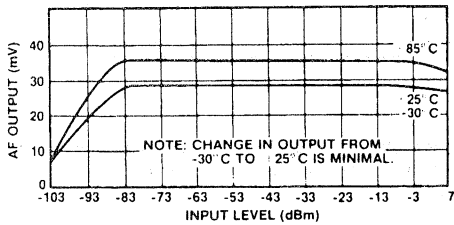


Fig. 6 Audio output vs input and temperature at +7.5V

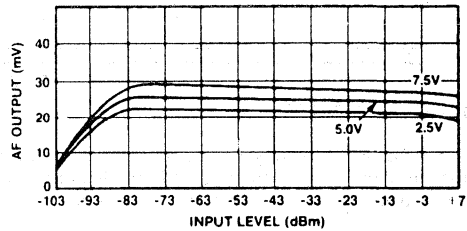


Fig. 7 Audio output vs input and supply voltage at +25°C

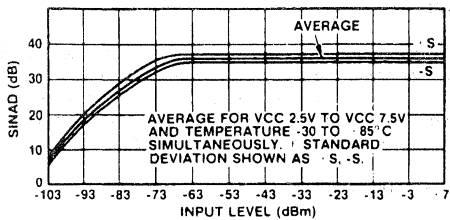


Fig. 8 SINAD and input level

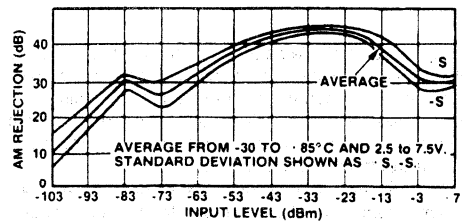


Fig. 9 AM rejection and input level

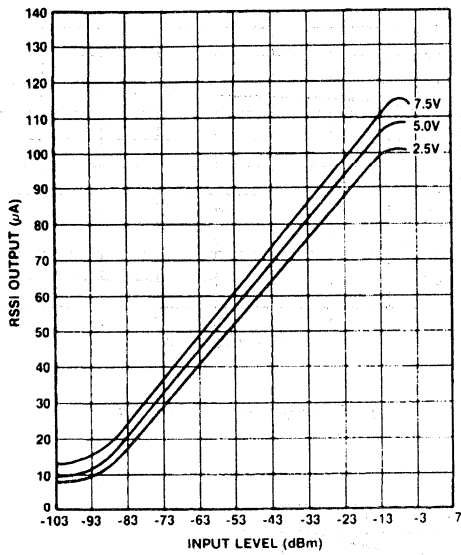


Fig. 10 RSSI output vs input and supply voltage  
( $T_{amb} = 20^{\circ}\text{C}$ )

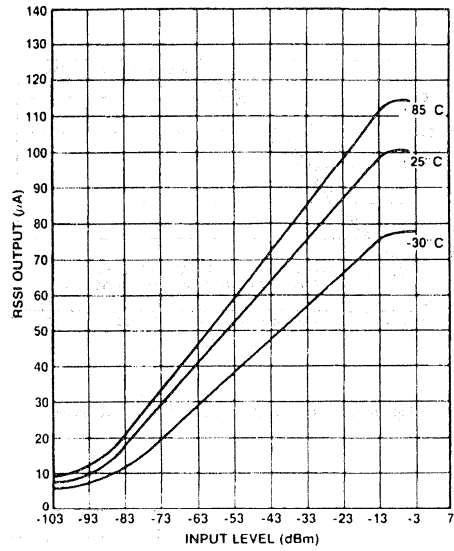


Fig. 11 RSSI output vs input level and temperature  
( $V_{cc} = 2.5\text{V}$ )

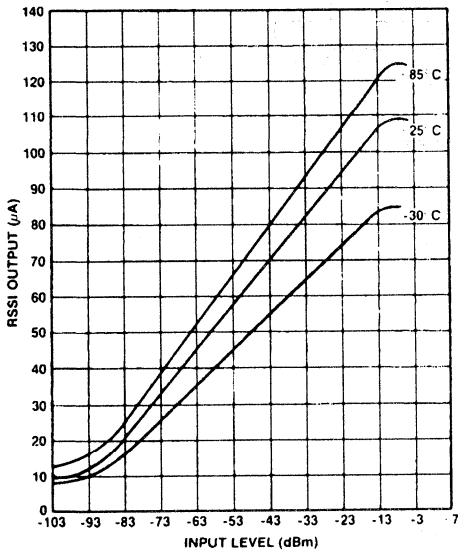


Fig. 12 RSSI output vs input level and temperature  
( $V_{cc} = 5\text{V}$ )

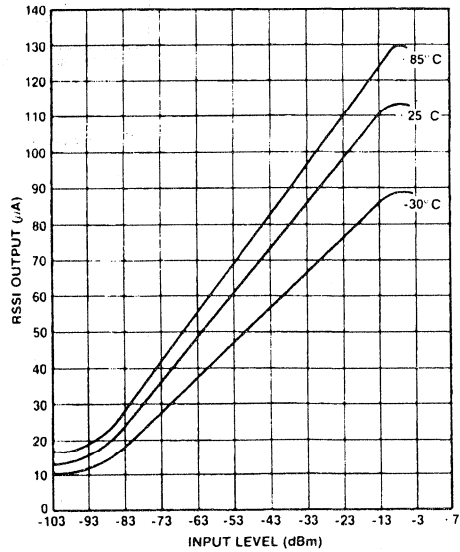


Fig. 13 RSSI output vs input level and temperature  
( $V_{cc} = 7.5\text{V}$ )

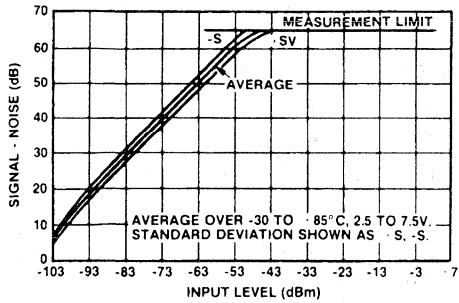


Fig. 14 Signal + noise to noise ratio vs input level

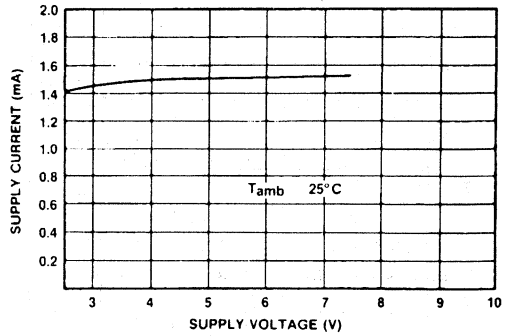


Fig. 15 Supply current vs supply voltage

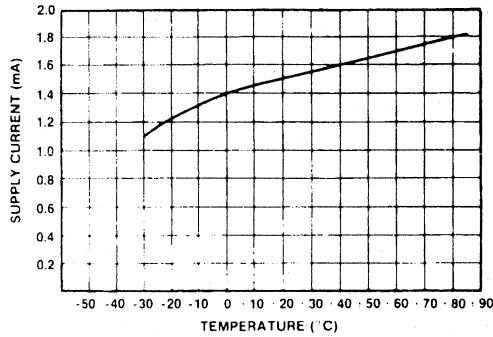
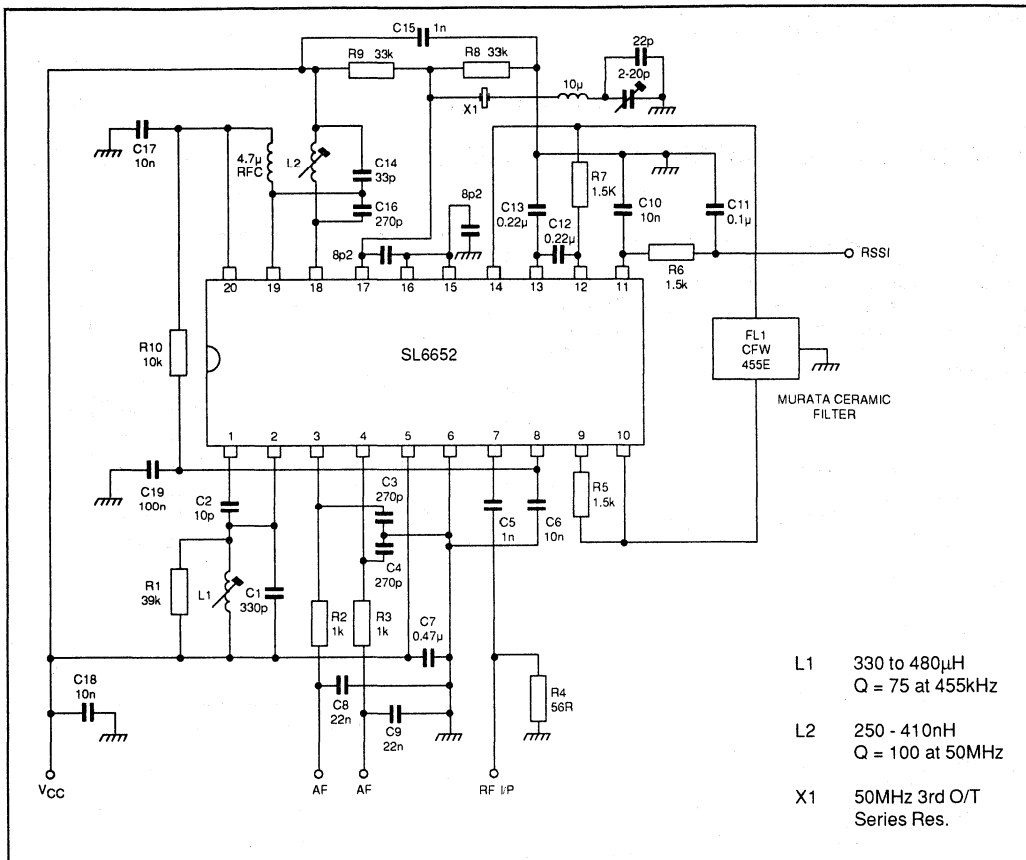


Fig. 16 Supply current vs temperature ( $V_{cc} = 5V$ )



- L1 330 to 480μH  
Q = 75 at 455kHz
- L2 250 - 410nH  
Q = 100 at 50MHz
- X1 50MHz 3rd O/T  
Series Res.

Fig. 17 Circuit diagram of SL6652 application circuit



# SL6654

## LOWER POWER IF/AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6654 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

### FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

### APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

### QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3µV
- Co-Channel Rejection 7dB

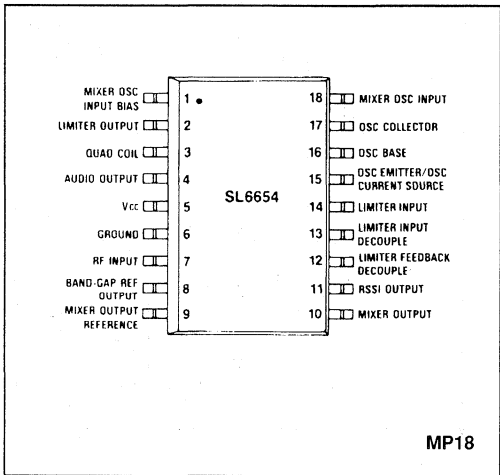


Fig. 1 Pin connections (top view)

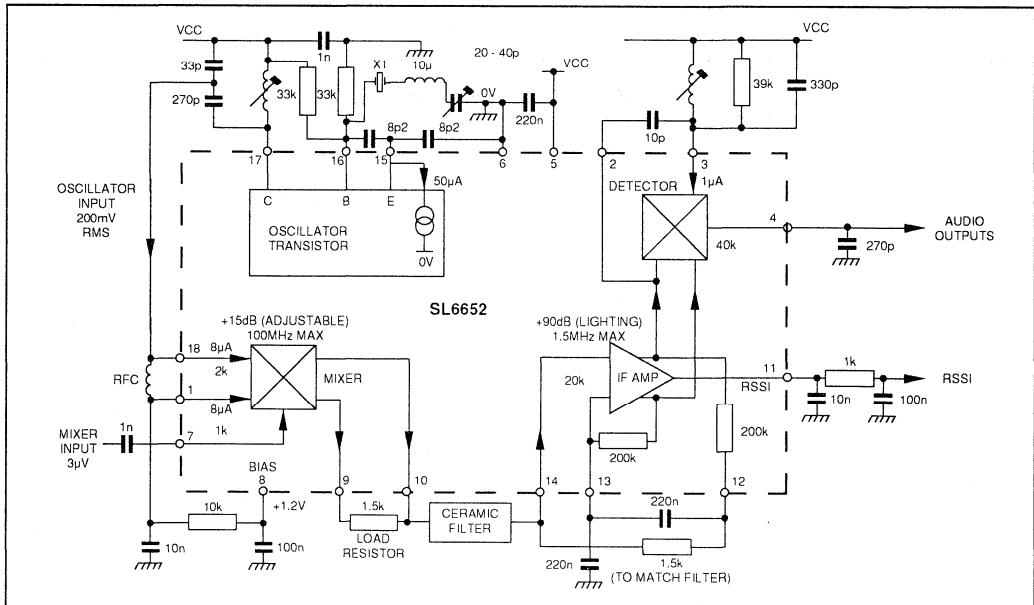


Fig. 2 block diagram

## ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

 $V_{CC} = 2.5V$  to  $7.5V$ ,  $T_{amb} = -30^{\circ}C$  to  $+85^{\circ}C$ ,  $IF = 455kHz$ ,  $RF = 50MHz$ , Quad Coil Working  $Q = 30$ 

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
<b>Overall</b>					
Supply current		1.5	20	mA	
Sensitivity		5	10	$\mu V$	20dB SINAD
		3		$\mu V$	12dB SINAD
AM rejection		40		dB	RF input <500 $\mu V$
$V_{bias}$	1.0	1.2	1.4	V	$T_{amb} = 25^{\circ}C$
Co-channel rejection		7		dB	See Note 2
<b>Mixer</b>					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		$\mu A$	At $V_{bias}$
Mixer gain		15		dB	$R_{load} = 1.5k$
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
<b>Oscillator</b>					
Current sink	40		70	$\mu A$	$T_{amb} = 25^{\circ}C$
$H_{fe}$	30				40 ... 70 $\mu A$
$f_T$		500		MHz	40 ... 70 $\mu A$
<b>IF Amplifier</b>					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
<b>Detector</b>					
Audio output level	75		125	mV	} 5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
<b>RSSI Output (<math>T_{amb} = +25^{\circ}C</math>)</b>					
Output current			20	$\mu A$	No input pin 14
Output current	50		80	$\mu A$	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	$\mu A/dB$	See Note 1
Linear dynamic range	70			dB	See Note 1

## NOTES

1. The RSSI output is 100% dynamically tested at 5V and  $+20^{\circ}C$  over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1 kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

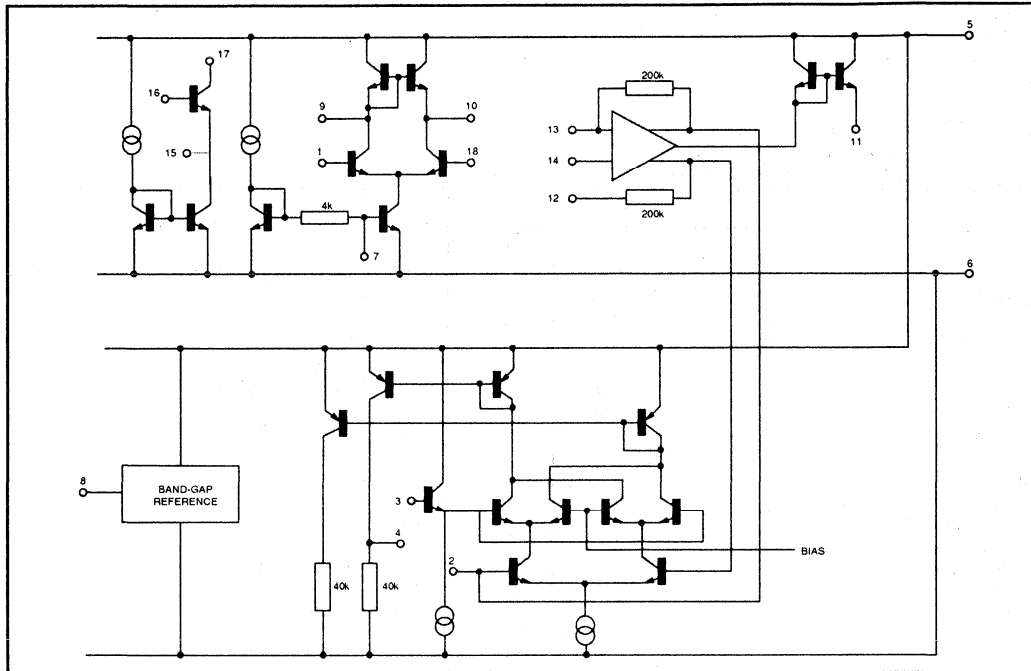


Fig. 3 Internal schematic

## GENERAL DESCRIPTION

The SL6654 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

### Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300 $\mu$ A. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

### Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design

of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

### IF amplifier

The limiting amplifier is capable of operation to at least 1 MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

### Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

### RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.



### Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

### Detector

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

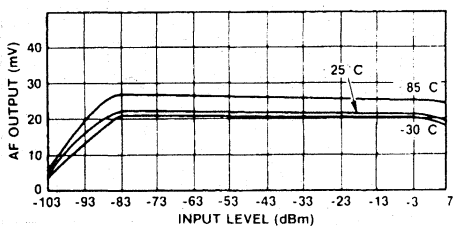


Fig. 4 Audio output vs input and temperature at 2.5V

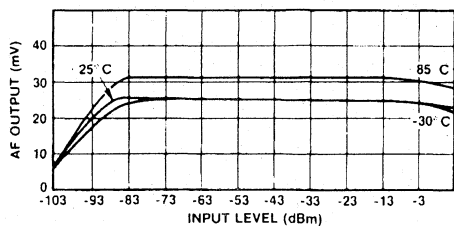


Fig. 5 Audio output vs input and temperature at 5.0V

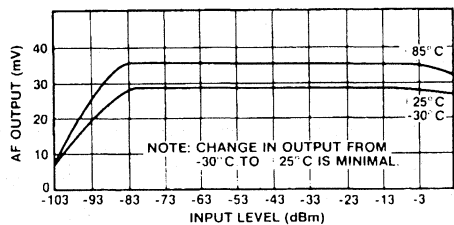


Fig. 6 Audio output vs input and temperature at +7.5V

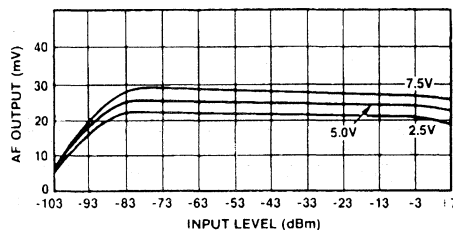


Fig. 7 Audio output vs input and supply voltage at +25°C

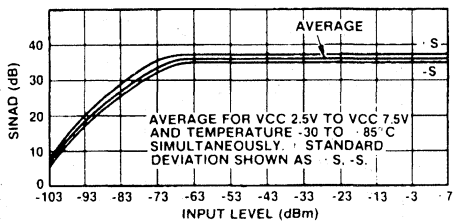


Fig. 8 SINAD and input level

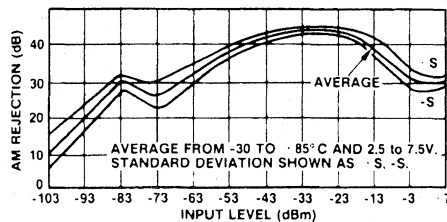


Fig. 9 AM rejection and input level

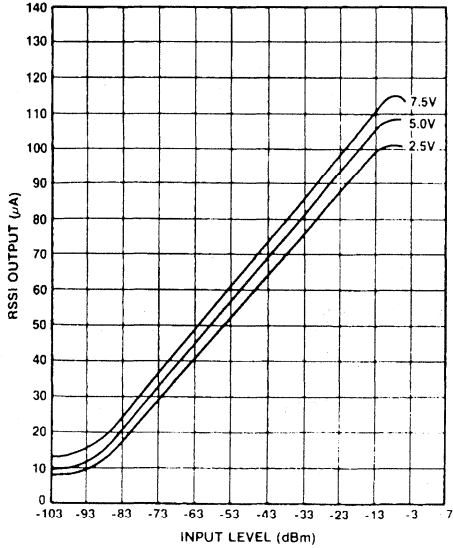


Fig. 10 RSSI output vs input and supply voltage  
( $T_{amb} = 20^{\circ}\text{C}$ )

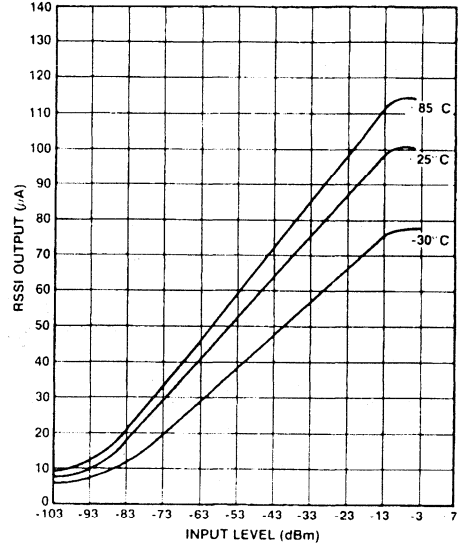


Fig. 11 RSSI output vs input level and temperature  
( $V_{cc} = 2.5\text{V}$ )

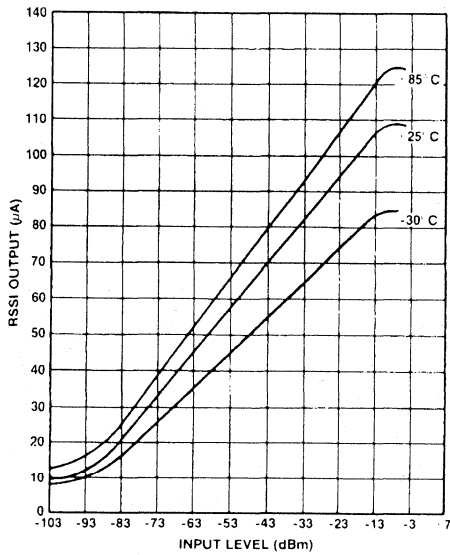


Fig. 12 RSSI output vs input level and temperature  
( $T_{cc} = 5\text{V}$ )

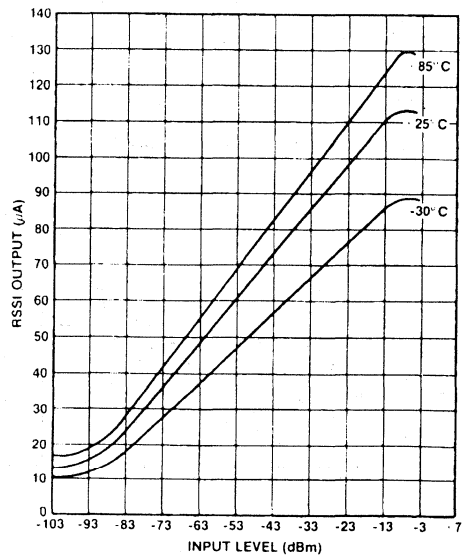


Fig. 13 RSSI output vs input level and temperature  
( $V_{cc} = 7.5\text{V}$ )

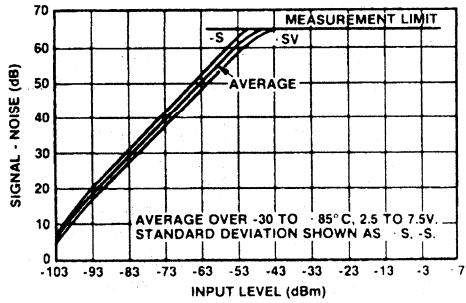


Fig. 14 Signal + noise to noise ratio vs input level

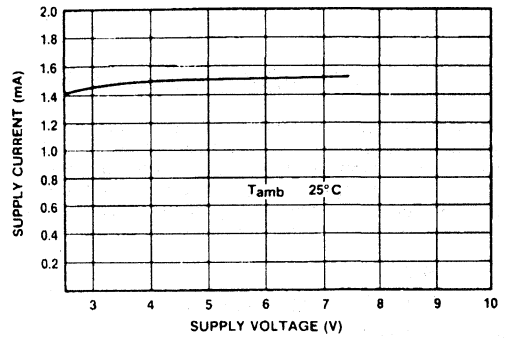


Fig. 15 Supply current vs supply voltage

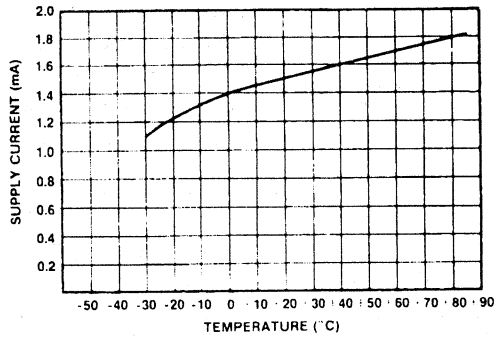


Fig. 16 Supply current vs temperature ( $V_{CC} = 5V$ )

# SL6659

## LOW POWER IF/AF CIRCUIT (WITH RSSI) FOR FM RADIO

The SL6659 is a complete single chip mixer, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

### FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 200MHz Operation
- Exceptionally Stable RSSI

### APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

### ORDERING INFORMATION

SL6659 NA MP – Miniature plastic DIL package  
SL6659 NA MPTD - As above, supplied on tape and reel

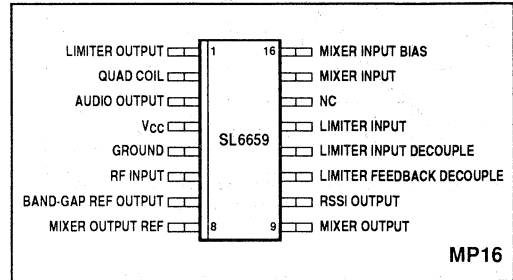


Fig. 1 Pin connections – top view

### QUICK REFERENCE DATA

- Supply Voltage: 2.5V to 7.5V
- Sensitivity: 3µV
- Co-channel Rejection: 7dB

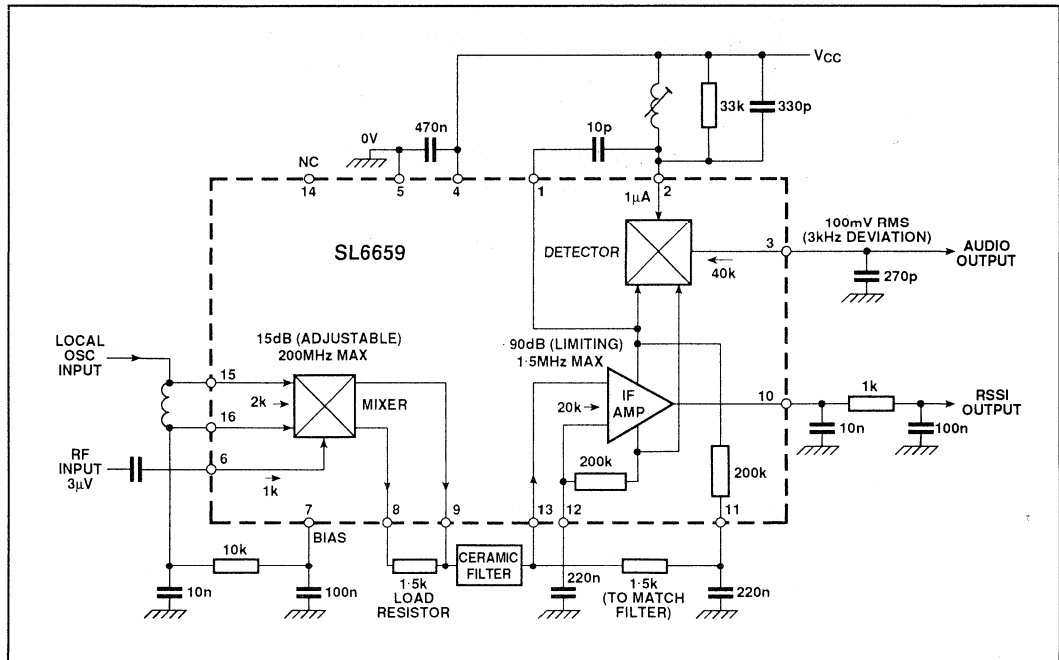


Fig. 2 Block diagram

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage	8V
Storage temperature	-55°C to +150°C
Mixer input	1V <sub>rms</sub>

NOTE: This device has static sensitive inputs, sensitivity typically measured as 500V using MIL-STD-883 method 3015. Therefore, ESD handling precautions are essential to avoid degradation of performance or permanent damage of this device.

**ELECTRICAL CHARACTERISTICS**

The characteristics are guaranteed over the following conditions, unless otherwise stated:

$$V_{CC} = 2.5V \text{ to } 7.5V, T_{AMB} = -30^{\circ}C \text{ to } +85^{\circ}C, IF = 455kHz, RF = 50MHz, \text{ Quad Coil working } Q = 30$$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
<b>Overall</b>					
Supply current		1.5	2.0	mA	20dB SINAD 12dB SINAD RF input <500μV T <sub>AMB</sub> = 25°C See Note 2
Sensitivity		5		μV	
		3		μV	
AM rejection		40		dB	
V <sub>BIAS</sub>	1.0	1.2	1.4	V	
Co-channel rejection		7		dB	
<b>Mixer</b>					
RF input impedance		1		kΩ	At V <sub>BIAS</sub> R <sub>LOAD</sub> = 1.5kΩ
LO input impedance		2		kΩ	
LO input bias		5		μA	
Mixer gain		15		dB	
3rd order input intercept		-10		dBm	
LO input level	180		300	mV	
LO frequency	200			MHz	
<b>IF Amplifier</b>					
Gain		90		dB	
Frequency	455	1500		kHz	
Differential input impedance		20		kΩ	
<b>Detector</b>					
Audio output level	75		125	mV	} 5mV into pin 13
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kΩ	
<b>RSSI Output (T<sub>AMB</sub> = +25°C)</b>					
Output current			25	μA	No input pin13 Pin 13 = 2.5mV
	50		80	μA	
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

**NOTES**

- The RSSI output is 100% dynamically tested at 5V and +20°C over a 70dB range. First the input to pin 13 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30db, the current is measured. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.
- Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

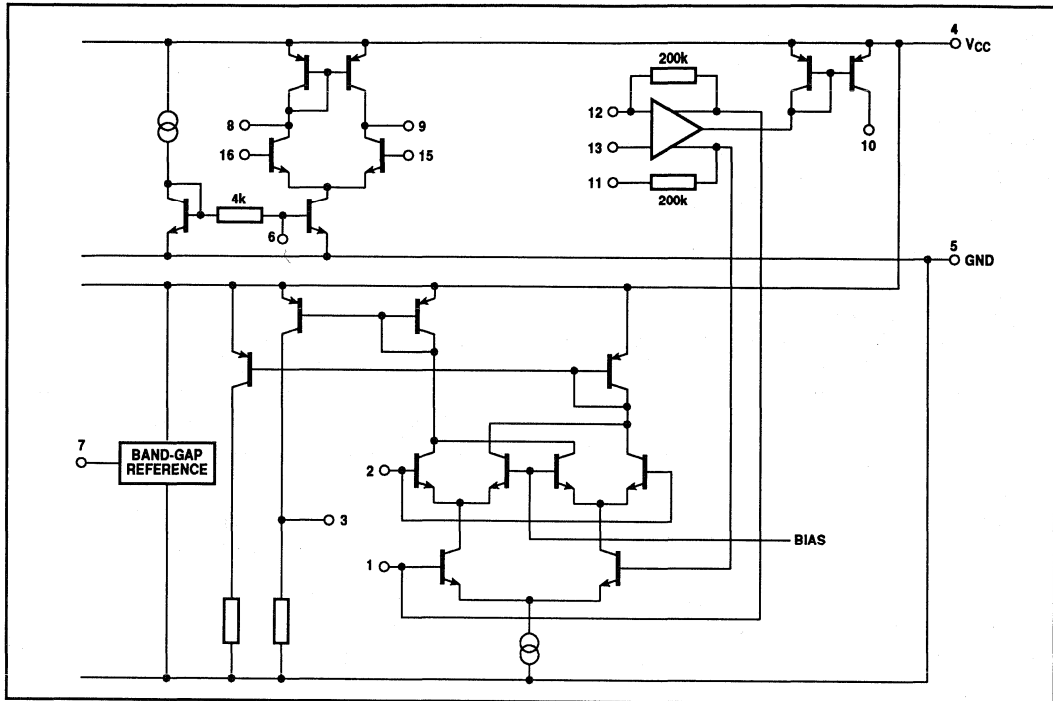


Fig. 3 Internal schematic

## GENERAL DESCRIPTION

The SL6659 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 200MHz
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output
- An RSSI (Received Signal Strength Indicator) output

### Mixer

The Mixer is single balanced with an active load. Gain is set externally by the load resistor, although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300 $\mu$ A. The LO input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the local oscillator input.

### IF Amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the

ceramic filter. Because of the high gain, pins 11 and 12 must be adequately bypassed.

### Detector

A conventional quadrature detector providing audio output is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

### RSSI Output

The RSSI output is a current source with value proportional to the logarithm of the IF signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

### Supply Voltage

The SL6659 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

### Internal Bias Voltage

The internal band-gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 $\Omega$ .

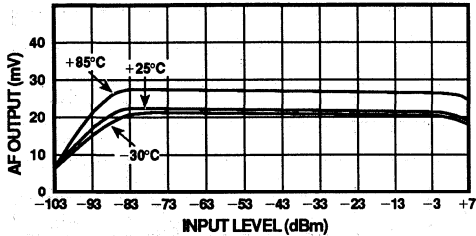


Fig. 4 Audio output v. input and temperature at 2.5V

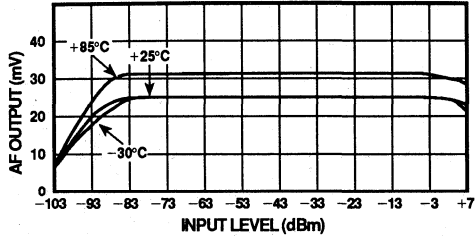


Fig. 5 Audio output v. input and temperature at 5.0V

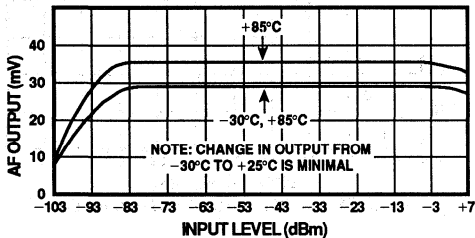


Fig. 6 Audio output v. input and temperature at 7.5V

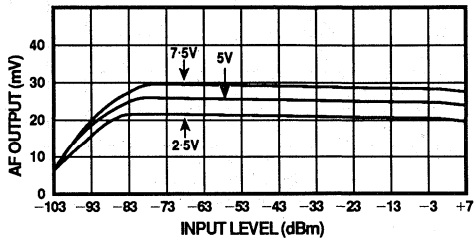


Fig. 7 Audio output v. input and supply voltage at +25°C

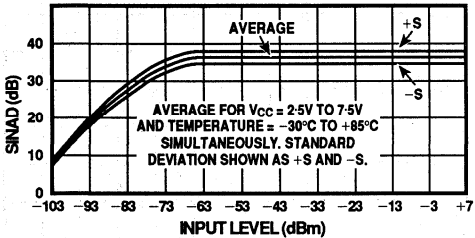


Fig. 8 SINAD v. input level

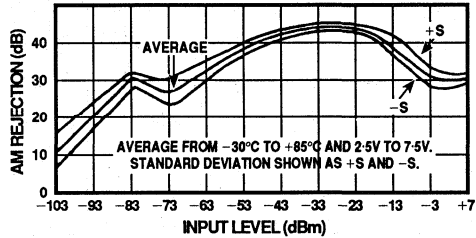


Fig. 9 AM rejection and input level

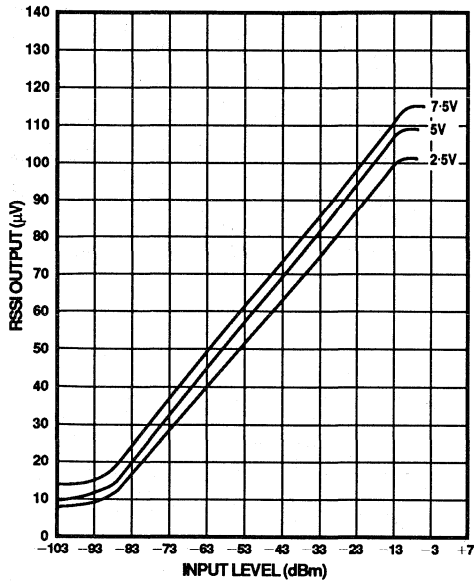


Fig. 10 RSSI output v. input and supply voltage  
( $T_{AMB} = 20^{\circ}C$ )

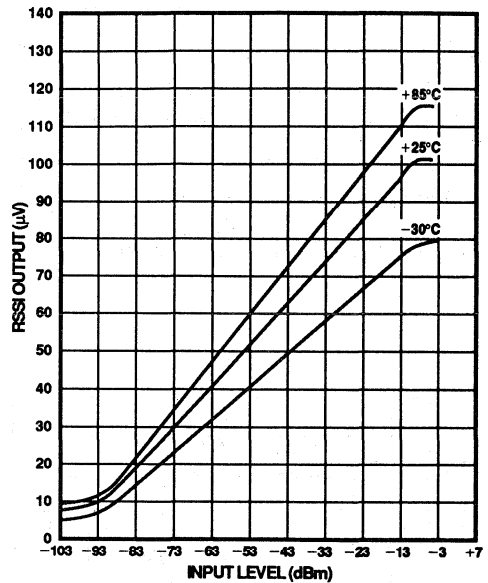


Fig. 11 RSSI output v. input and temperature  
( $V_{CC} = 2.5V$ )

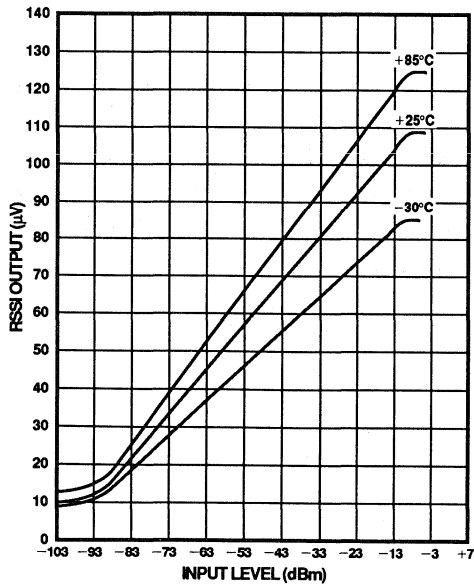


Fig. 12 RSSI output v. input level and temperature  
( $V_{CC} = 5V$ )

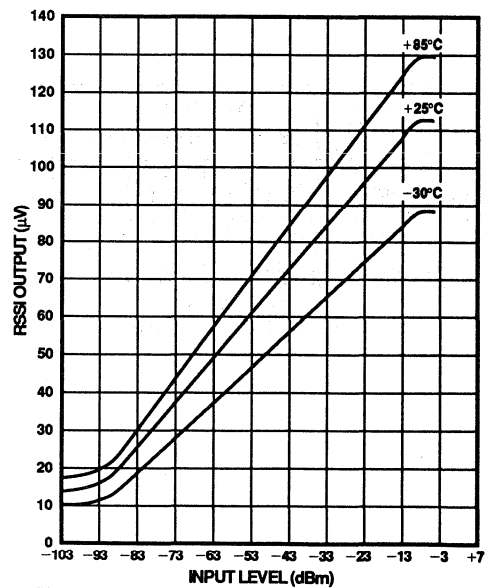


Fig. 13 RSSI output v. input level and temperature  
( $V_{CC} = 7.5V$ )



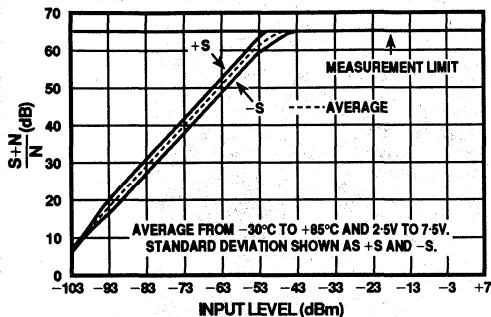


Fig. 14 (Signal+ noise) to noise ratio v. input level

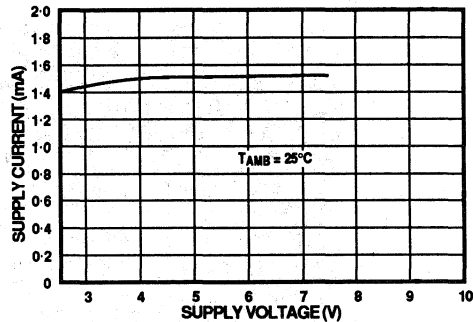


Fig. 15 Supply current v. supply voltage

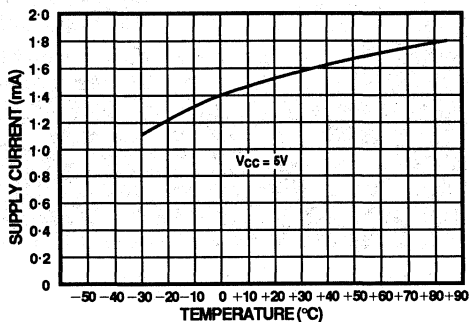


Fig. 16 Supply current v. temperature

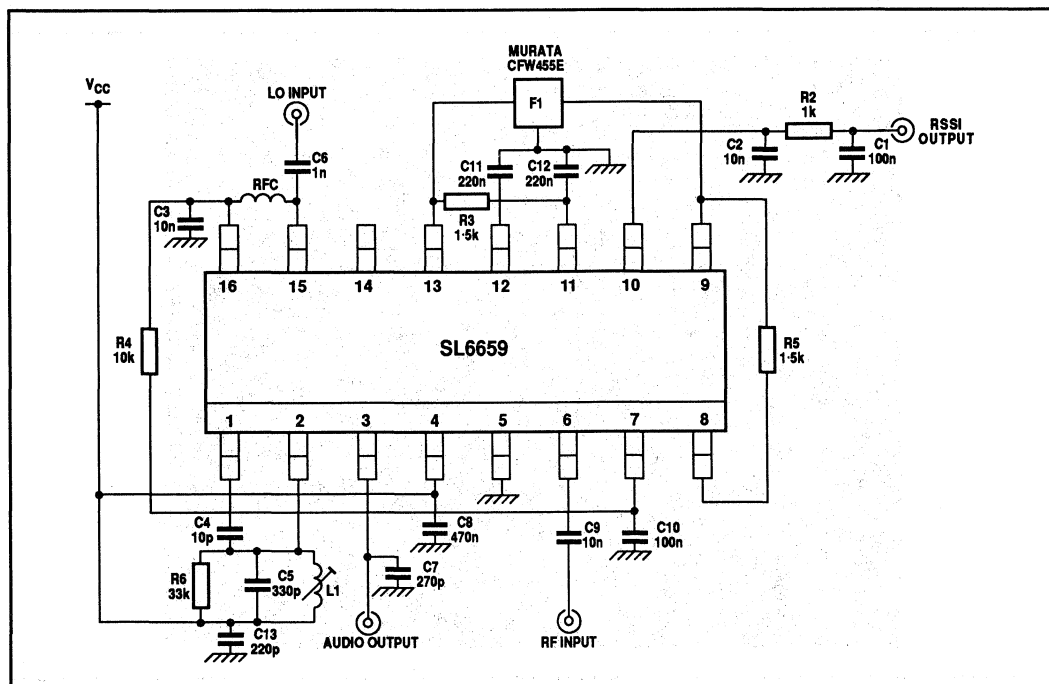


Fig. 17 Circuit diagram of SL6659 demonstration board

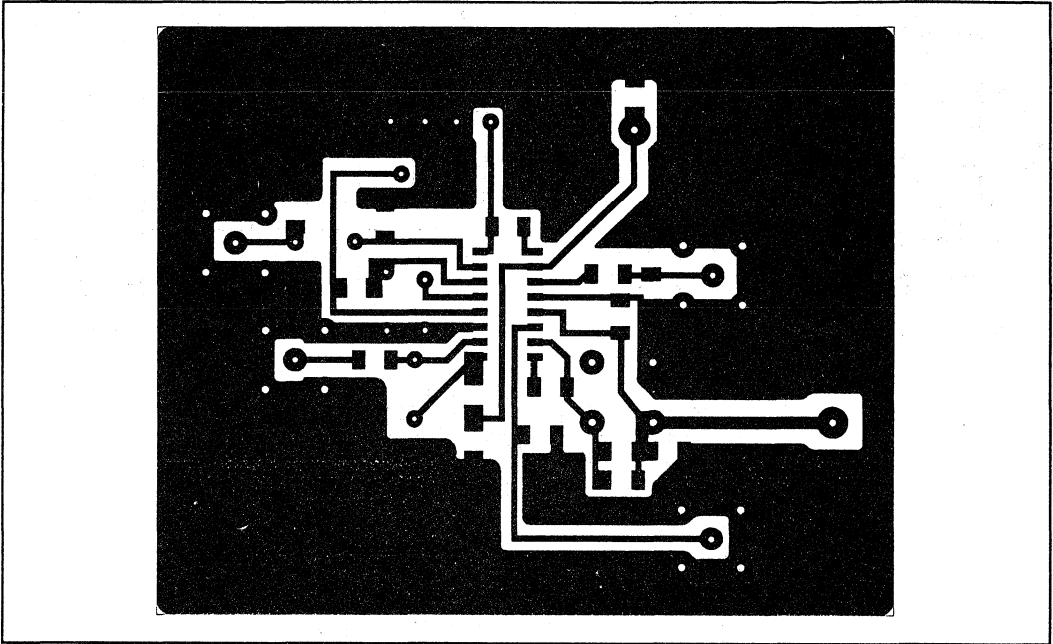


Fig. 18 Track side of demonstration board. Scale = 2:1.

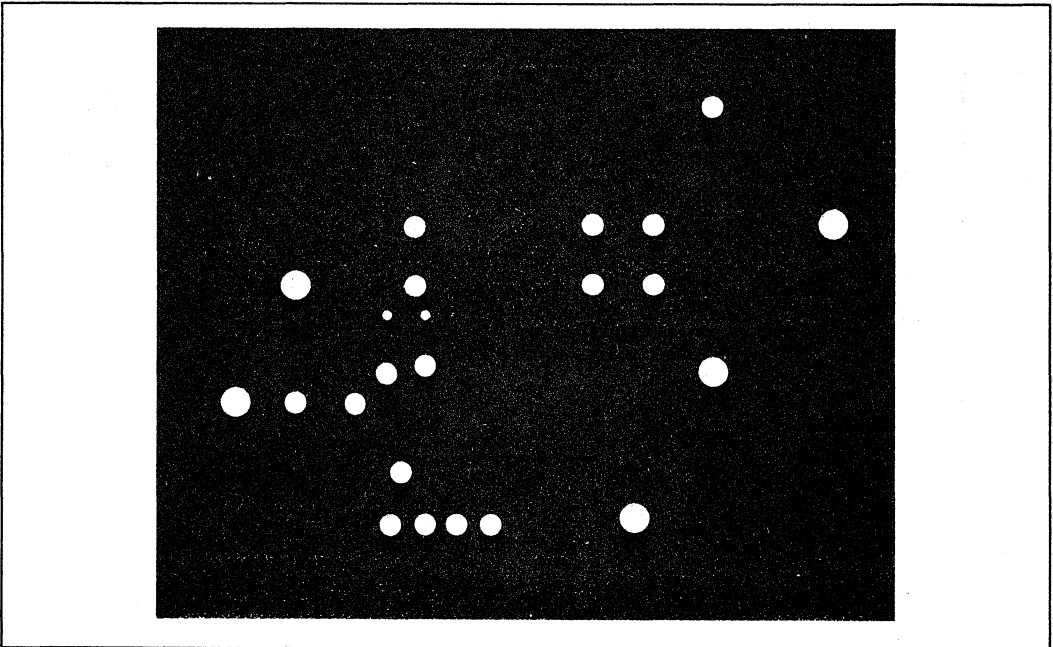


Fig. 19 Ground plane side of demonstration board. Scale = 2:1.

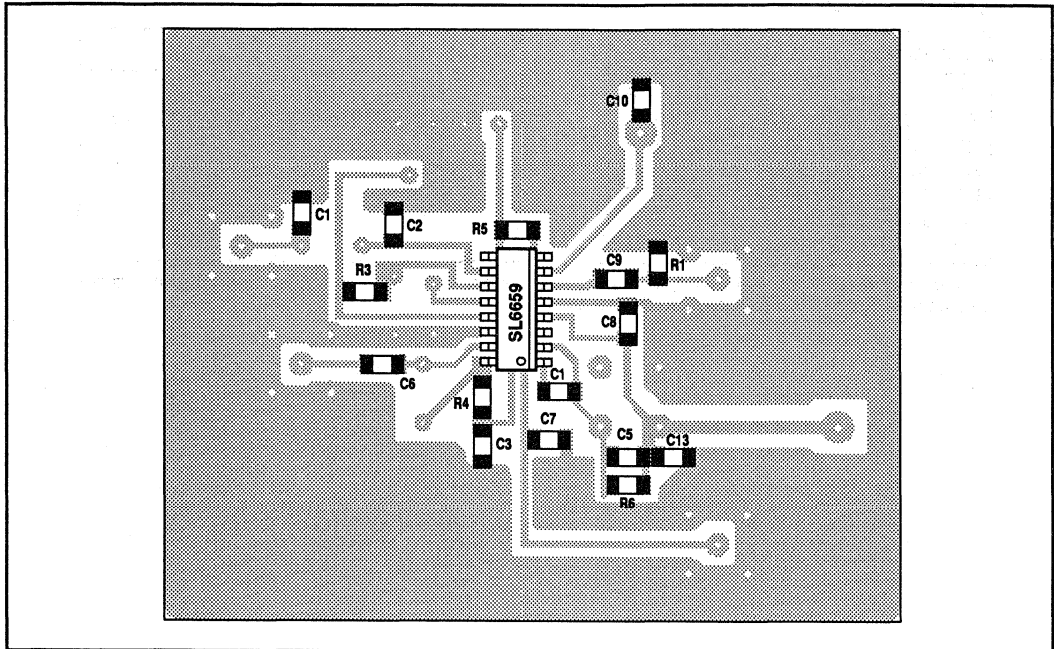


Fig. 20 Demonstration board surface mount component overlay (track side). Scale = 2:1.

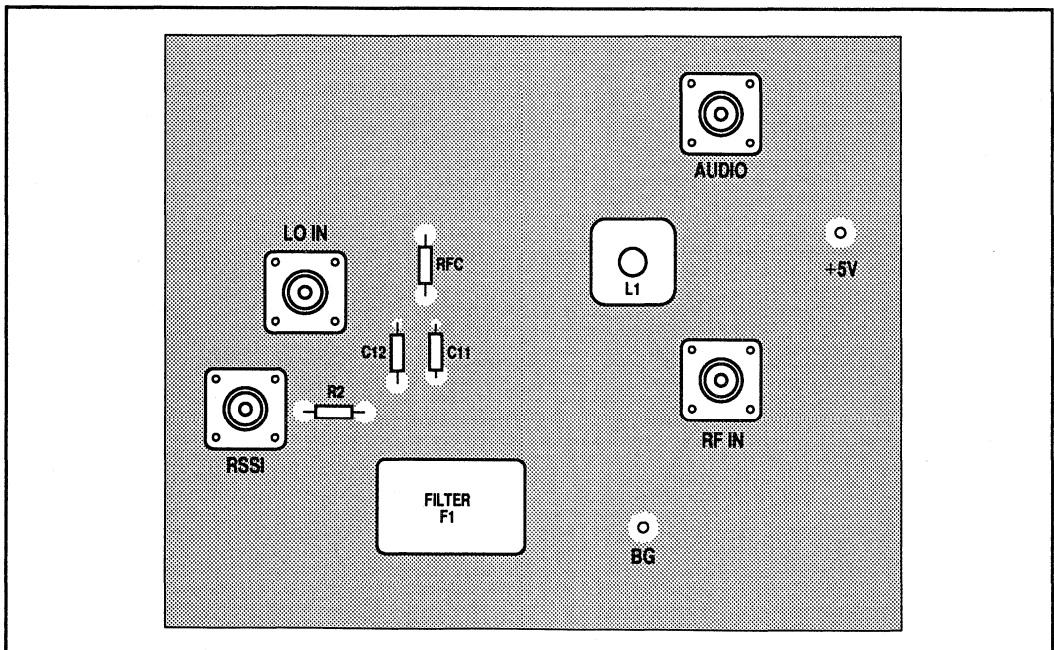


Fig. 21 Demonstration board connectors and through-board component overlay (ground plane side). Scale = 2:1.

**SL6659**

**COMPONENT LIST**

Resistors		Capacitors		Inductors		Filter
R1	51Ω	C1	100nF	C8	470nF	F1* MURATA Type CFW 445 E
R2*	1kΩ	C2	10nF	C9	10nF	
R3	1.5kΩ	C3	10nF	C10	100nF	
R4	10kΩ	C4	10pF	C11	220nF*	
R5	1.5kΩ	C5	330pF	C12	220nF*	
R6	33kΩ	C6	1nF	C13	220nF	
		C7	270pF			
				L1* 330μH (adjustable), CAMBION Type 553-7107-43 RFC* 4.7μH		

Components marked thus: \* are through-board mounted from the ground plane side; all other components are surface mounted on the track side. See Figs. 20 and 21.

# Section 3

## Prescalers





# SP8704

## 950MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8704 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8704 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

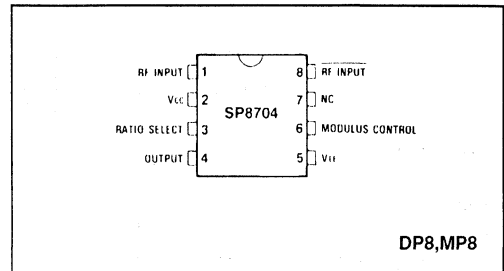


Fig. 1 Pin connections - top view

### FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

### QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C
Input voltage	2.5V p-p

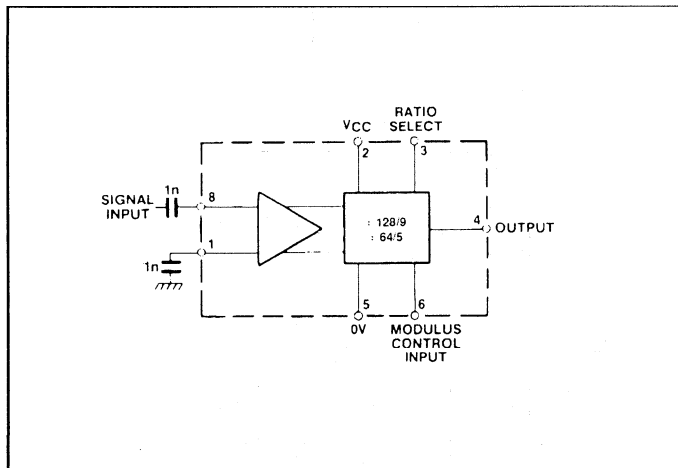


Fig. 2 Functional diagram SP8704

SP8704

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = +2.75\text{V}$  to  $+5.5\text{V}$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		10		mA	Including output emitter follower Sinewave input into 50Ω
Input sensitivity	10MHz		150	mV rms	
	80MHz		25		
	150MHz		15		
	850MHz		15		
Input impedance	950MHz		50	Ω	
		50		pF	
Output		1		V pk-pk	Emitter follower output current source = 0.75mA
Ratio select (pin 3)	LO		1	V	
	HI	$V_{CC}$		V	
Modulus control (pin 6)	LO		1	V	
	HI	2		V	
Clock to output delay		8		ns	
Set up time		16		ns	
Release time		16		ns	

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

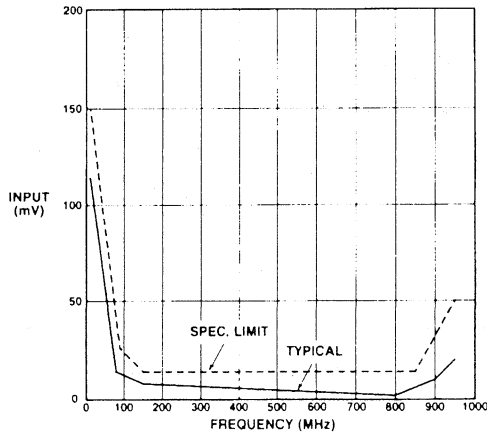


Fig. 3 Typical input sensitivity at 85°C



# SP8713

## 1100MHz VERY LOW CURRENT THREE MODULUS DIVIDER

The SP8713 is a switchable divide by 64/65/72 programmable divider which is guaranteed to operate up to 1100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 4.1mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers, such as the NJ88C51.

### FEATURES

- Operation to 1100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Inputs
- Push Pull Output Drive
- ESD Protection on All Pins†

### APPLICATIONS

- Cellular Telephones
- Cordless Telephones
- Mobile Radio

† ESD precautions must be observed

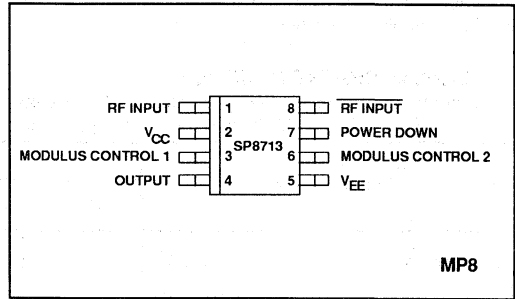


Fig. 1 Pin connections - top view

### ORDERING INFORMATION

- SP8713 IG MPAS Industrial Temperature Range  
Miniature Plastic DIL Package
- SP8713 IG MPAC As above supplied on Tape and Reel

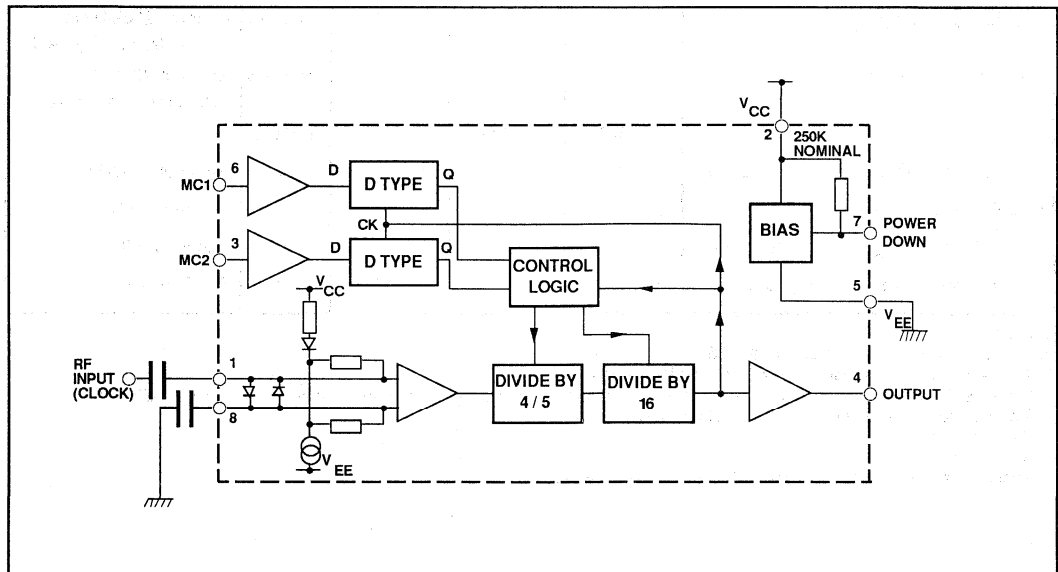


Fig. 2 Block diagram

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage ( $V_{EE}=0V$ )	(note 1)	-0.5V to 7V
Control and RF inputs,		
RF output ( $V_{EE}=0V$ )	(note 1)	-0.5V to $V_{CC}+0.5V$
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

**ELECTRICAL CHARACTERISTICS**

Guaranteed over the following conditions (unless otherwise stated):

$V_{CC}=+2.7V$  to  $+5.5V$  (with respect to  $V_{EE}$ ), Output load (pin 4) = 10pF,  $T_{amb} = -40°C$  to  $+85°C$  (note 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current (note 3)		4.1	4.7	mA	Power down input low
Supply current (note 3)		8	50	µA	Power down input high
Power down high	$V_{CC}-0.5$		$V_{CC}$	V	
Power down low	0		$V_{CC}-2.0$	V	
Modulus control 1 high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 64 or 72
Modulus control 1 low (note 4)	0		$0.4V_{CC}$	V	Divide by 65 or 72
Modulus control 2 high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 72
Modulus control 2 select low (note 4)	0		$0.4V_{CC}$	V	Divide by 64 or 65
Max. sinewave input frequency	1100			MHz	See Figure 5
Min. sinewave input frequency			200	MHz	See Figure 5
Min. RF input voltage			50	mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Max. RF input voltage	200			mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Output level (pin 4)	500	600		mV p-p	
Modulus set-up time, $t_s$ (notes 5,6,8)	20			ns	RF input = 1GHz
Modulus hold time, $t_h$ (notes 6,8)			1	ns	RF input = 1GHz
Power down time, $t_{pd}$ (notes 7,8)			10	µs	See Figure 9
Power down recovery time, $t_{pu}$ (notes 7,8)			6	µs	See Figure 9

NOTES

2. All electrical testing is performed at +85°C.
3. Typical values are measured at +25°C and  $V_{CC} = +5V$ .
4. Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
5. Modulus control is latched at the end of the previous cycle.
6. See Figure 4.
7. See Figure 8.
8. These parameters are not tested but are guaranteed by design.

**OPERATING NOTES**

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors.

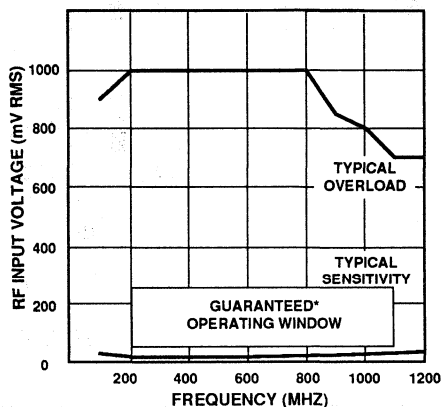
The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8713 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/ $\mu$ s.

POWER DOWN (pin 7) is connected internally to a pull-up resistor. If the battery economy facility is not used, pin 7 should be connected to  $V_{EE}$ .

Modulus Control 1 (Pin 3)	Modulus Control 2 (Pin 6)	Division Ratio
L	L	65
H	L	64
H	H	72
L	H	72

Table 1 Truth table



\* Tested as specified in table of Electrical Characteristics

Fig. 3 Typical input characteristics

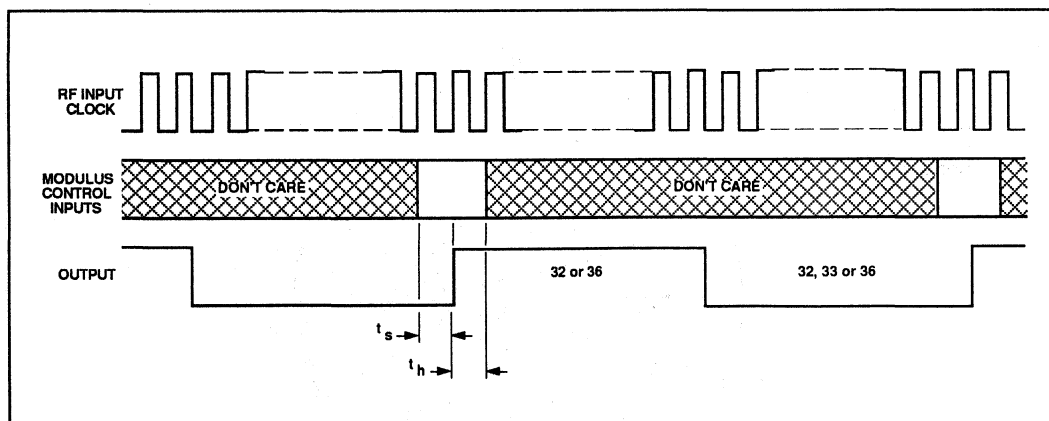


Fig. 4 Modulus control timing diagram

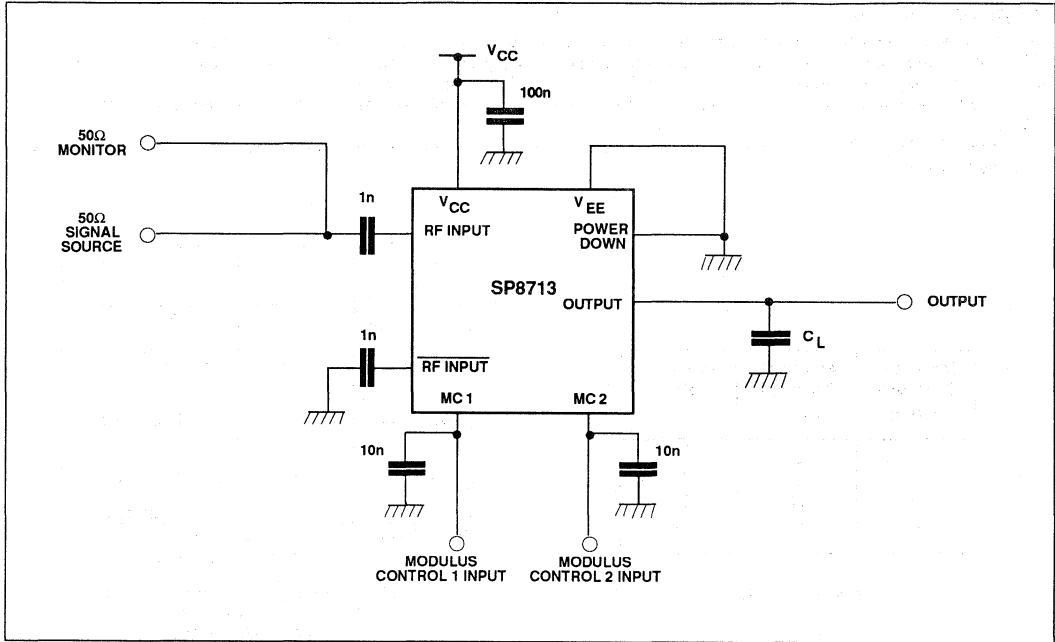


Fig. 5 Toggle frequency test circuit

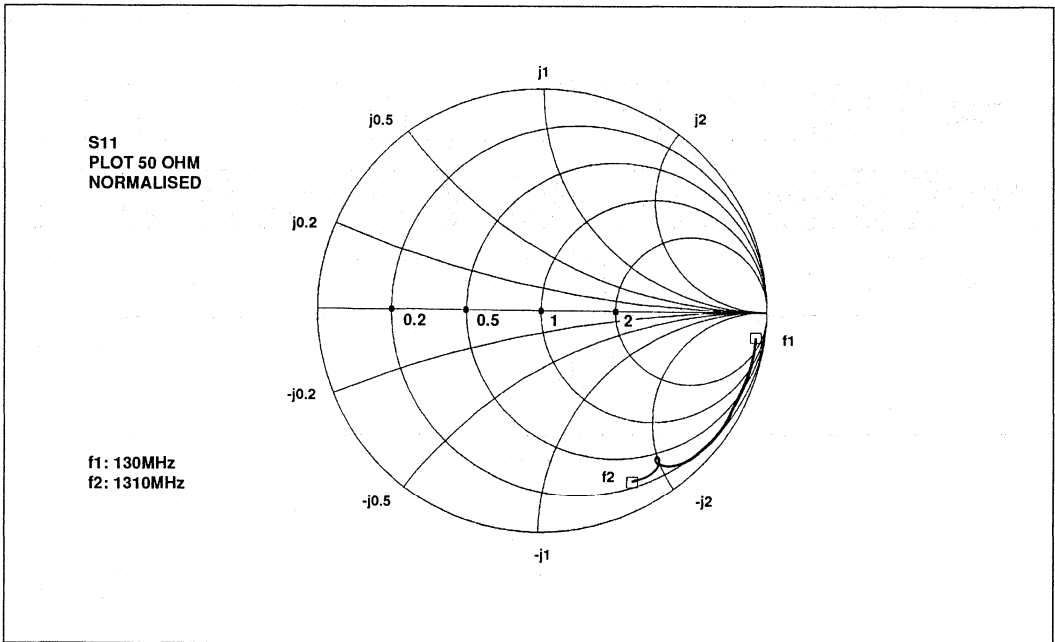


Fig. 6 Typical S11 parameter for pin 1.  $V_{CC} = +5.0V$

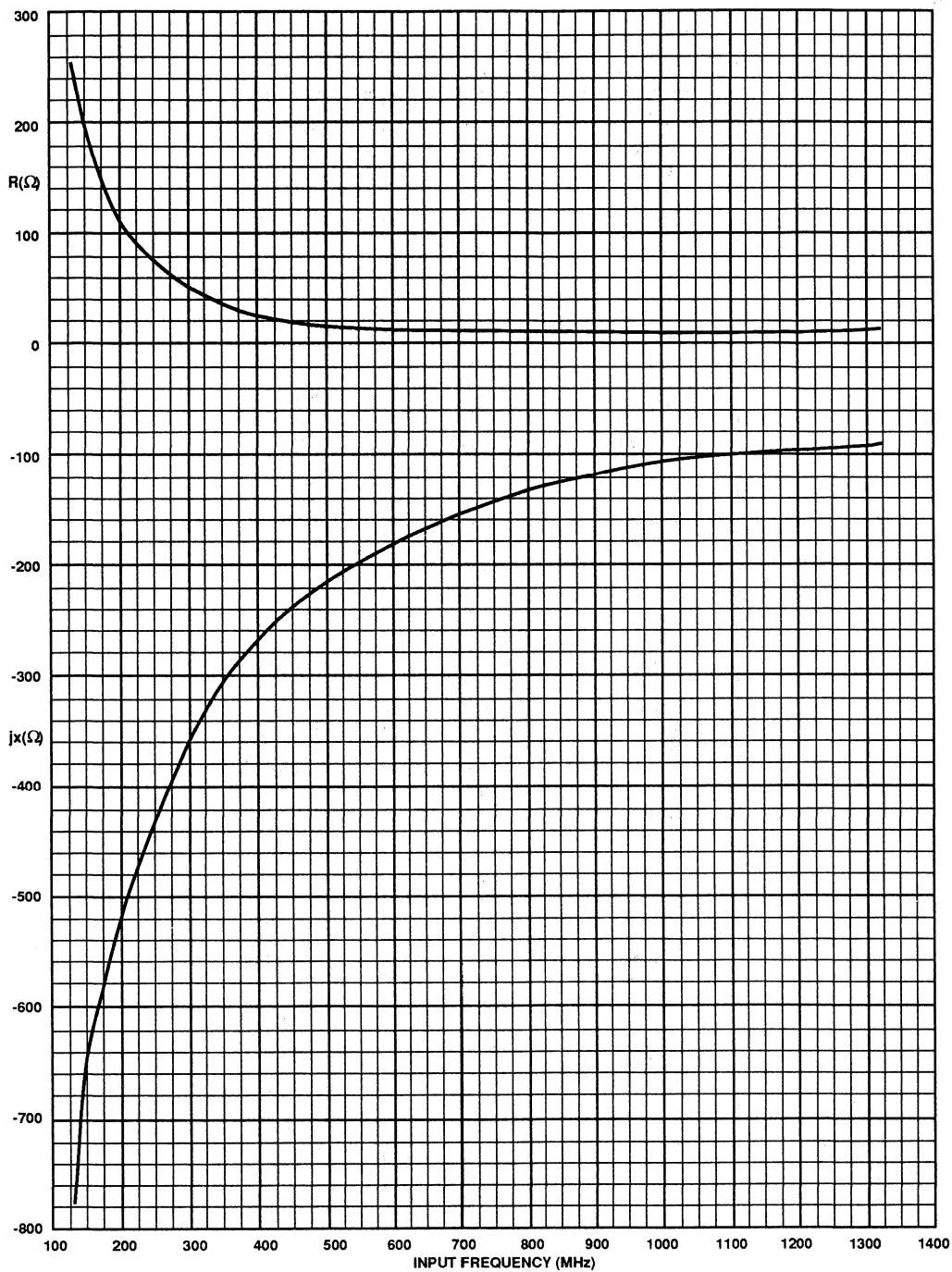


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R ( $\Omega$ )	jx ( $\Omega$ )
130.000	255.068	-733.538
153.600	153.362	-688.623
177.200	153.330	-583.339
200.800	115.187	-545.839
224.400	88.649	-482.377
248.000	80.815	-441.798
271.600	71.050	-411.502
295.200	56.207	-369.645
318.800	39.526	-346.620
342.400	41.338	-323.129
366.000	38.779	-304.804
389.600	39.210	-280.556
413.200	23.809	-269.674
436.800	21.221	-255.279
460.400	27.545	-245.161
484.000	23.333	-234.680
507.600	22.227	-224.572
531.200	19.931	-211.375
554.800	17.767	-203.241
578.400	17.636	-194.613
602.000	14.607	-186.545
625.600	12.479	-182.049
649.200	13.075	-174.839
672.800	12.891	-168.320
696.400	12.583	-160.468
720.000	11.250	-156.267
743.600	10.213	-149.642
767.200	10.187	-145.328
790.800	11.269	-143.144
814.400	11.081	-137.557
838.000	10.509	-132.750
861.600	10.063	-129.254
885.200	10.172	-124.495
908.800	10.745	-120.568
932.400	10.841	-118.100
956.000	10.884	-113.395
979.600	12.260	-109.552
1003.20	12.984	-105.975
1026.80	14.508	-103.110
1050.40	16.625	-99.886
1074.00	19.260	-98.149
1097.60	22.799	-98.605
1121.20	23.285	-99.907
1144.80	21.149	-100.925
1168.40	18.956	-99.639
1192.00	16.434	-98.425
1215.60	14.377	-95.033
1239.20	13.743	-92.553
1262.80	12.711	-89.249
1286.40	12.776	-86.081
1310.00	12.598	-82.581

Table.2 Coefficients for Fig.7

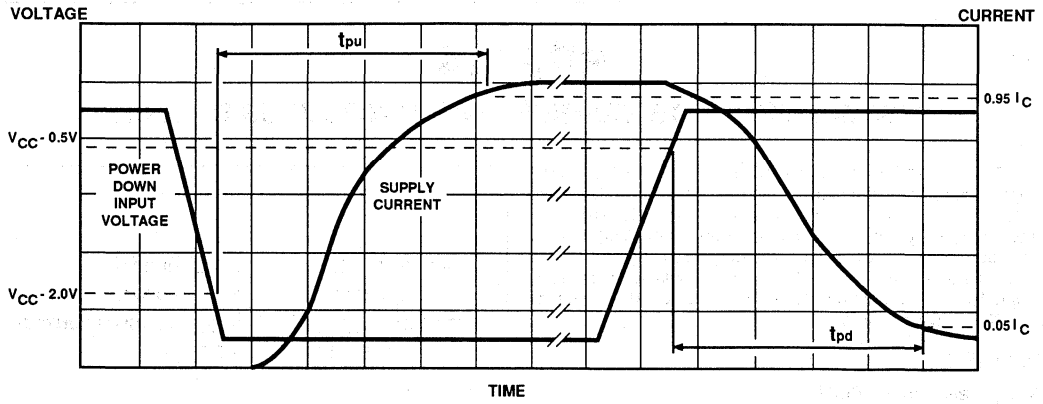


Fig. 8 Power up and power down

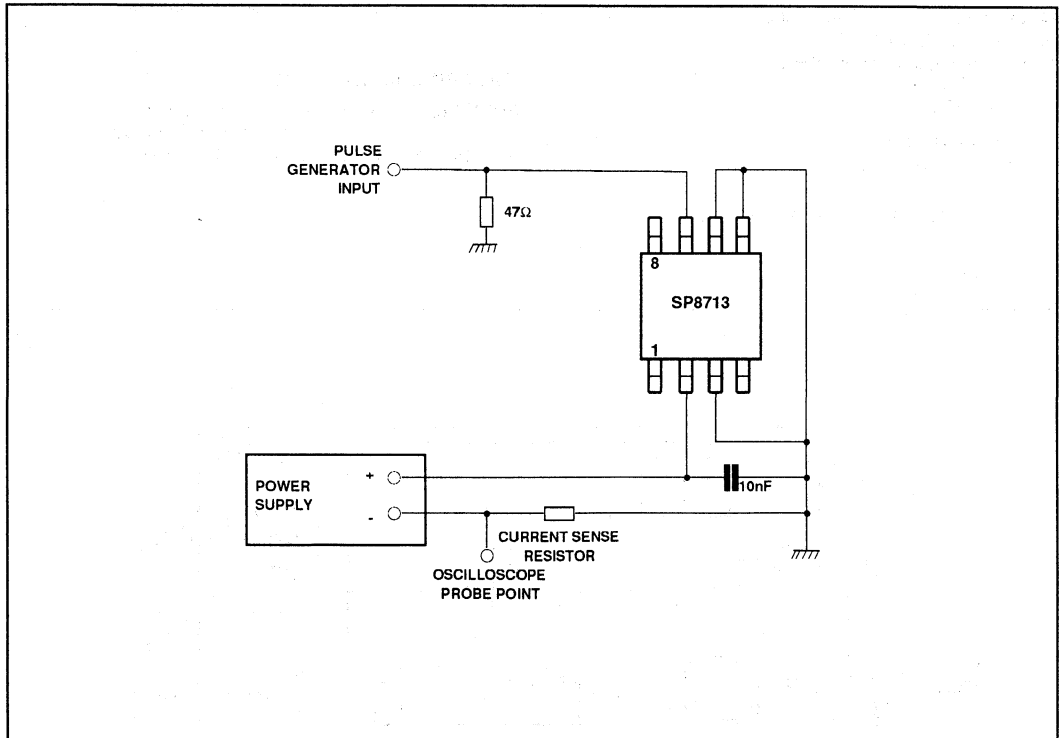


Fig. 9 Power-down time test circuit

# SP8714

## 2100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8714 is a switchable divide by 32/33, 64/65 programmable divider which is guaranteed to operate up to 2100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 6.8mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

### FEATURES

- Operation to 2100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

### APPLICATIONS

- Cellular Telephones
- Cordless Telephones

† ESD precautions must be observed

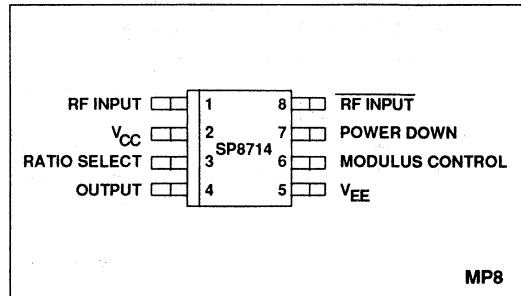


Fig. 1 Pin connections - top view

### ORDERING INFORMATION

- SP8714 IG MPAS Industrial Temperature Range  
Miniature Plastic DIL Package
- SP8714 IG MPAC As above supplied on Tape and Reel

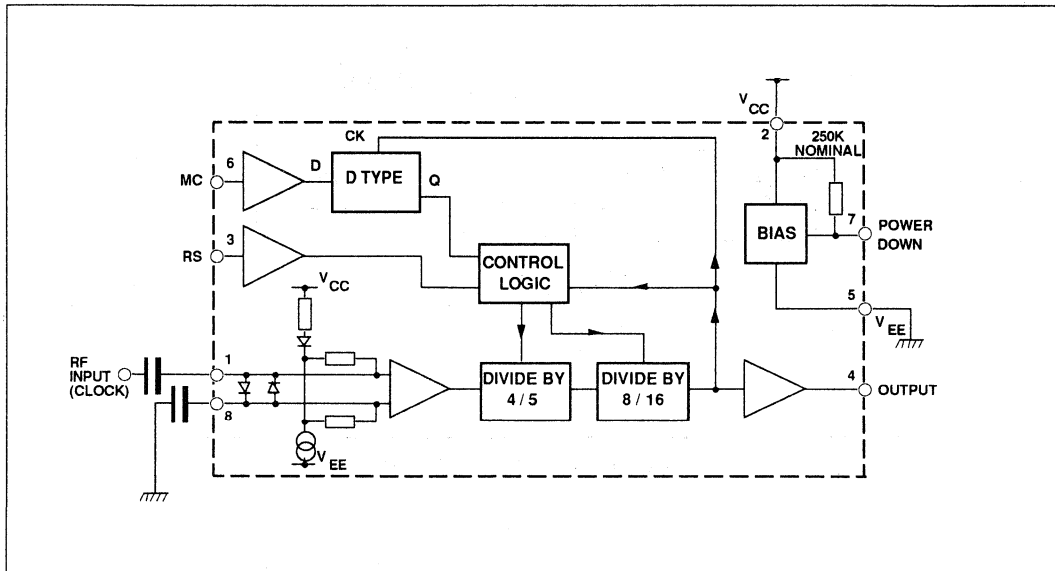


Fig. 2 Block diagram



**ABSOLUTE MAXIMUM RATINGS**

Supply voltage ( $V_{EE}=0V$ )	(note 1)	-0.5V to 7V
Control and RF inputs,		
RF output ( $V_{EE}=0V$ )	(note 1)	-0.5V to $V_{CC}+0.5V$
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration &lt;2 minutes.

**ELECTRICAL CHARACTERISTICS**

Guaranteed over the following conditions (unless otherwise stated):

 $V_{CC}=+2.7V$  to  $+5.5V$  (with respect to  $V_{EE}$ ), Output load (pin 4) = 10pF,  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$  (note 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current (note 3)		6.8	8.5	mA	Power down input low
Supply current (note 3)		8	50	$\mu A$	Power down input high
Power down high	$V_{CC}-0.5$		$V_{CC}$	V	
Power down low	0		$V_{CC}-2.0$	V	
Modulus control high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 32 or 64
Modulus control low (note 4)	0		$0.4V_{CC}$	V	Divide by 33 or 65
Ratio select high (note 4, 9)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 32 or 33
Ratio select low (note 4, 9)	0		$0.4V_{CC}$	V	Divide by 64 or 65
Max. sinewave input frequency	2100			MHz	See Figure 5
Min. sinewave input frequency			200	MHz	See Figure 5
Min. RF input voltage			50	mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Max. RF input voltage	200			mV RMS	RF input 200MHz to 2100MHz. See Figure 5
Output level (pin 4)	500	600		mV p-p	
Modulus set-up time, $t_s$ (notes 5,6,8)	10			ns	RF input = 1GHz
Modulus hold time, $t_h$ (notes 6,8)			1	ns	RF input = 1GHz
Power down time, $t_{pd}$ (notes 7,8)			10	$\mu s$	See Figure 9
Power down recovery time, $t_{pu}$ (notes 7,8)			8	$\mu s$	See Figure 9

**NOTES**

- All electrical testing is performed at +85°C.
- Typical values are measured at +25°C and  $V_{CC} = +5V$ .
- Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
- Modulus control is latched at the end of the previous cycle.
- See Figure 4.
- See Figure 8.
- These parameters are not tested but are guaranteed by design.
- The ratio select pin is not intended to be switched dynamically.

# SP8714

## OPERATING NOTES

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors.

The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8714 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than  $100\text{V}/\mu\text{s}$ .

POWER DOWN (pin 7) is connected internally to a pull-up resistor. If the battery economy facility is not used, pin 7 should be connected to  $V_{EE}$ .

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	65
L	H	64
H	L	33
H	H	32

Table 1 Truth table

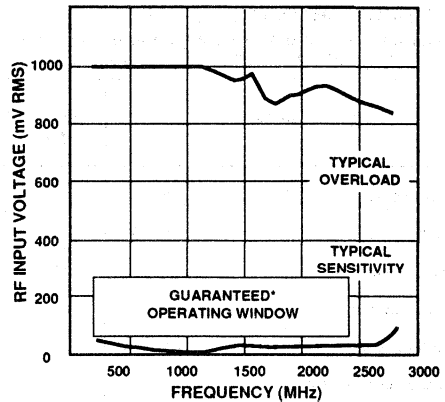


Fig. 3 Typical input characteristics

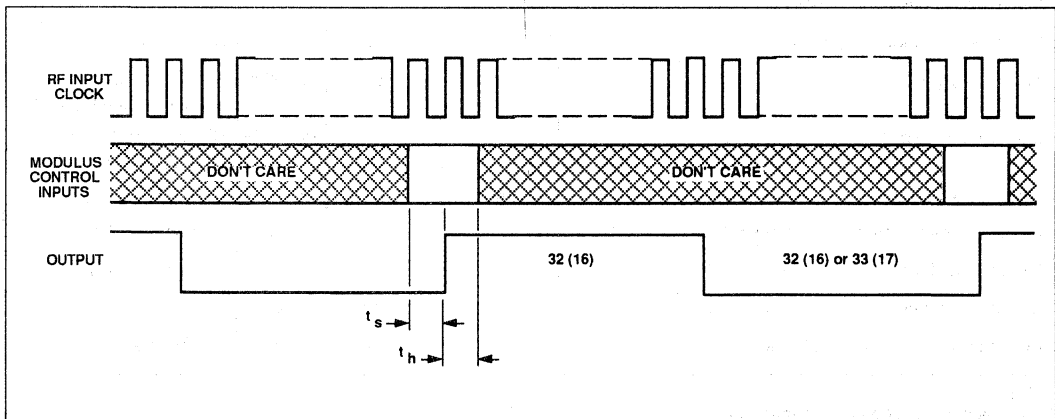


Fig. 4 Modulus control timing diagram

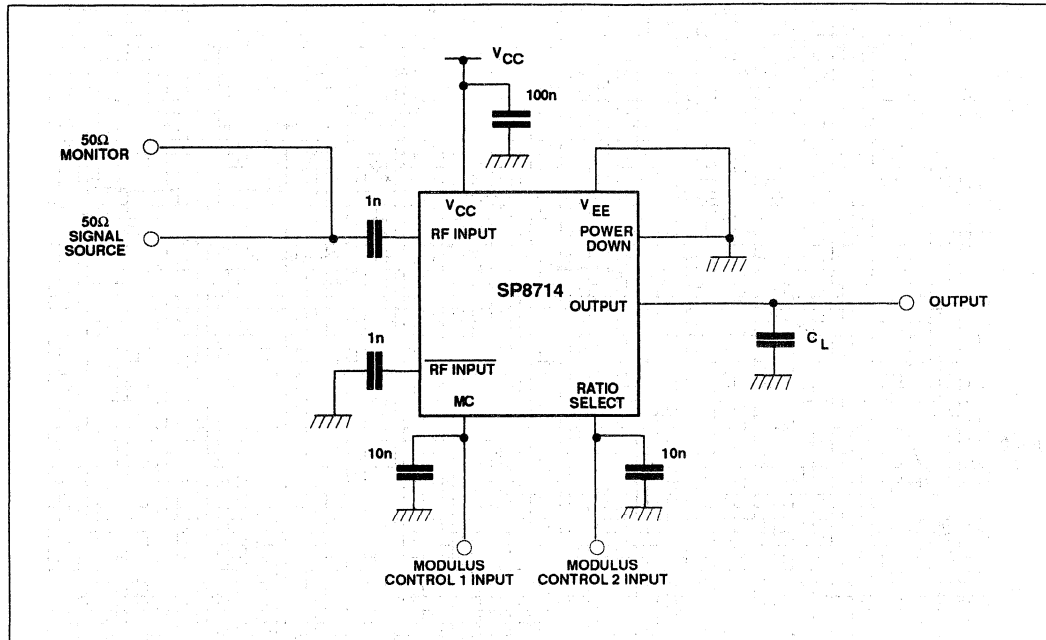


Fig. 5 Toggle frequency test circuit

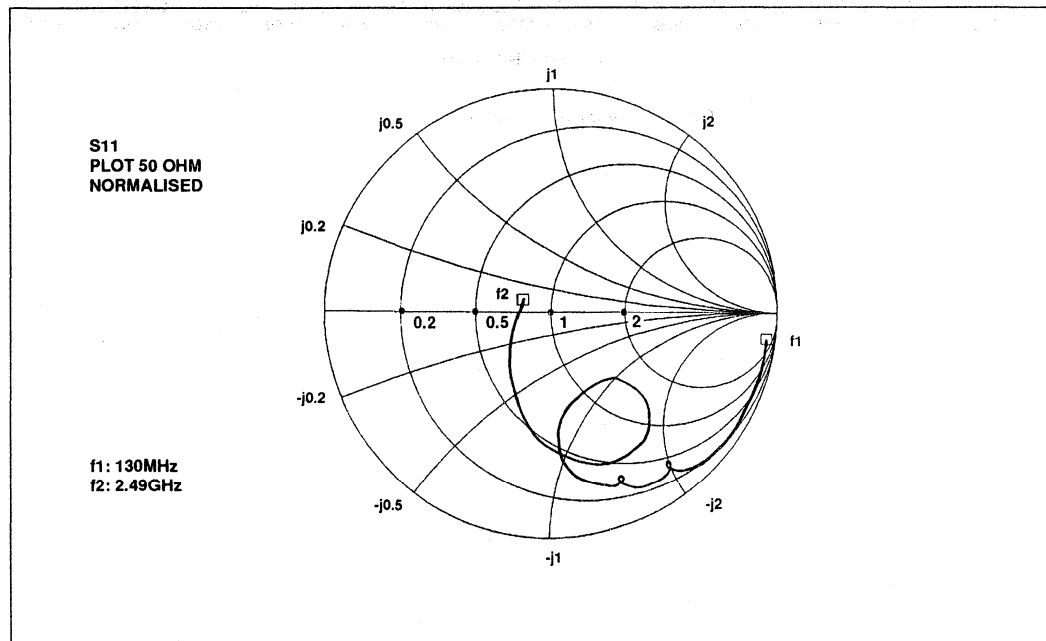


Fig. 6 Typical S11 parameter for pin 1.  $V_{CC} = +5.0V$

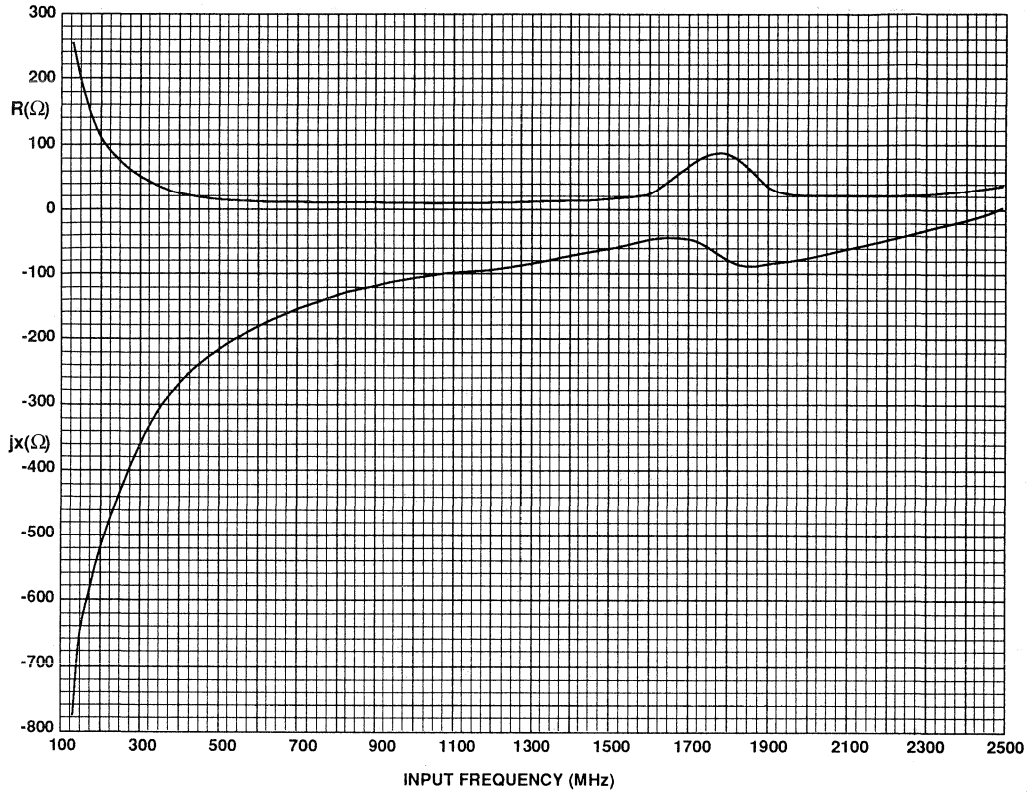


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R ( $\Omega$ )	jx ( $\Omega$ )
130.000	255.068	-733.538
177.200	153.330	-583.339
224.400	88.649	-482.377
271.600	71.050	-411.502
318.800	39.526	-346.620
366.000	38.779	-304.804
413.200	23.809	-269.674
460.400	27.545	-245.161
507.600	22.227	-224.572
554.800	17.767	-203.241
602.000	14.607	-186.545
649.200	13.075	-174.839
596.400	12.583	-160.468
743.600	10.213	-149.642
790.800	11.269	-143.144
838.000	10.509	-132.750
885.200	10.172	-124.495
332.400	10.841	-118.100
979.600	12.260	-109.552
1026.80	14.508	-103.110
1074.00	19.260	-98.149
1121.20	23.285	-99.907
1168.40	18.956	-99.639
1215.60	14.377	-95.033
1262.80	12.711	-89.249
1310.00	12.598	-82.581
1357.20	14.565	-77.212
1404.40	19.164	-71.976
1451.60	15.001	-70.250
1498.80	15.864	-61.898
1546.00	18.993	-53.403
1593.20	26.822	-44.704
1640.40	39.830	-41.522
1687.60	47.875	-43.255
1734.80	63.267	-44.879
1782.00	74.259	-67.801
1829.20	58.878	-86.964
1876.40	42.530	-87.052
1923.60	32.302	-80.484
1970.80	27.333	-73.570
2018.00	24.894	-67.291
2065.20	23.369	-60.620
2112.40	23.577	-54.716
2159.60	23.023	-49.220
2206.80	23.325	-43.340
2254.00	24.623	-37.163
2301.20	26.340	-30.805
2348.40	28.632	-24.040
2395.60	31.161	-17.165
2442.80	34.219	-8.172
2490.00	39.808	-4.368

Table.2 Coefficients for Fig.7

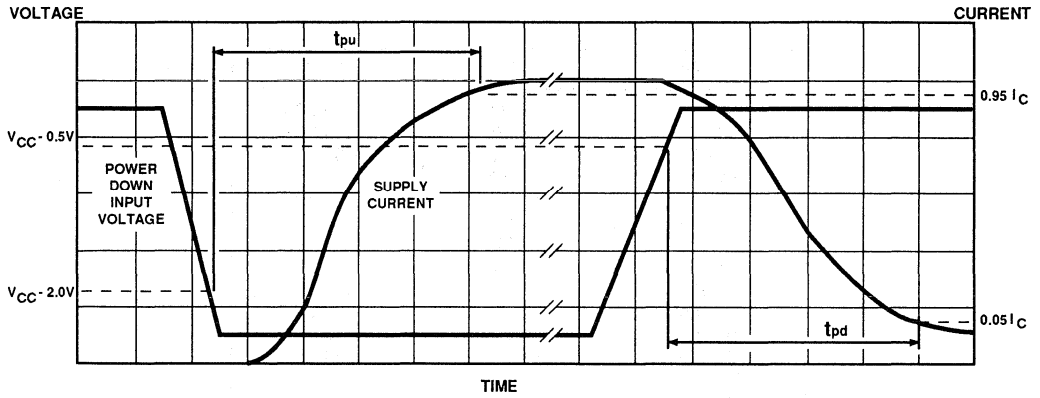


Fig. 8 Power up and power down

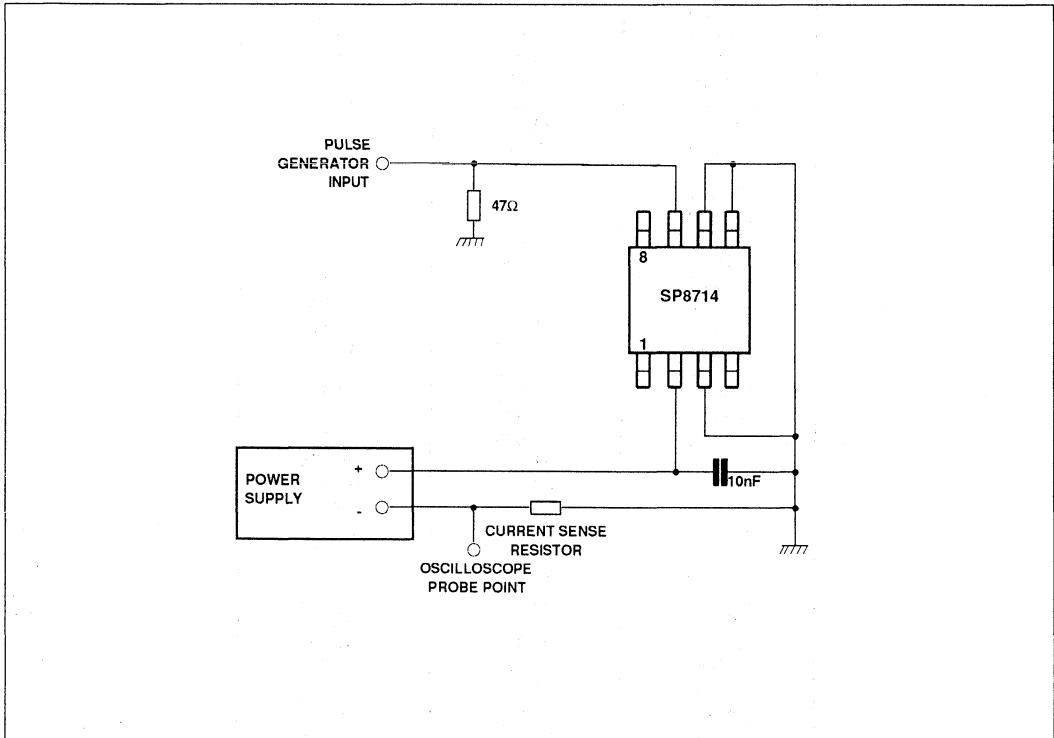


Fig. 9 Power-down time test circuit

# SP8715

## 1100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8715 is a switchable divide by 64/65, 128/129 programmable divider which is guaranteed to operate up to 1100MHz. It will operate from a supply of 2.7V to 5.5V and requires typically 3.6mA (including the output current). It also features a power down facility for battery economy.

The RF inputs are internally biased and should be capacitively coupled to the signal source. The output is designed to interface with CMOS synthesisers.

### FEATURES

- Operation to 1100MHz
- Very Low Power
- Single Supply Operation 2.7V to 5.5V
- Power Down Facility for Battery Economy
- Latched Modulus Control Input
- Push Pull Output Drive
- ESD Protection on All Pins†

### APPLICATIONS

- Cellular Telephones
- Cordless Telephones
- Mobile Radio

† ESD precautions must be observed

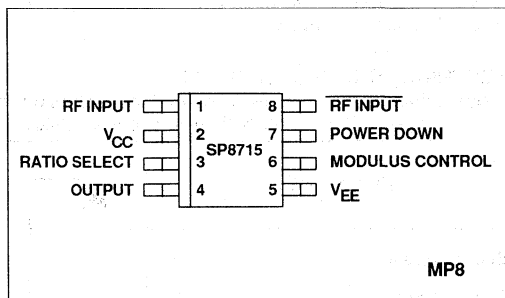


Fig. 1 Pin connections - top view

### ORDERING INFORMATION

- SP8715 IG MPAS Industrial Temperature Range  
Miniature Plastic DIL Package
- SP8715 IG MPAC As above supplied on Tape and Reel

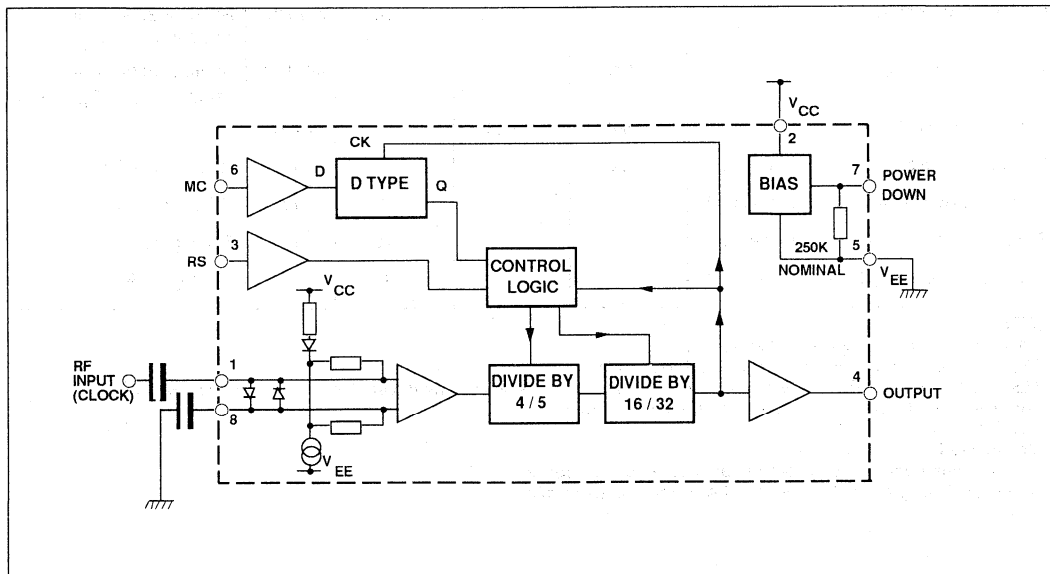


Fig. 2 Block diagram

# SP8715

## ABSOLUTE MAXIMUM RATINGS

Supply voltage ( $V_{EE}=0V$ )	(note 1)	-0.5V to 7V
Control and RF inputs,		
RF output ( $V_{EE}=0V$ )	(note 1)	-0.5V to $V_{CC}+0.5V$
RF input current	(note 1)	10mA
Operating temperature		-40°C to +85°C
Storage temperature range		-55°C to +150°C
Maximum junction temperature		+150°C

NOTE 1. Duration <2 minutes.

## ELECTRICAL CHARACTERISTICS

Guaranteed over the following conditions (unless otherwise stated):

$V_{CC}=+2.7V$  to  $+5.5V$  (with respect to  $V_{EE}$ ), Output load (pin 4) = 10pF,  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$  (note 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current (note 3)		3.6	4.2	mA	Power down input low
Supply current (note 3)		8	50	$\mu A$	Power down input high
Power down high	$V_{CC}-0.5$		$V_{CC}$	V	
Power down low	0		$V_{CC}-2.0$	V	
Modulus control high (note 4)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 64 or 128
Modulus control low (note 4)	0		$0.4V_{CC}$	V	Divide by 65 or 129
Ratio select high (note 4, 9)	$0.6V_{CC}$		$V_{CC}$	V	Divide by 64 or 65
Ratio select low (note 4, 9)	0		$0.4V_{CC}$	V	Divide by 128 or 129
Max. sinewave input frequency	1100			MHz	See Figure 5
Min. sinewave input frequency			200	MHz	See Figure 5
Min. RF input voltage			50	mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Max. RF input voltage	200			mV RMS	RF input 200MHz to 1100MHz. See Figure 5
Output level (pin 4)	500	600		mV p-p	
Modulus set-up time, $t_s$ (notes 5,6,8)	20			ns	RF input = 1GHz
Modulus hold time, $t_h$ (notes 6,8)			1	ns	RF input = 1GHz
Power down time, $t_{pd}$ (notes 7,8)			10	$\mu s$	See Figure 9
Power down recovery time, $t_{pu}$ (notes 7,8)			6	$\mu s$	See Figure 9

### NOTES

- All electrical testing is performed at +85°C.
- Typical values are measured at +25°C and  $V_{CC} = +5V$ .
- Modulus Control and Ratio Select are high impedance inputs which can be driven directly by standard CMOS outputs.
- Modulus control is latched at the end of the previous cycle.
- See Figure 4.
- See Figure 8.
- These parameters are not tested but are guaranteed by design.
- The ratio select pin is not intended to be switched dynamically.



**OPERATING NOTES**

The RF inputs are biased internally and are normally coupled to the signal source with suitable capacitors.

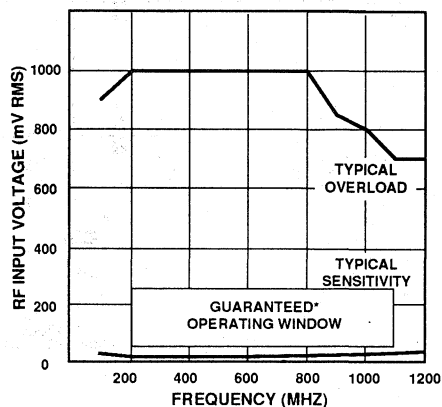
The output stage has a novel design and is intended to drive a CMOS synthesiser input. External pull-down resistors or circuits are not required. The SP8715 is not suitable for driving TTL or similar devices.

The device will operate down to DC frequencies for non-sinusoidal signals provided that the input slew rate is better than 100V/ $\mu$ s.

POWER DOWN (pin 7) is connected internally to a pull-down resistor. If the battery economy facility is not used, pin 7 should be either left unconnected or connected to  $V_{EE}$ .

Ratio Select (Pin 3)	Modulus Control (Pin 6)	Division Ratio
L	L	129
L	H	128
H	L	65
H	H	64

Table 1 Truth table



\* Tested as specified in table of Electrical Characteristics

Fig. 3 Typical input characteristics

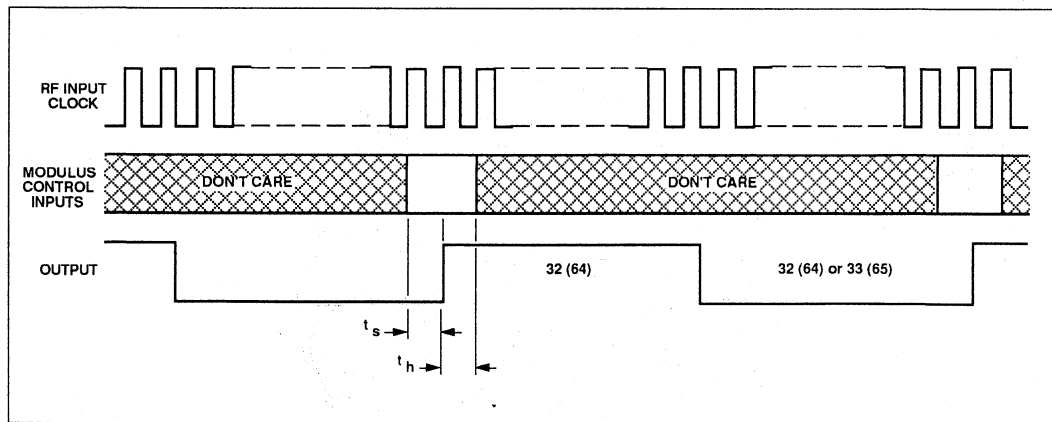


Fig. 4 Modulus control timing diagram

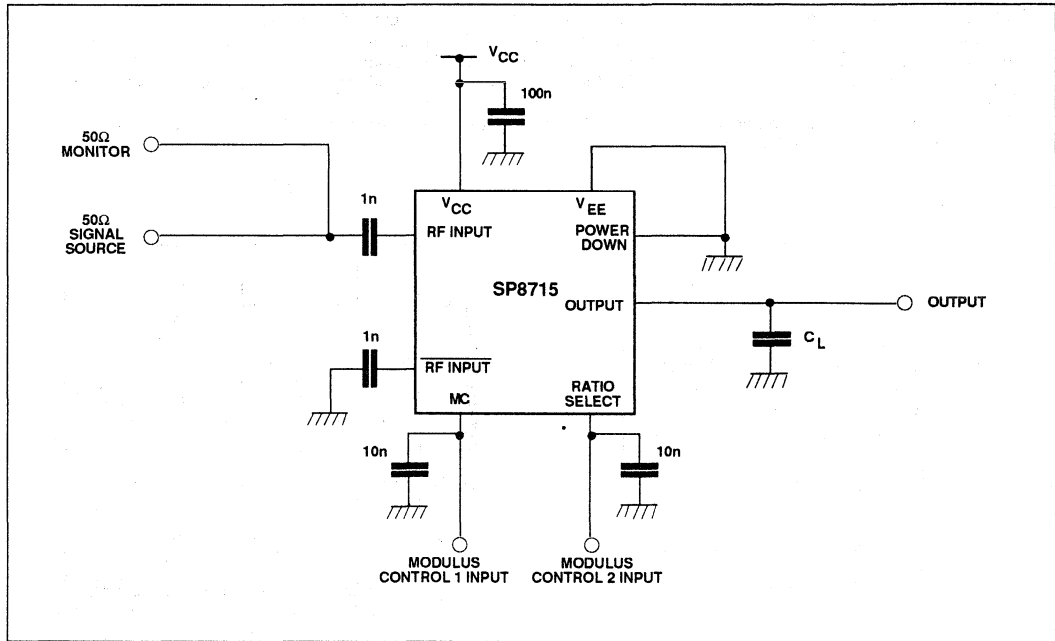


Fig. 5 Toggle frequency test circuit

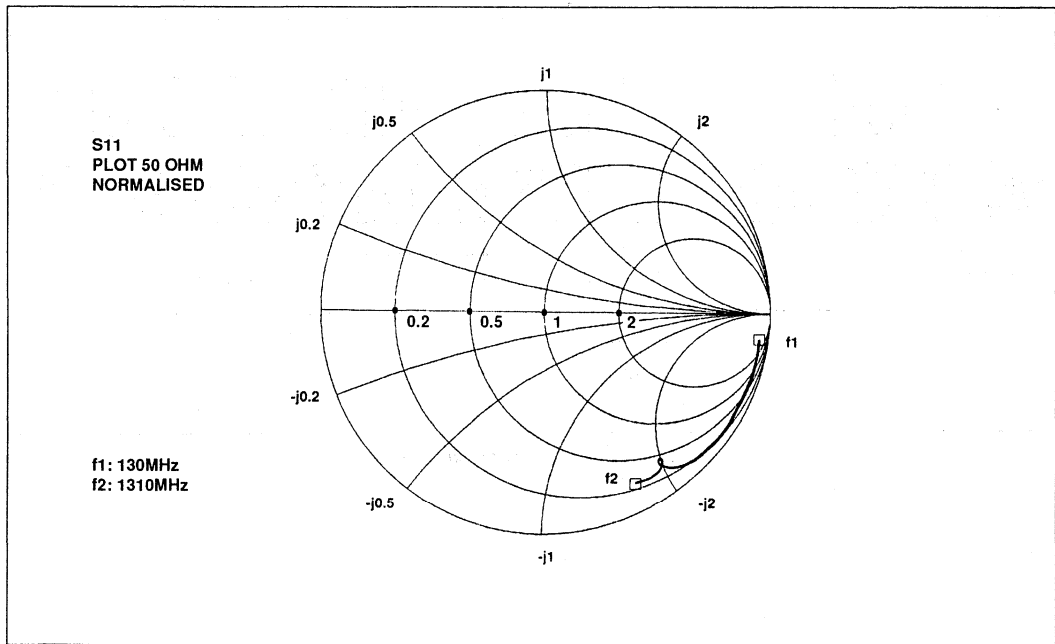


Fig. 6 Typical S11 parameter for pin 1.  $V_{CC} = +5.0V$

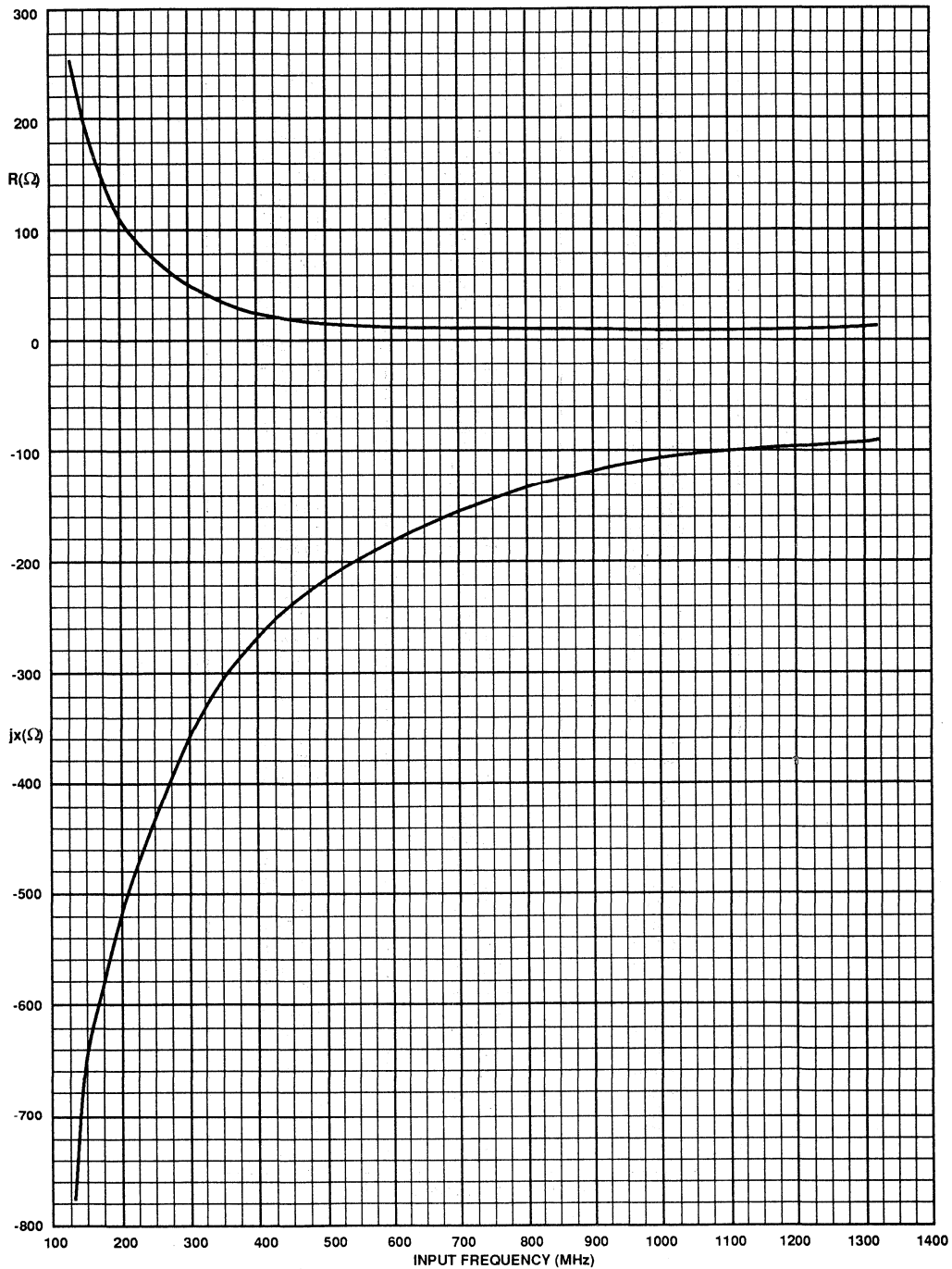


Fig. 7 Typical input impedance v. frequency

FREQ-MHZ	R ( $\Omega$ )	jx ( $\Omega$ )
130.000	255.068	-733.538
153.600	153.362	-688.623
177.200	153.330	-583.339
200.800	115.187	-545.839
224.400	88.649	-482.377
248.000	80.815	-441.798
271.600	71.050	-411.502
295.200	56.207	-369.645
318.800	39.526	-346.620
342.400	41.338	-323.129
366.000	38.779	-304.804
389.600	39.210	-280.556
413.200	23.809	-269.674
436.800	21.221	-255.279
460.400	27.545	-245.161
484.000	23.333	-234.680
507.600	22.227	-224.572
531.200	19.931	-211.375
554.800	17.767	-203.241
578.400	17.636	-194.613
602.000	14.607	-186.545
625.600	12.479	-182.049
649.200	13.075	-174.839
672.800	12.891	-168.320
696.400	12.583	-160.468
720.000	11.250	-156.267
743.600	10.213	-149.642
767.200	10.187	-145.328
790.800	11.269	-143.144
814.400	11.081	-137.557
838.000	10.509	-132.750
861.600	10.063	-129.254
885.200	10.172	-124.495
908.800	10.745	-120.568
932.400	10.841	-118.100
956.000	10.884	-113.395
979.600	12.260	-109.552
1003.20	12.984	-105.975
1026.80	14.508	-103.110
1050.40	16.625	-99.886
1074.00	19.260	-98.149
1097.60	22.799	-98.605
1121.20	23.285	-99.907
1144.80	21.149	-100.925
1168.40	18.956	-99.639
1192.00	16.434	-98.425
1215.60	14.377	-95.033
1239.20	13.743	-92.553
1262.80	12.711	-89.249
1286.40	12.776	-86.081
1310.00	12.598	-82.581

Table.2 Coefficients for Fig.7

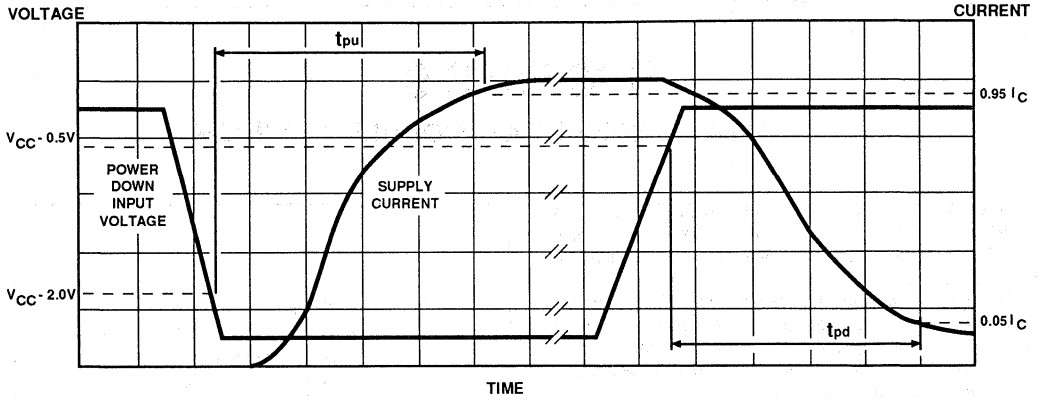


Fig. 8 Power up and power down

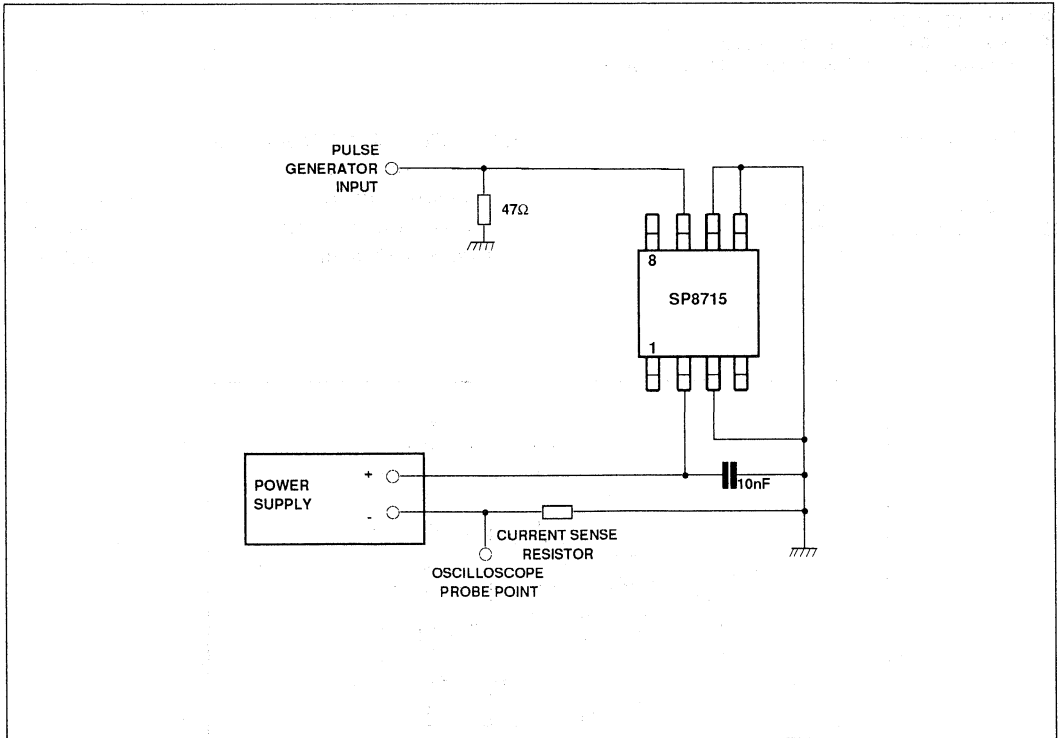


Fig. 9 Power-down time test circuit

# SP8716/8/9

## 520MHz LOW CURRENT TWO-MODULUS DIVIDERS

SP8716 + 40/41, SP8718 + 64/65, SP8719 + 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -40 °C to + 85 °C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

### FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

### QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 10.5mA typ.

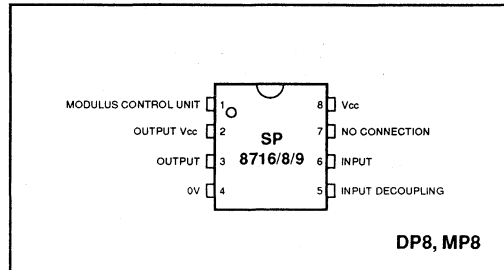


Figure : 1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. Junction temperature:	+175°C
Max. clock I/P voltage:	2.5V p-p

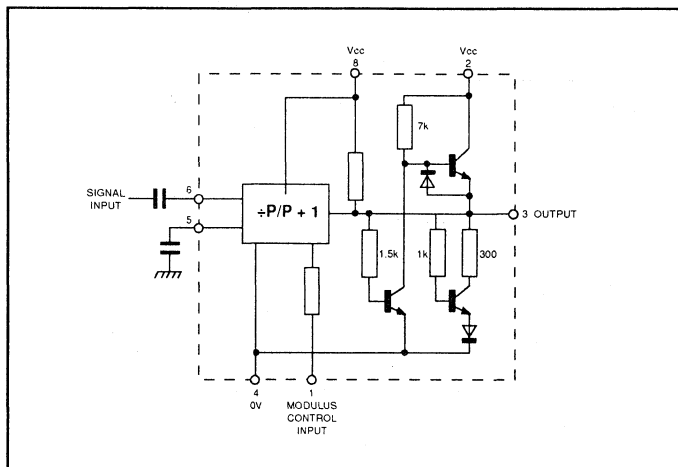


Figure 2 : Functional diagram

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):]

Supply voltage:  $V_{cc} = +4/95$  to 5.45V, Temperature:  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	$f_{max}$	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	$f_{min}$		30	MHz	Input 400-800mV p-p	2
Power supply current	$I_{CC}$		11.9	mA	$C_L = 3pF$ ; pins 2, 8 linked	1
Output high voltage	$V_{OH}$	$(V_{cc} - 1.2)$		V	$I_L = -0.2mA$	1
Output low voltage	$V_{OL}$		1	V	$I_L = 0.2mA$	1
Control input high voltage	$V_{INH}$	3.3	8	V	+P	1
Control input low voltage	$V_{INL}$	0	1.7	V	+P +1	1
Control input high current	$V_{INH}$		0.41	mA	$V_{INH} = 8V$	1
Control input low current	$V_{INL}$	-0.20		mA	$V_{INL} = 0V$	1
Clock to output delay	$t_p$		28	ns	$C_L = 10pF$	2
Set-up time	$t_s$	10		ns	$C_L = 10pF$	2
Release time	$t_r$	10		ns	$C_L = 10pF$	2

**NOTES**

1. Tested at 25°C only
2. Guaranteed but not tested

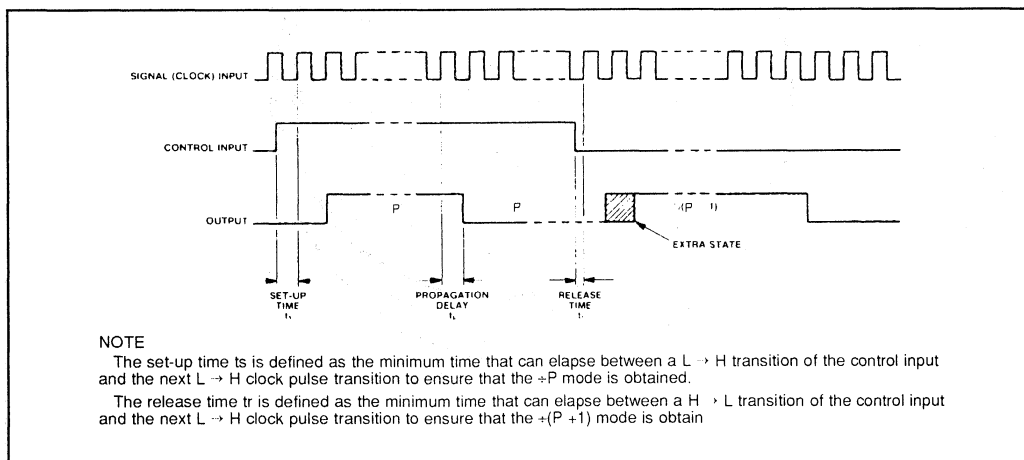
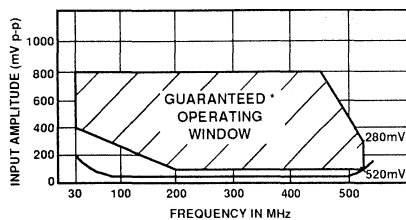


Figure 3 : Timing diagram



\*Tested as specified in table of Electrical Characteristics

Figure 4 : Typical input characteristics

**OPERATING NOTES**

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/us.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

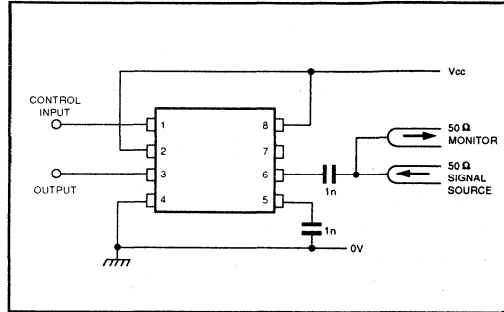


Figure 5: Toggle frequency test circuit

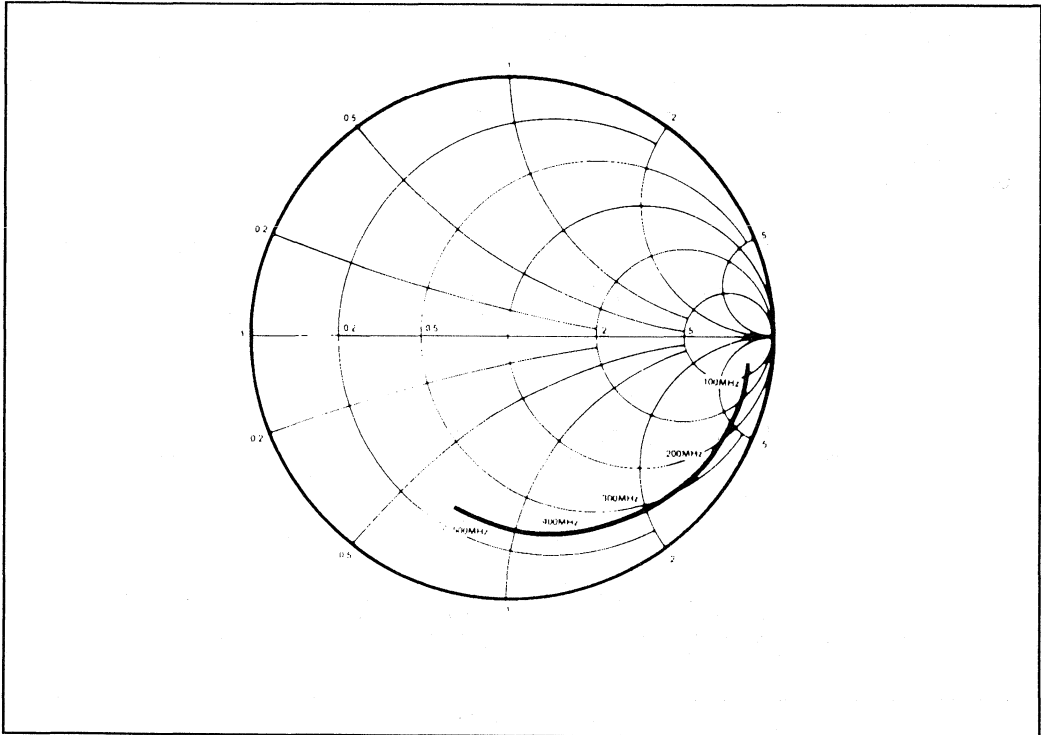


Figure 6: Typical input impedance



# SP8789

## 225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable +20/21 counter. It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

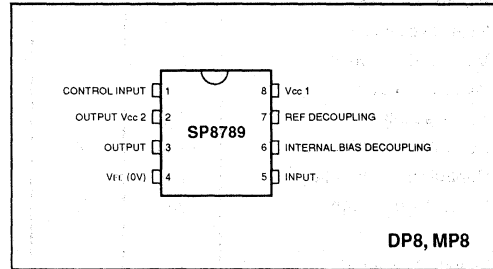


Figure 1 Pin connections - top view

### FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

### QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

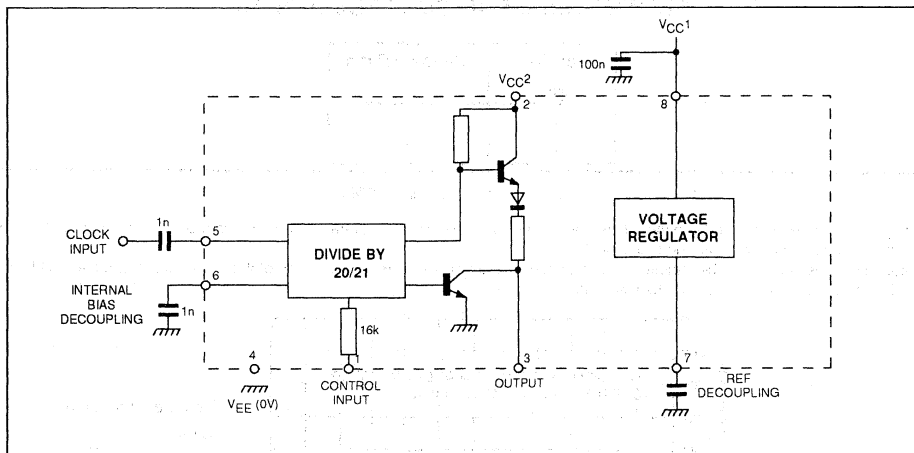


Figure 2 : Functional diagram SP8789

**SP8789**

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):]

Supply voltage :  $V_{CC} 1 \ \& \ 2 = 5.2 \pm 0.25V$  or 6.8V to 9.5V (see Operating Note 7):

$V_{EE} = 0V$ ; Temperature  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{max}$	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	$f_{min}$		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	$I_{EE}$		7	mA	Note 4	
Control input high voltage	$V_{INH}$	4		V	Note 4	
Control input low voltage	$V_{INL}$		2	V	Note 4	
Output high voltage	$V_{OH}$	2.4		V	Note 4	Pins 2, 7 and 8 linked $V_{CC} = 4.95V$ $I_{OH} = 100\mu A$
Output low voltage	$V_{OL}$		0.5	V	Note 4	Pin 2 linked to 8 and 7 $I_{OL} = 1.6mA$
Set up time	$t_s$	14		ns	Note 3	25°C
Release time	$t_r$	20		ns	Note 3	25°C
Clock to output propagation time	$t_p$		45	ns	Note 3	25°C

**NOTES**

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C

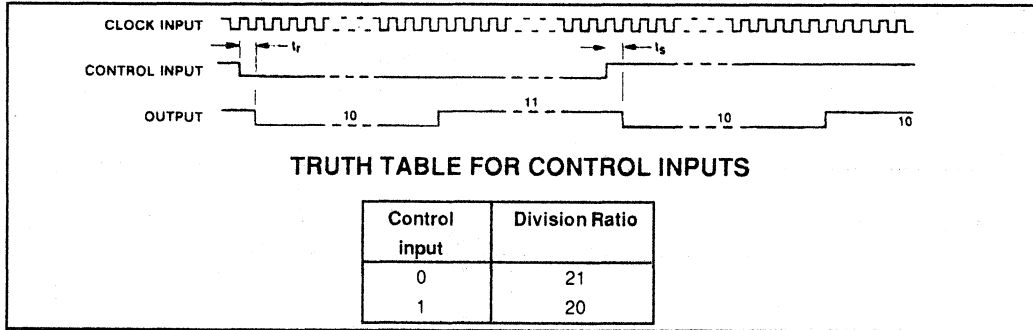
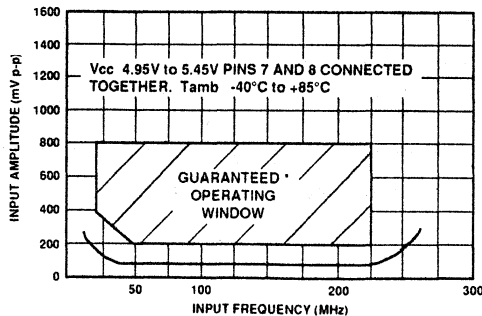


Figure 3 : Timing diagram SP8789

**NOTES**

The set-up time  $t_s$  is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the + 20 mode is selected.  
 The release time  $t_r$  is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the + 21 mode is selected.



\*Tested as specified  
in table of  
Electrical Characteristics

Figure 4 : Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/ $\mu$ s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.

5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

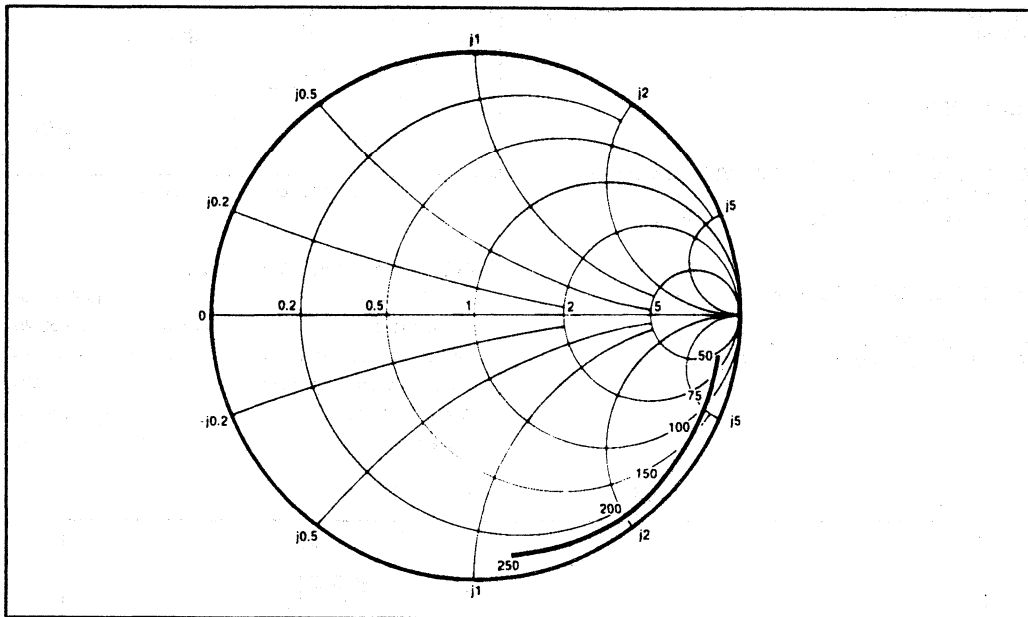


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

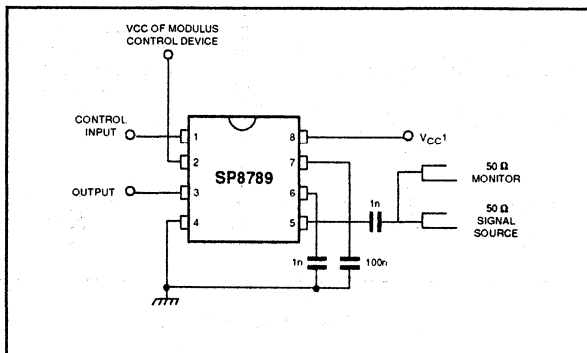


Figure 6 : Toggle frequency test circuit

# SP8792 225MHz ÷ 80/81

# SP8793 225MHz ÷ 40/41

## WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 AND SP8793 are low power programmable ÷80/81 and ÷40/41 counter, temperature range: -40°C to +85°C. They divide by 80(40) when in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

### FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

### QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical

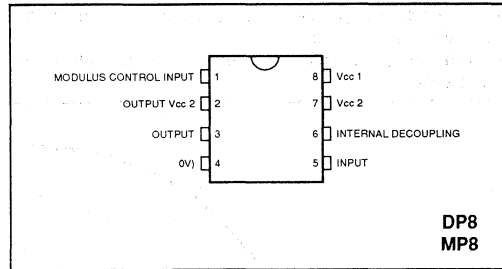


Figure 1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max.	10V

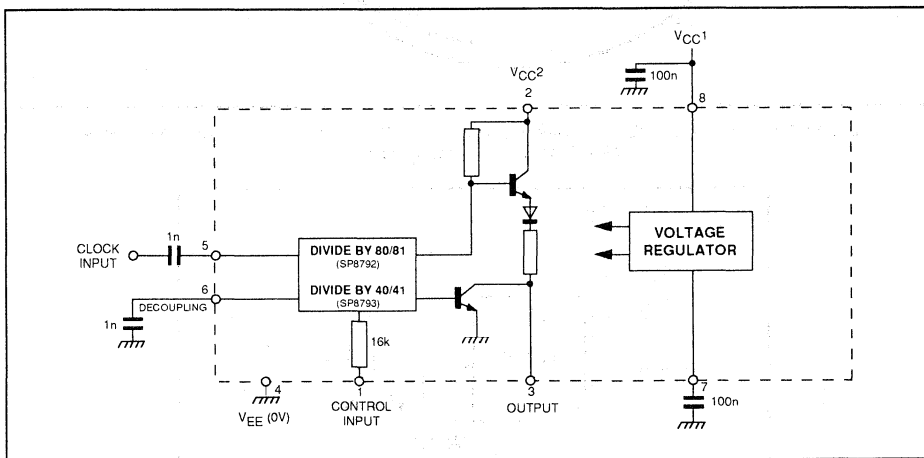


Figure 2 : Functional diagram SP8799

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):]

Supply voltage :  $V_{CC} = 5.2 \pm 0.25V$  or 6.8V to 9.5V (see Operating Note 6);  $V_{EE} = 0V$

Temperature  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{max}$	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	$f_{min}$		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	$I_{EE}$		7	mA	Note 4	
Control input high voltage	$V_{INH}$	4		V	Note 4	
Control input low voltage	$V_{INL}$		2	V	Note 4	
Output high voltage	$V_{OH}$	2.4		V	Note 4	Pins 2, 7 and 8 linked $V_{CC} = 4.95V$ $I_{OH} = 100\mu A$
Output low voltage	$V_{OL}$		0.5	V	Note 4	Pin 2 linked to 8 and 7 $I_{OL} = 1.6mA$
Set up time	$t_s$	14		ns	Note 3	25°C
Release time	$t_r$	20		ns	Note 3	25°C
Clock to output propagation time	$t_p$		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C

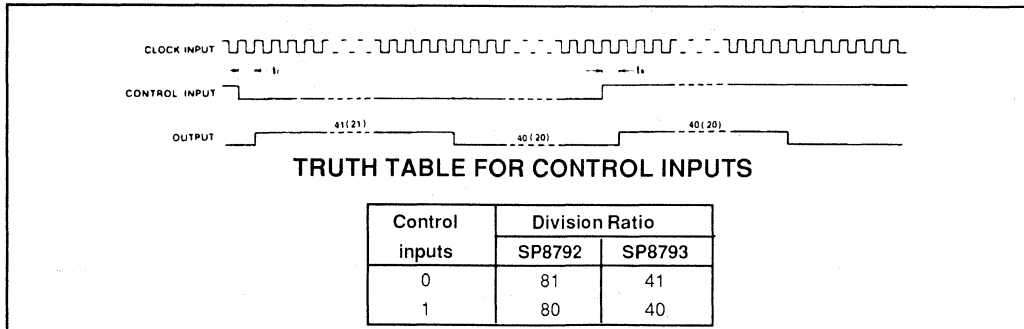
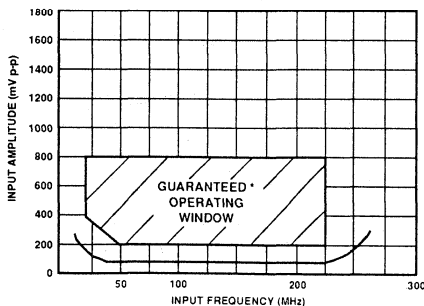


Figure 3 : Timing diagram SP8792/3

NOTES

The set-up time  $t_s$  is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure + 80 or 40 mode is selected.

The release time  $t_r$  is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure + 81 or 41 mode is selected.



\*Tested as specified  
in table of  
Electrical Characteristics

Figure 4 : Input sensitivity SP8792/SP8793

**SP8792/3**  
**OPERATING NOTES**

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/ $\mu$ s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.

5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

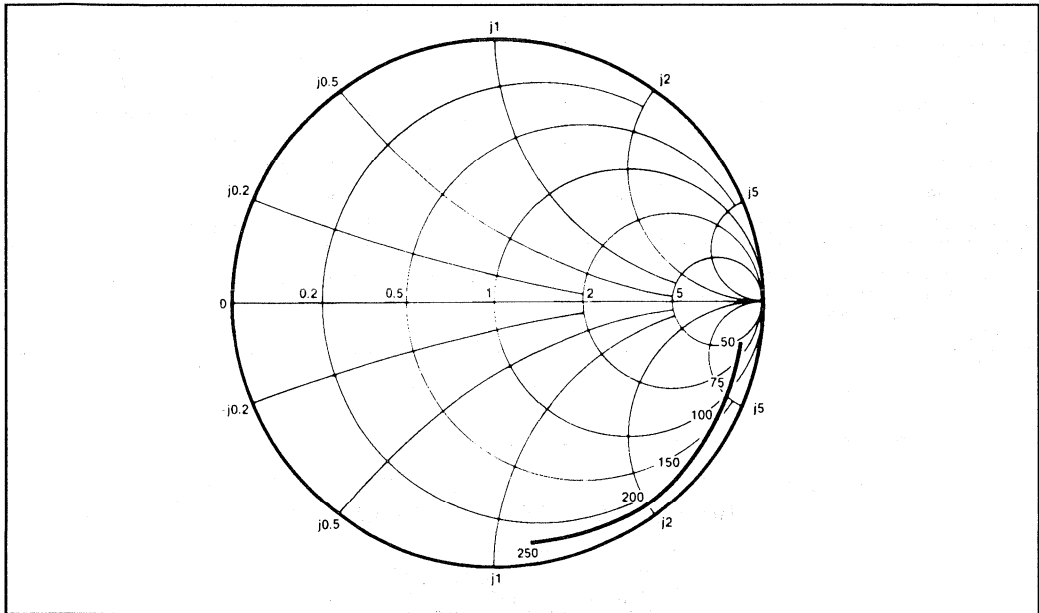


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

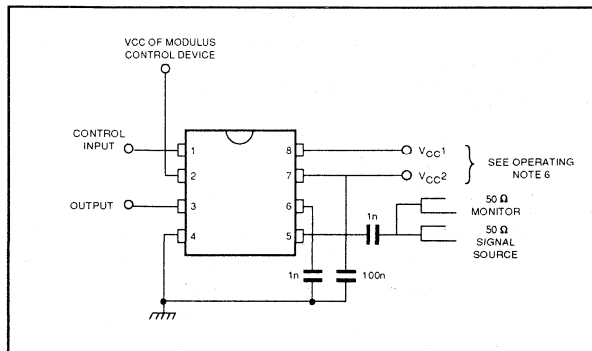


Figure 6 : Toggle frequency test circuit

# SP8795

## 225MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8789 is a low power programmable +32/33 counter. It divides by 32, when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

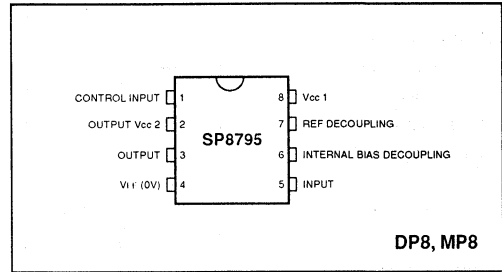


Figure 1 Pin connections - top view

### FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

### QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

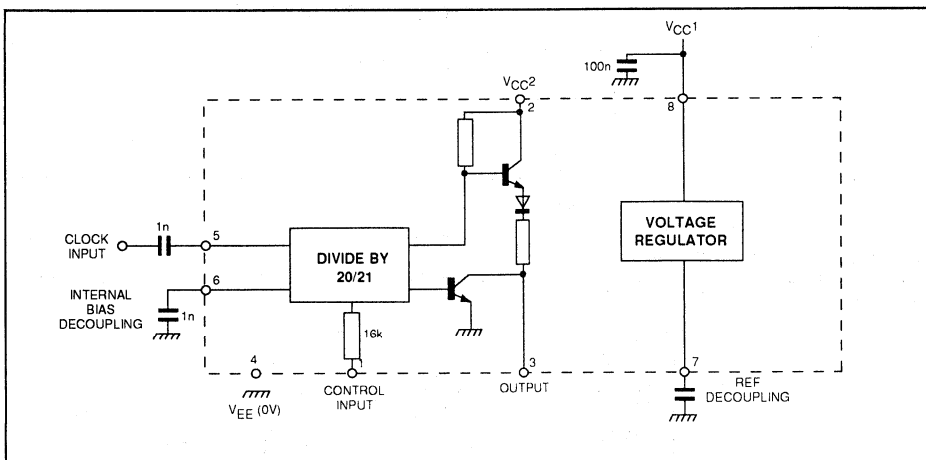


Figure 2 : Functional diagram SP8789

# SP8795

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage :  $V_{CC} 1 \ \& \ 2 = 5.2 \pm 0.25V$  or 6.8V to 9.5V (see Operating Note 7):

$V_{EE} = 0V$ ; Temperature  $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	$f_{max}$	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	$f_{min}$		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	$I_{EE}$		7	mA	Note 4	
Control input high voltage	$V_{INH}$	4		V	Note 4	
Control input low voltage	$V_{INL}$		2	V	Note 4	
Output high voltage	$V_{OH}$	2.4		V	Note 4	Pins 2, 7 and 8 linked $V_{CC} = 4.95V$ $I_{OH} = 100\mu A$
Output low voltage	$V_{OL}$		0.5	V	Note 4	Pin 2 linked to 8 and 7 $I_{OL} = 1.6mA$
Set up time	$t_s$	14		ns	Note 3	25°C
Release time	$t_r$	20		ns	Note 3	25°C
Clock to output propagation time	$t_p$		45	ns	Note 3	25°C

### NOTES

- Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
- The test configuration for dynamic testing is shown in Fig.6.
- Guaranteed but not tested.
- Tested only at 25°C

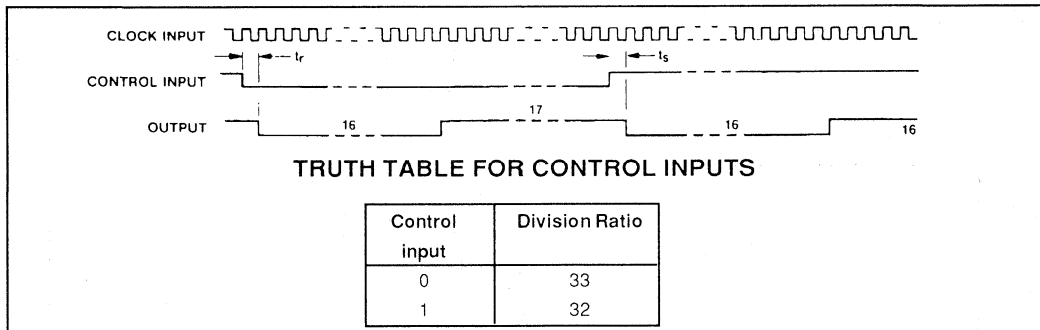
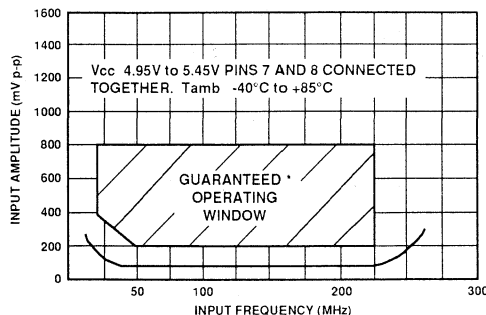


Figure 3 : Timing diagram SP8785

### NOTES

The set-up time  $t_s$  is defined as the minimum time that can elapse between a L  $\rightarrow$  H transition of the control input and the next L  $\rightarrow$  H clock pulse transition to ensure that the + 32 mode is selected.

The release time  $t_r$  is defined as the minimum time that can elapse between a H  $\rightarrow$  L transition of the control input and the next L  $\rightarrow$  H clock pulse transition to ensure that the + 33 mode is selected.



\*Tested as specified  
in table of  
Electrical Characteristics

Figure 4 : Input sensitivity SP8785



OPERATING NOTES

- 1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
- 2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
- 3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
- 4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.

- 5. Input impedance is a function of frequency. See Fig.5.
- 6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
- 7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

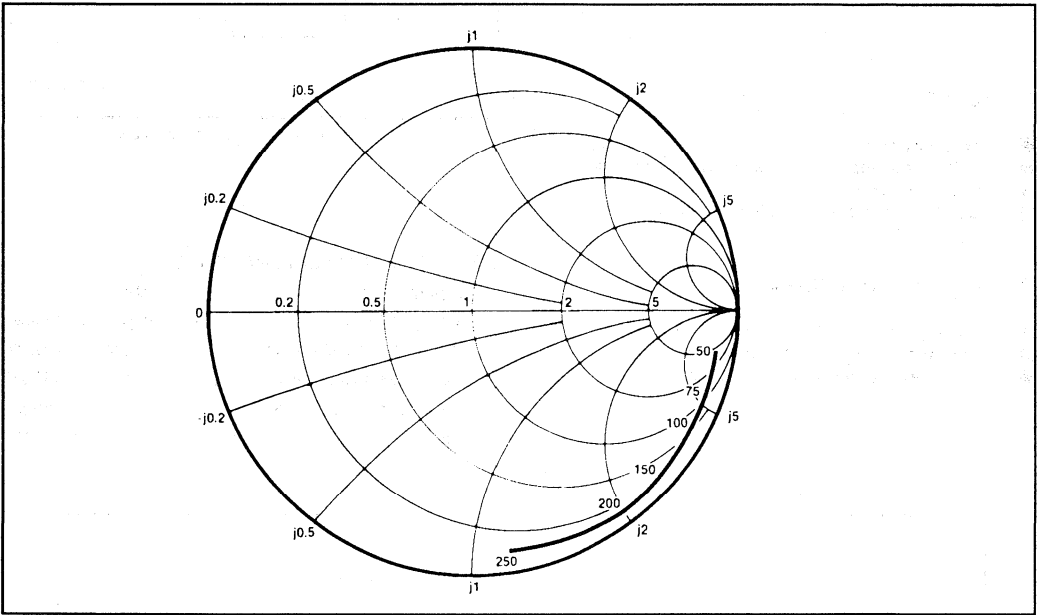


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

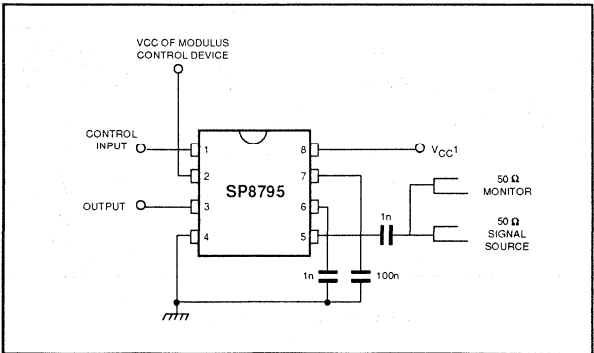


Figure 6 : Toggle frequency test circuit

# SP8799

## 225MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799 is a low power programmable +10/11 counter. It divides by 10, when the control input is in the high state and by 11 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

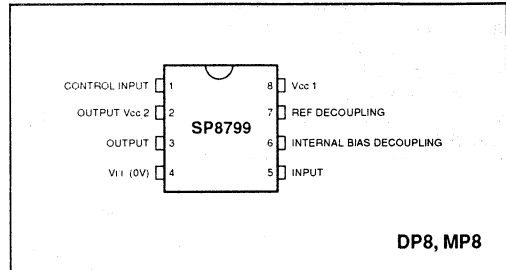


Figure 1 Pin connections - top view

### FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

### QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

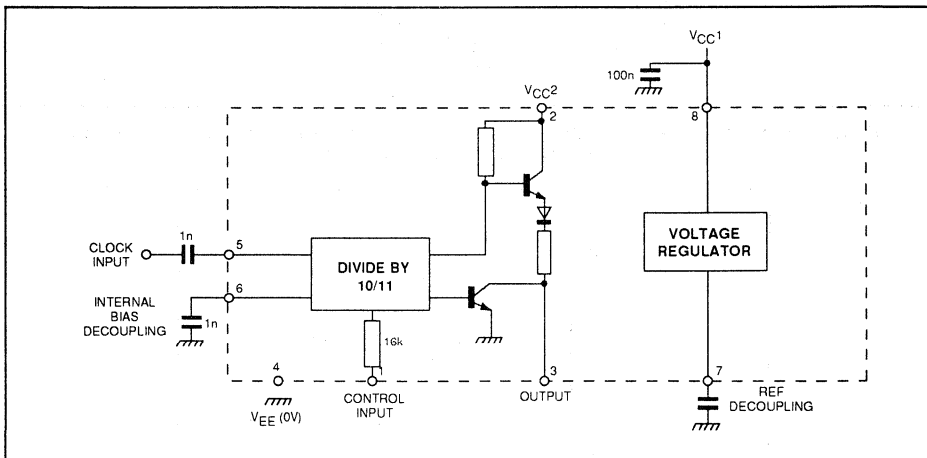


Figure 2 : Functional diagram SP8799

**ELECTRICAL CHARACTERISTICS**

**Test conditions (unless otherwise stated):]**

Supply voltage : Vcc 1 & 2 = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 7);

V<sub>EE</sub> = 0V; Temperature T<sub>amb</sub> = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f <sub>max</sub>	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f <sub>min</sub>		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I <sub>EE</sub>		7	mA	Note 4	
Control input high voltage	V <sub>INH</sub>	4		V	Note 4	
Control input low voltage	V <sub>INL</sub>		2	V	Note 4	
Output high voltage	V <sub>OH</sub>	2.4		V	Note 4	Pins 2, 7 and 8 linked V <sub>CC</sub> = 4.95V I <sub>OH</sub> = 100µA
Output low voltage	V <sub>OL</sub>		0.5	V	Note 4	Pin 2 linked to 8 and 7 I <sub>OL</sub> = 1.6mA
Set up time	t <sub>s</sub>	14		ns	Note 3	25°C
Release time	t <sub>r</sub>	20		ns	Note 3	25°C
Clock to output propagation time	t <sub>p</sub>		45	ns	Note 3	25°C

**NOTES**

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C

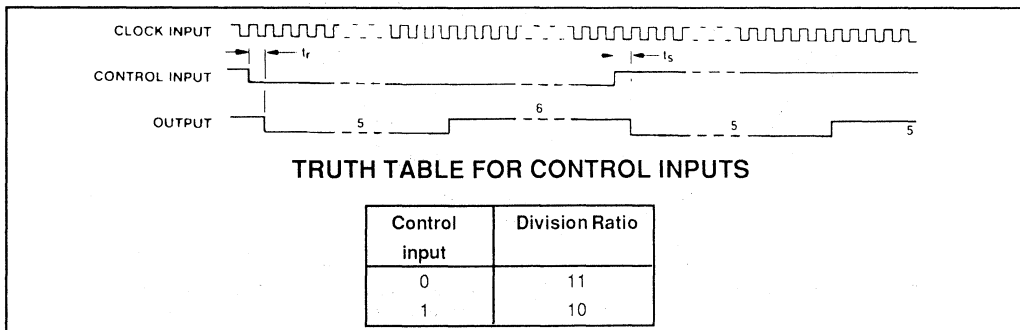
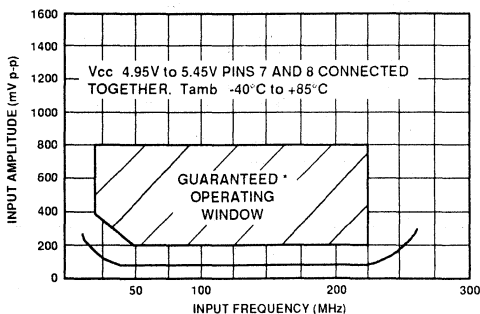


Figure 3 : Timing diagram SP8799

**NOTES**

The set-up time t<sub>s</sub> is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the → 10 mode is selected.

The release time t<sub>r</sub> is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the → 11 mode is selected.



\*Tested as specified in table of Electrical Characteristics

Figure 4 : Input sensitivity SP8799

# SP8799

## OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.

5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

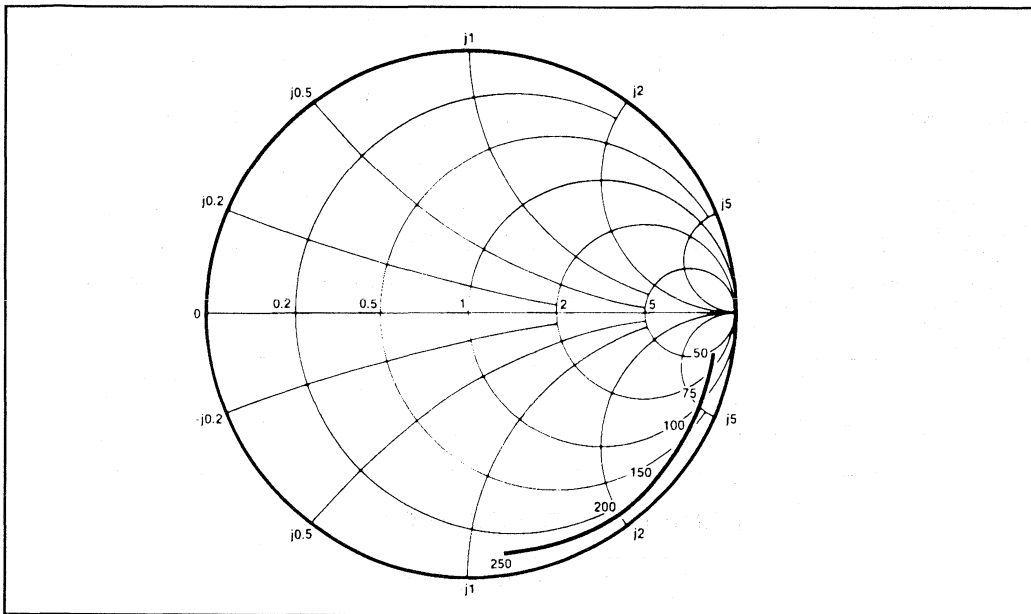


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

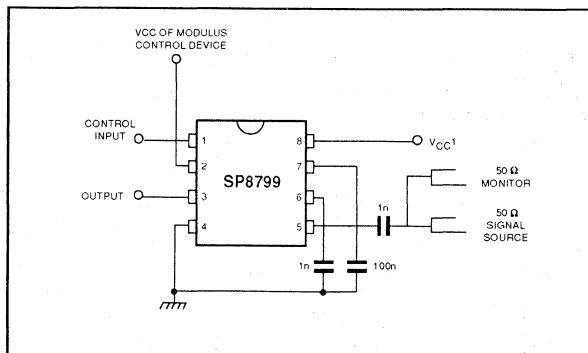


Figure 6 : Toggle frequency test circuit

# Section 4

## RF Front Ends



1. The first part of the text discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes that this is crucial for ensuring transparency and accountability in the organization's operations.

2. The second part of the text focuses on the role of the management team in setting clear goals and objectives. It highlights that effective communication and collaboration are essential for the success of any project or initiative.

3. The third part of the text addresses the need for regular monitoring and evaluation of progress. It suggests that this helps in identifying potential issues early on and allows for timely adjustments to be made.

4. The fourth part of the text discusses the importance of maintaining a positive and supportive work environment. It notes that this can significantly impact the productivity and morale of the staff.

5. The fifth part of the text concludes by reiterating the key points discussed and emphasizes the need for continuous improvement and learning from experience.

6. The sixth part of the text provides a summary of the main findings and recommendations. It suggests that these should be used as a guide for future actions and decisions.

7. The seventh part of the text offers some final thoughts and reflections on the overall process. It expresses optimism about the future and the potential for continued growth and success.

# SL6442

## 1GHZ AMPLIFIER/MIXER

(Supersedes May 1992 Edition)

The SL6442 UHF Amplifier and Mixer is designed for use in cordless telephones, cellular telephones, pagers and low-power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier (LNA) with AGC facility and two mixers for use in I and Q direct conversion receivers or image cancelling in superheterodyne receivers.

Operating from a single supply of 5V, the SL6442 requires a current of 4.6mA (typ.) when powered up and only 11µA (typ.) when powered down using the battery economy facility.

### FEATURES

- 1GHz Operation
- Very Low Power
- Suitable for Direct Conversion or Superhet Systems
- On-Chip RF Amplifier
- Power Down Facility for Battery Economy
- AGC Capability

### ORDERING INFORMATION

SL6442 NA MP Miniature Plastic DIL Package

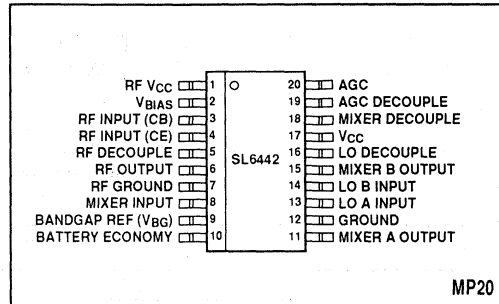


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	0°C to +70°C

This device has static-sensitive terminations, sensitivity measured as typically 400V using MIL-STD-883 Method 3015. Therefore, ESD handling precautions are essential in order to avoid degradation of performance or permanent damage to the device.

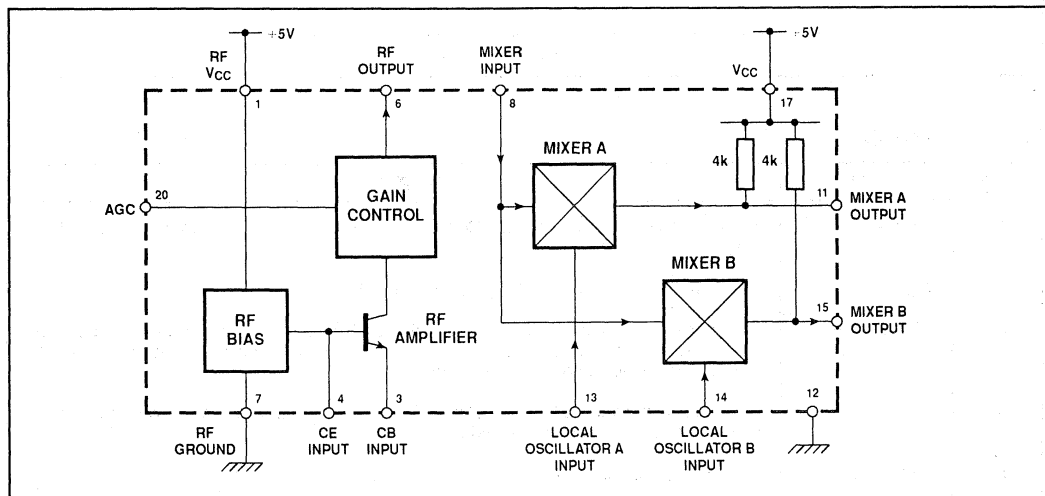


Fig.2 block diagram

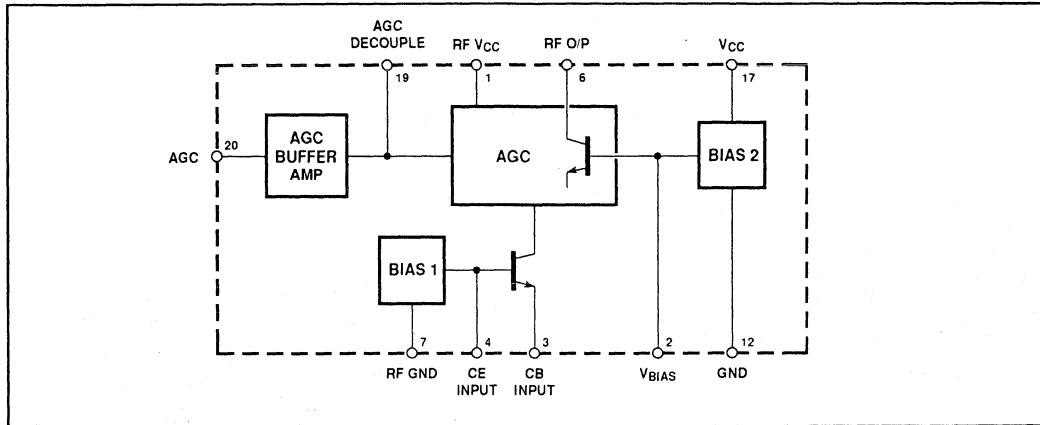


Fig.3 Circuit schematic of LNA

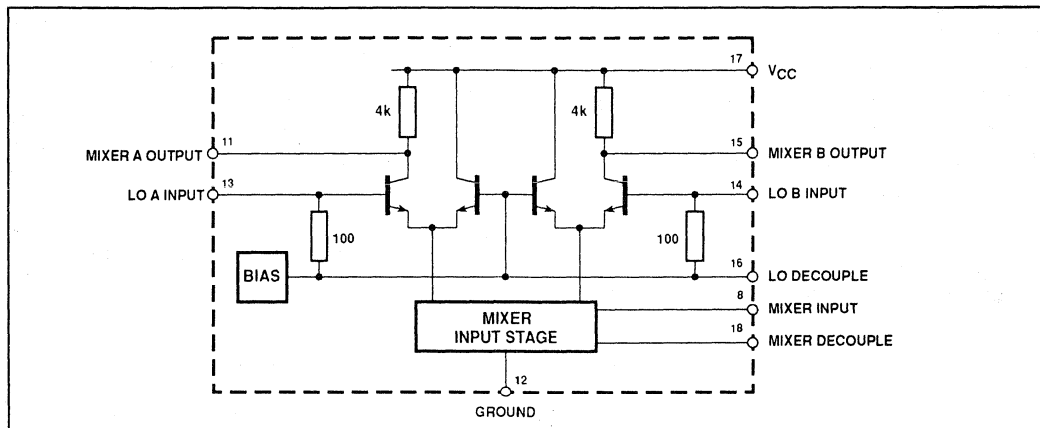


Fig.4 Circuit schematic of mixer

**PIN DESCRIPTIONS**

Pin no.	Name	Description
1	RF V <sub>CC</sub>	Power supply to the RF amplifier. Normally connected to +5V, it should be adequately bypassed.
2	V <sub>BIAS</sub>	A 1.6V bias source capable of supplying up to 0.5mA.
3	RF input (CB)	Common base input to the emitter of the RF transistor. It should be returned to ground for DC using an RF choke or tuned circuit when in common base mode. In common emitter mode it should be connected directly to ground.
4	RF input (CE)	Common emitter input to the base of the RF transistor. It is DC biased internally but should be decoupled in common base mode.
5	RF decouple	Decoupling of DC bias line.
6	RF output	Output port of the RF amplifier. It should be returned to +5V via an RF load. A current of 2mA will flow if pin 20 (AGC) is connected to pin 9 (V <sub>BG</sub> ).



## PIN DESCRIPTIONS (Continued)

Pin no.	Name	Description
7	RF ground	A separate ground is provided for the RF amplifier to improve stability.
8	Mixer input	This is coupled externally to the output of the RF amplifier (pin 6). It should be decoupled to $V_{BIAS}$ via an RF choke.
9	Bandgap ref. ( $V_{BG}$ )	Temperature compensated DC reference voltage. It should not be loaded.
10	Battery economy	Turns device 'off' when HIGH (>3V), 'on' when LOW (<1.5V).
11	Mixer A output	The output impedance is about 4k $\Omega$ ; quiescent voltage is approximately 4V ( $V_{CC}=5V$ ).
12	Ground	Mixer and biasing ground.
13	Local osc. A input	Input level of -10dBm. DC level is approximately 2.3V.
14	Local osc. B input	Input level of -10dBm. DC level is approximately 2.3V.
15	Mixer B output	The output impedance is about 4k $\Omega$ ; quiescent voltage is approximately 4V ( $V_{CC}=5V$ ).
16	LO decouple	Decoupling of DC bias line.
17	$V_{CC}$	+5V supply; it should be bypassed effectively.
18	Mixer decouple	Decoupling of DC bias line.
19	AGC decouple	Decoupling of AGC input line.
20	AGC	Varies RF amplifier gain. Gain reduces with increasing voltage, with RF gain reduced by 6dB when $AGC=V_{BIAS}$ . Full range of AGC requires only typically 300mV DC range (see Fig. 9). This pin should be connected to $V_{BG}$ if the AGC facility is not required.

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

$T_{AMB}=25^{\circ}C$ ,  $V_{CC}=4.5V$  and at  $V_{CC}=6.5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Total supply current	1, 6, 11, 15, 17	3.5	4.6	5.5	mA	Pin 10 at 0V
Total supply current (economised)	1, 6, 11, 15, 17		11.0	15.0	$\mu A$	Pin 10 at $V_{CC}$
Battery economiser input current	10	-1.0		+1.0	$\mu A$	
Total RF amplifier current	1, 5		2.0	2.75	mA	
Maximum RF amplifier current	6		2.0	2.75	mA	$V_{AGC}=1.2V$
Minimum RF amplifier current	6			10.0	$\mu A$	$V_{AGC}=2.0V$
AGC amplifier offset voltage	20, 19	-20.0	0	+20.0	mV	
Bandgap voltage, $V_{BG}$	9	1.00	1.23	1.40	V	
$V_{BIAS}$	2	1.40	1.64	1.80	V	
$V_{BIAS}$ supply regulation	2		+24.0	+50	mV	Step $V_{CC}$ from 4.50V to 5.50V,
$V_{BIAS}$ load regulation	2		-17.0	-50	mV	Step load from 0mA to 0.5mA,
Mixer conversion gain	11, 15	10.0	12.7	16.0	dB	$f_{CARRIER}=50MHz$ at -10dBm, $f_{SIGNAL}=50.01MHz$ at -34dBm, $IF=10kHz$ , $Z_L (EXT)=1M\Omega/20pF$
Mixer A/B gain match	11, 15	-1.0	0	+1.0	dB	$f_{CARRIER}=50MHz$ at -10dBm, $f_{SIGNAL}=50.01MHz$ at -34dBm, $IF=10kHz$ , $Z_L (EXT)=1M\Omega/20pF$

NOTE: Typical figures are for a  $V_{CC}$  of 5.0V

## ELECTRICAL CHARACTERISTICS OF THE SL6442 DEMONSTRATION BOARD (PAGES 8-10)

These characteristics are guaranteed over the following conditions unless otherwise stated:

$T_{AMB} = 25^{\circ}C$ ,  $V_{CC} = 5.0V$ ,  $V_{AGC} = V_{BG}$ ,  $LO = -5dBm$ , Input/Output =  $50\Omega$ ,  $f_{IN} = 950MHz$ ,  $f_{LO} = 930MHz$  (IF = 20MHz),  
 $f_{LO} = 949-990MHz$  (IF = 10kHz)

Overall performance	Typ.	Units	Conditions
Noise figure	8.3	dB	DSB (20MHz IF)
Third order input intercept	-22	dBm	20MHz IF
Power gain	7.5	dB	20MHz IF
Voltage gain	30	dB	$Z_L > 100k\Omega$ , IF = 10kHz

NOTE: Refer to Figs. 5, 6 and 7 for typical performance of overall low noise amplifier and mixer configuration (demonstration board) across temperature and supply voltage 4.0V, 5.0V and 7.0V.

## SUPPLEMENTARY INFORMATION

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		4.5	5.0	6.5	V	
<b>RF Amplifier Common emitter</b>						
Power gain	20		14		dB	Matched input and output.
AGC range			25		dB	$V_{BIAS} \pm 150mV$ typ. (see Fig. 9).
Input intercept			-9		dBm	Third order.
1dB gain compression			-23		dBm	At input
Noise figure			4.5		dB	Common emitter.
Input impedance						See Fig. 8.
Optimum operating frequency range	4	400		1000	MHz	
<b>Mixers (950MHz)</b>						
Voltage conversion gain			19		dB	At IF = 50kHz, matched input.
Power conversion gain			-7		dB	At IF = 20kHz. Matched input and output.
LO drive level	13,14		-10		dBm	Measured at pins 13 and 14.
Input intercept point	8		-6		dBm	Third order.
1dB gain compression			-12		dBm	At input
Mixer 'A' to Mixer 'B' gain input match				$\pm 1.0$	dB	Equal LO level at pins 13 and 14
Mixer 'A' to Mixer 'B' phase input match				$\pm 4$	deg	LO inputs $90 \pm 0.1^{\circ}$ phase
Input impedance						See Fig. 10.
Noise figure			21		dB	
Optimum operating frequency range	8			1000	MHz	Low frequency operation dependent on external components.
IF output bandwidth	11,15		20		MHz	Can be extended by external tuned circuit.
Output impedance			4		k $\Omega$	
Isolation LO to mix RF I/P		25			dB	All ports terminated with $50\Omega$
Reverse isolation of RF amp		14			dB	All ports terminated with $50\Omega$
Isolation LO to IF		50			dB	All ports terminated with $50\Omega$
Isolation RF to IF		37			dB	All ports terminated with $50\Omega$

**PERFORMANCE CHARACTERISTICS OF THE SL6442 DEMONSTRATION BOARD**

**Test conditions:**

Input frequency = 950MHz, LO frequency = 930MHz, LO amplitude = -5dBm, intermediate frequency = 20MHz,  
 $V_{AGC} = V_{BG}$ , input/output 50Ω matched.

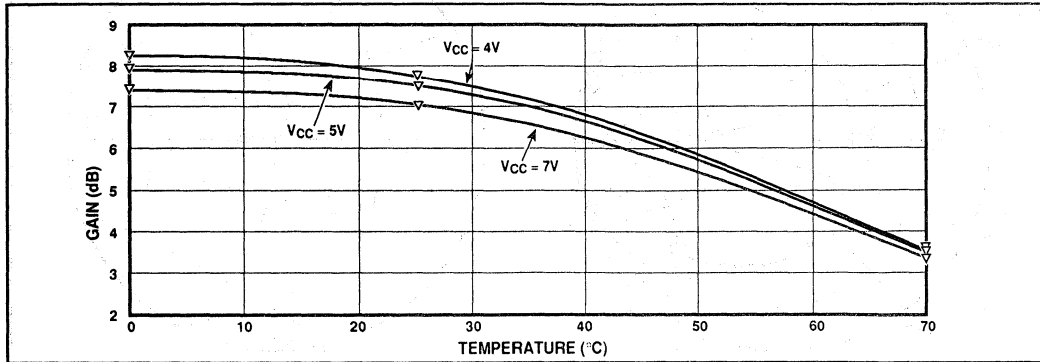


Fig. 5 Typical overall power gain

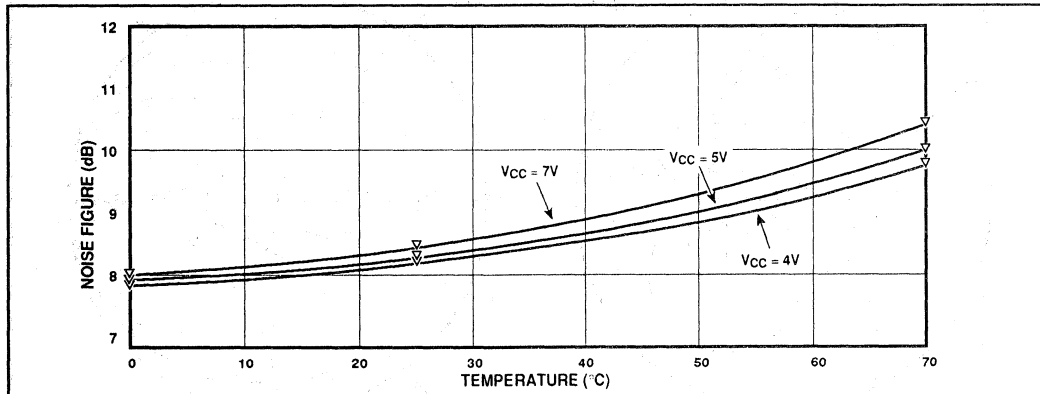


Fig. 6 Typical overall noise figure

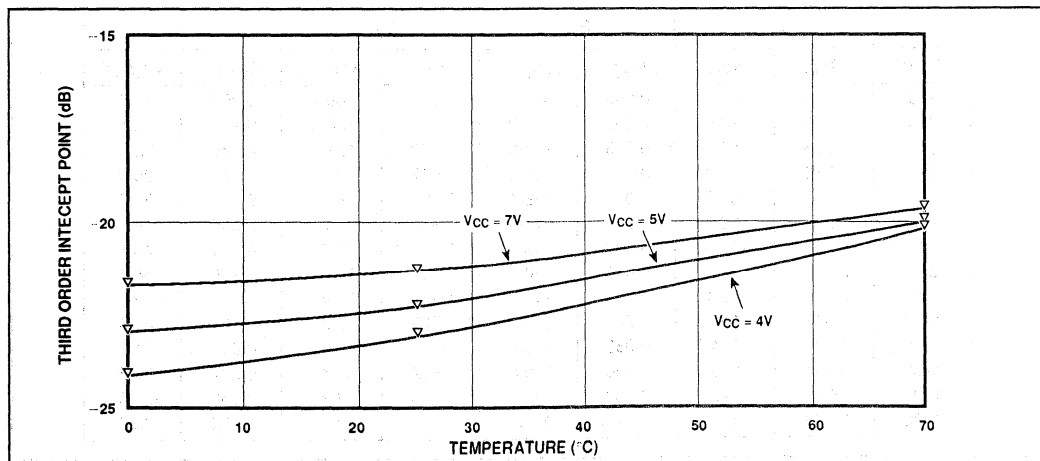


Fig. 7 Typical overall third order intercept

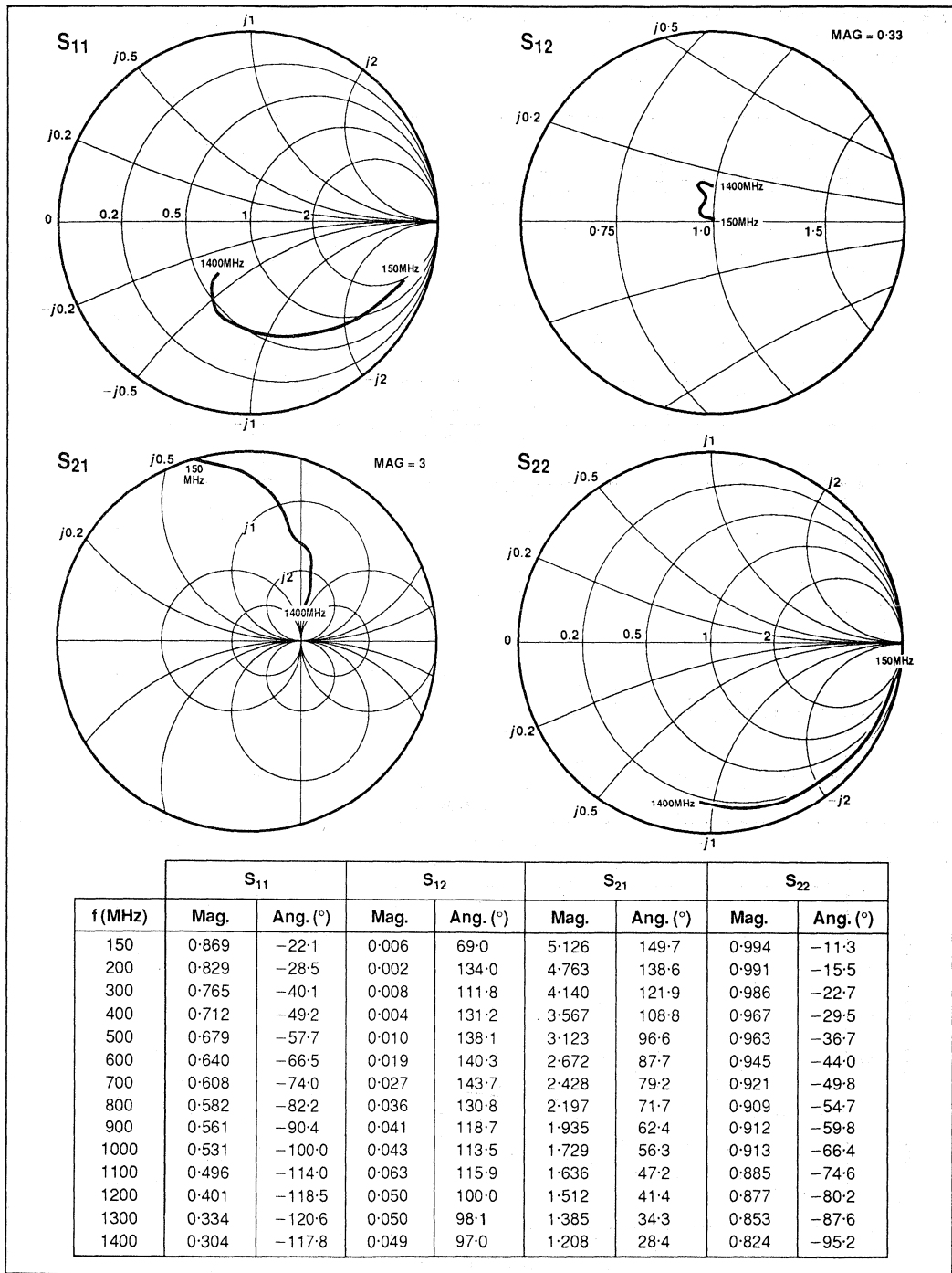


Fig. 8 RF amplifier common emitter S-parameters

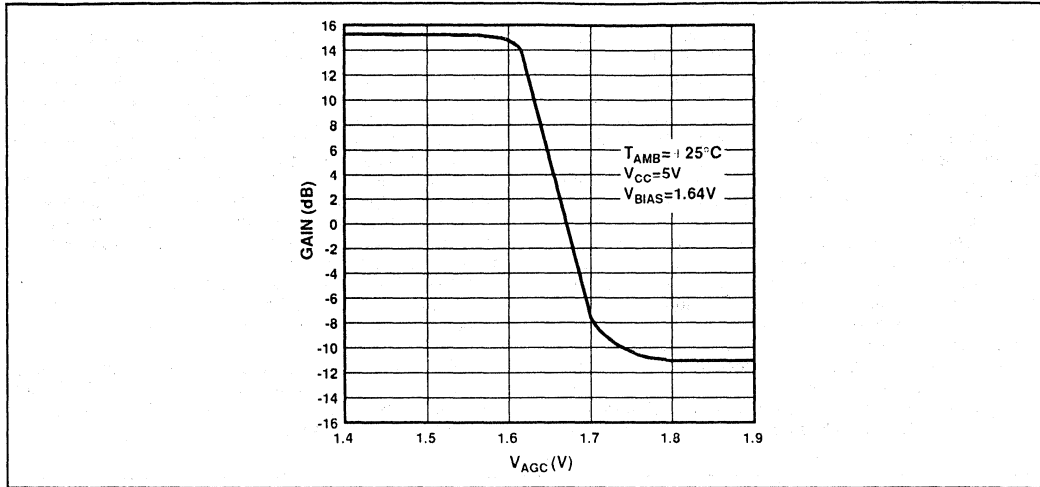


Fig. 9 SL6442 AGC characteristic

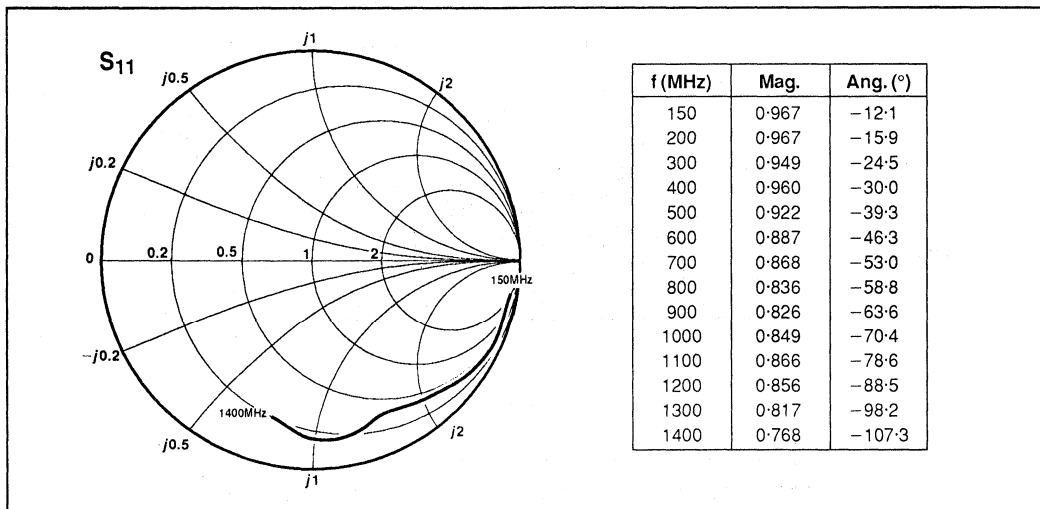


Fig. 10 Mixer RF input impedance,  $S_{11}$  (pin 8)

**APPLICATION CIRCUIT FOR USE AT 950MHz**

This Application Note describes a circuit which demonstrates the functions and performance of the SL6442 in a 950MHz amplifier/mixer receiver front end configuration.

Fig. 11 is a schematic diagram which illustrates the arrangement of the ancillary components required for optimum performance at 950MHz. Component layout, PCB track and ground plane are shown in Figs. 12, 13 and 14, respectively. Approximate starting values for the components were obtained using Smith charts and data derived from S-parameter analysis (see Figs. 8 and 10).

The actual component values were determined by using a linear circuit simulator such as Touchstone™. In this case the circuit is optimised for maximum stable gain and minimum input reflection coefficient at the required frequency.

The input match is achieved using a stripline shorted-stub network. The LNA output to mixer input match is achieved by using a series inductor, and the mixer output to 50Ω match consists of a tunable LC network.

To prevent possible RF instability, pin 2 (V<sub>BIAS</sub>) is decoupled with a series RC network as well as a 2·2μF capacitor.

The quadrature phase shift components consist of phase lead (R3, C18) and phase lag (R2, C17) networks, which are capacitively coupled to the LO input pins. Inductor L3 serves to resonate out the parasitic capacitance between the two ports.

The exact values of the phase shift components were determined empirically and achieve a maximum amplitude and phase imbalance of about 1dB and 4 degrees respectively.

The variable capacitors VC1 and VC2 are adjusted to give a maximum output level at an IF of 20MHz. Other intermediate frequencies may require different values of VC1 and VC2 and/or L4 and L5. At zero IF, as in direct conversion receivers, the output matching network is transparent.

If the AGC facility is not required it is necessary to connect pin 20 to pin 9 (V<sub>BG</sub>). The battery economy pin (10) may be connected directly to ground if the power down facility is not required.

*NOTE: Ensure adequate decoupling is used close to the chip, especially when designing for maximum power gain. Refer to LNA S-parameters to avoid possible stability problems when designing the LNA close to maximum gain.*

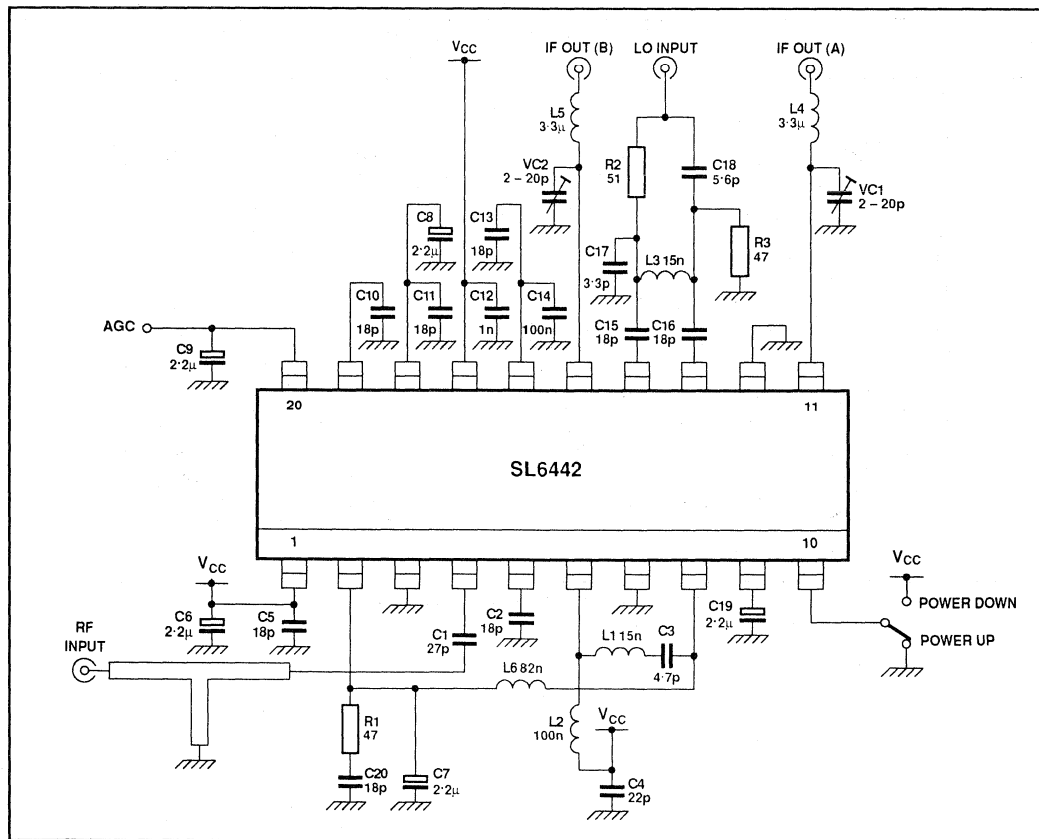


Fig. 11 SL6442 demonstration board circuit

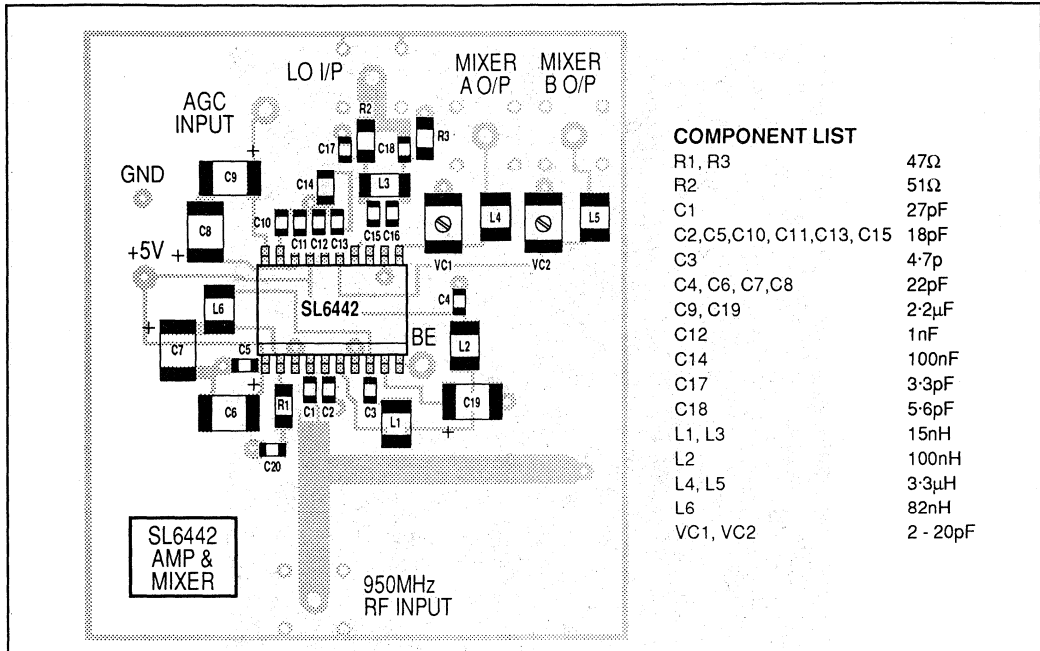


Fig. 12 SL6442 demonstration board component layout. Scale=2 x full size. Input and output coaxial connectors are mounted on the ground plane side of the board.

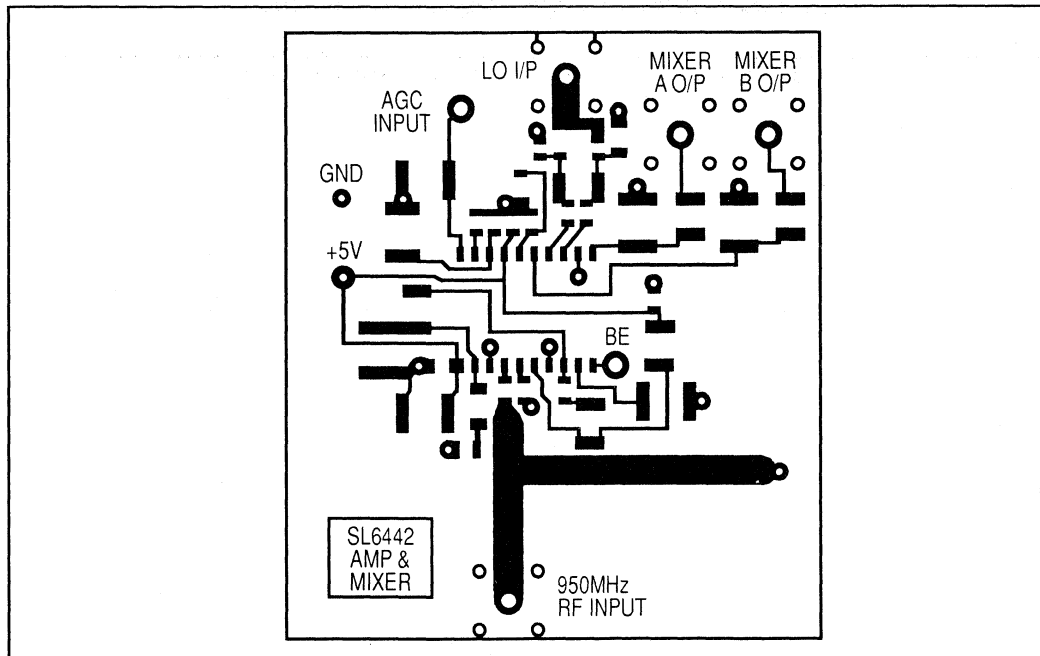


Fig. 13 SL6442 demonstration board track. Scale=2 x full size

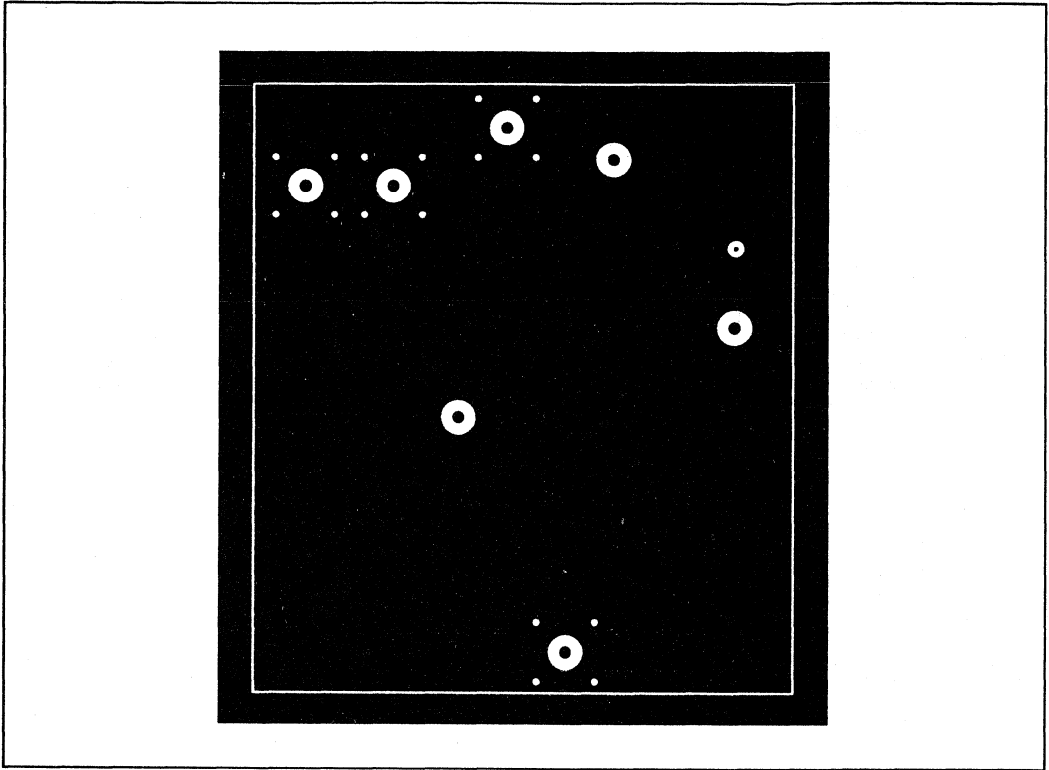


Fig. 14 SL6442 demonstration board ground plane. Scale=2 x full size.



# SL6444

## 1GHz AMPLIFIER / MIXER

The SL6444 Amplifier and Mixer is designed for use in Cordless Telephones, Cellular Radios, Pagers and Low Power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier and mixer. Operating from a single supply it draws a current of 9.5mA and has a power down facility.

### FEATURES

- 1GHz Operation
- Low Power Consumption
- Low Noise Figure
- Suitable for Superheterodyne Architectures
- Power Down Facility for Battery Economy
- Balun for Balanced Mixer Drive

### ORDERING INFORMATION

SL6444 KG MPAS Miniature Plastic DIL Package

NOTE. This device has static sensitive terminations, sensitivity typically measured as 200V using MIL-STD-883 method 3015. ESD handling precautions are essential to avoid degradation of performance or permanent damage to this device.

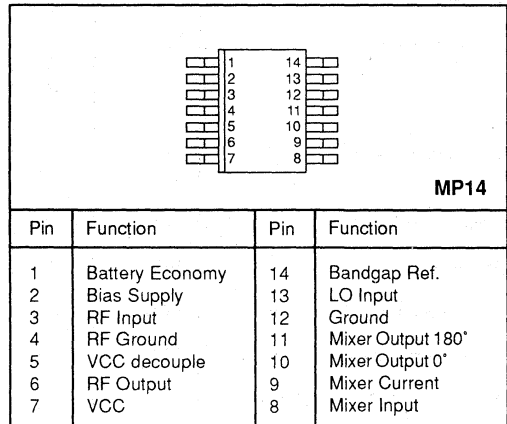


Fig. 1 Pin connections - top view

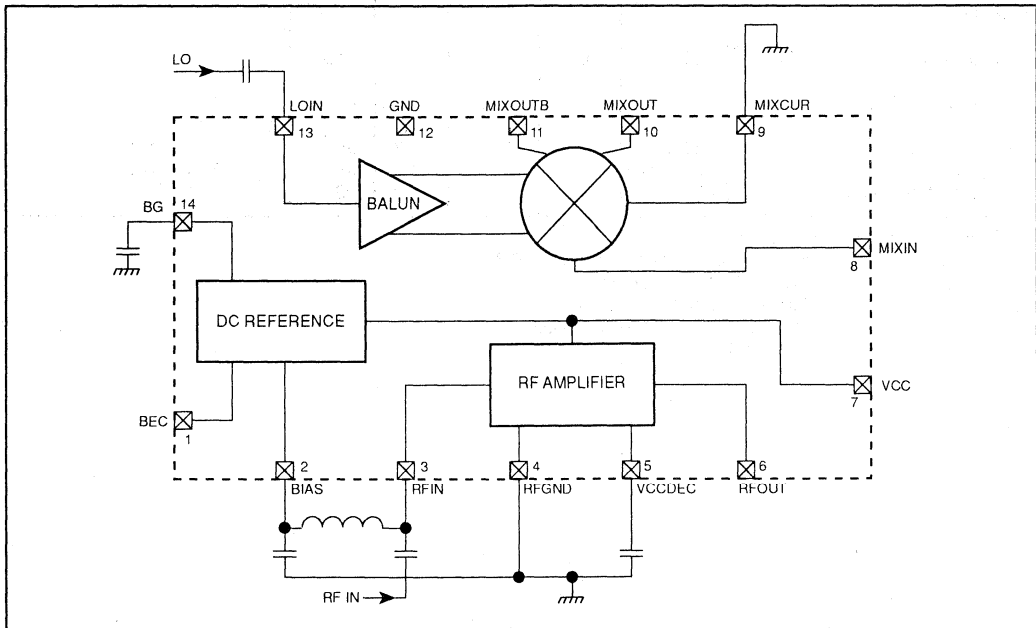


Fig. 2 Block diagram

# SL6444

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated.

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  and at  $V_{CC} = 6.0\text{V}$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
<b>DC CHARACTERISTICS</b>						
Supply voltage	$V_{CC}$	2.7	5.0	6.0	V	
Supply current, $I_{CC}$ Note 1		7.0	7.8	8.5	mA	Battery economy low $V_{CC} = 2.7$ Battery economy low $V_{CC} = 6.0$ Battery economy high
		8.7	9.7	10.7	mA	
			0.5	1.0	$\mu\text{A}$	
Bandgap reference	VBG	1.15	1.17	1.20	V	No external load $V_{CC} = 2.7$
	VBG	1.19	1.22	1.25	V	No external load $V_{CC} = 6.0$
Battery economy high	BEC	$V_{CC}-0.5$		$V_{CC}$	V	
Battery economy low	BEC	0		0.5	V	
Battery economy sink current	BEC		0.1	2.0	$\mu\text{A}$	Battery economy high
Battery economy source current	BEC		1.0	2.0	$\mu\text{A}$	Battery economy low
<b>RFAMPLIFIER (COMMON EMITTER)</b>						
Supply current	RFOUT	2.1	2.5	2.8	mA	$V_{CC} = 6.0\text{V}$
<b>MIXER</b>						
Optimum frequency range	MIXIN	0.1			GHz	
Supply current Note 2.		3.5	3.9	4.3	mA	$V_{CC} = 2.7$ $V_{CC} = 6.0\text{V}$
		4.2	4.6	5.0	mA	
Mixer conversion	MIXOUT	10.3	11.0	11.7	dB	$V_{CC} = 6.0\text{V}$ Note 3
Voltage gain	MIXOUTB	10.0	10.6	11.2	dB	$V_{CC} = 2.7\text{V}$ Note 3
Mixer output gain match				-/+ 0.5	dB	

NOTES: (1) Total device supply current

(2) Half mixer current in each of MIXOUT and MIXOUTB

(3) conditions:-  
 $LOIN = 100\text{MHz}$ ,  $-15\text{dBm}$   
 $MIXIN = 100.01\text{MHz}$ ,  $-30\text{dBm}$   
 $MIXOUT$  and  $MIXOUTB$   $470\Omega$  load  
 $IF = 10\text{kHz}$

**TYPICAL ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed by design.

$T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 5$  Volts.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
<b>RF AMPLIFIER (COMMON EMITTER)</b>						
Input Impedance						50Ω system see fig 3
Output Impedance						50Ω system see fig 3
Gain (RF <sub>IN</sub> to RF <sub>OUT</sub> )						50Ω system see fig 3
Reverse isolation (RF <sub>IN</sub> to RF <sub>OUT</sub> )						50Ω system see fig 3
<b>MIXER</b>						
Input Impedance						50Ω system see fig 4
Output Impedance						50Ω system see fig 4

**PERFORMANCE CHARACTERISTICS (GPS Demonstration boards)**

Test conditions (unless otherwise stated):  $V_{CC} = 2.7\text{V}$ ;  $T_{amb} = 25^{\circ}\text{C}$

Input frequency 915MHz; Local oscillator frequency 765MHz;

Intermediate frequency 150MHz; Local oscillator amplitude 80mV r.m.s.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
<b>RF AMPLIFIER COMMON EMITTER (NOTE 1)</b>						Application circuit Fig. 5
Power gain			16		dB	
Third order intercept point			-12		dBm	At input
Noise figure			2.7		dB	
Output power at 1dB gain compression			-6		dBm	
<b>SINGLE BALANCED MIXER (Note 1)</b>						Application circuit Fig. 6
Power conversion gain			4.5		dB	
Third order intercept point			-5.5		dBm	At input
Double sideband noise figure			10		dB	
LO to RF isolation			28		dB	
LO to IF isolation			39		dB	

## SL6444

### PERFORMANCE CHARACTERISTICS (GPS Demonstration boards) continued

Test conditions (unless otherwise stated): VCC = 2.7V; T<sub>amb</sub> = 25°C

Input frequency 915MHz; Local oscillator frequency 765MHz;

Intermediate frequency 150MHz; Local oscillator amplitude 80mV r.m.s.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
RF to IF isolation			18		dB	Application circuit Fig. 7
<b>DOUBLE BALANCED MIXER (Note 1)</b>						
Power conversion gain			10			At input
Third order intercept point			-8		dBm	
Double sideband noise figure			10		dB	
LO to RF isolation			26		dB	
LO to IF isolation			42		dB	
RF to IF isolation			32		dB	

#### NOTE.

1. Application circuits have been optimised for minimum noise figure and maximum gain. Typical performance across temp at 2.7V and 6.0V are shown in graphs 1 to 6.

#### ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to + 150°C
Operating temperature	-10°C to + 85°C

PIN NO	NAME	TITLE	DESCRIPTION
1	BEC	Battery Economy	Turns device OFF when "HIGH", on when "LOW".
2	BIAS	Bias Supply	Controls the bias current in the RF amplifier. Must be decoupled externally to ground through 1nF capacitor.
3	RFIN	RFInput	This is the common emitter input to the base of the RF transistor. It is DC biased externally through a suitable inductor to the bias pin, pin 2.
4	RFGND	R.F. Ground	Must be connected to the system ground with minimum inductance.
5	VCCDEC	VCC Decouple	This pin allows the VCC supply at the RF Amplifier to be effectively decoupled.
6	RFOUT	RF Output	The collector of the RF amplifier output transistor. Must be returned to VCC through a load in which the DC bias current can flow.
7	VCC	Power Supply	Positive supply.
8	MIXIN	Mixer Input	Input port of mixer, should be AC coupled externally.
9	MIXCUR	Mixer Current	A resistor may be placed between this pin and ground to reduce mixer current. Otherwise connect to GND.
10	MIXOUT	Mixer Output 0°	Output port of the mixer. An open collector output which must be returned to VCC through a suitable load. Half of the total Mixer current will flow from this port.
11	MIXOUTB	Mixer Output 180°	Output port of the mixer. An open collector output which must be returned to VCC through a suitable load. Half the total mixer current will flow from this port.
12	GND	Ground	Must be connected to the system ground with minimum inductance.
13	LOIN	LO Input	Local Oscillator input to mixer, should be AC coupled externally.
14	VBG	Bandgap	Temperature compensated voltage reference. Must be decoupled externally to ground through a 1nF capacitor.

# SL6444

VCC = 5V Amplifier current 2.2mA

FREQ-MHz	MAG[S11]	ANG[S21]	MAG [S21]	ANG [S21]	MAG [S12]	ANG [12]	MAG [S22]	ANG [S22]
100.000	0.91	-10	5.89	167	0.016	158	0.99	-5
200.000	0.89	-21	5.86	151	0.010	-75	0.99	-11
300.000	0.86	-30	5.60	136	0.004	55	0.99	-16
400.000	0.81	-39	5.19	121	0.003	118	0.98	-21
500.000	0.77	-47	4.86	108	0.004	-102	0.97	-25
600.000	0.72	-55	4.48	95	0.005	154	0.98	-32
700.000	0.67	-63	4.11	84	0.004	134	0.97	-38
800.000	0.62	-70	3.73	73	0.008	165	0.97	-44
900.000	0.58	-77	3.35	61	0.008	150	0.94	-52
1000.000	0.55	-83	2.97	52	0.010	117	0.91	-59
1100.000	0.52	-87	2.64	43	0.014	97	0.87	-66
1200.000	0.49	-92	2.32	34	0.013	82	0.82	-73
1300.000	0.47	-95	2.06	28	0.010	78	0.76	-79
1400.000	0.45	-98	1.85	22	0.009	59	0.71	-85
1500.000	0.45	-101	1.71	16	0.004	80	0.67	-89

SL6444 Typical RF Amplifier scattering parameters

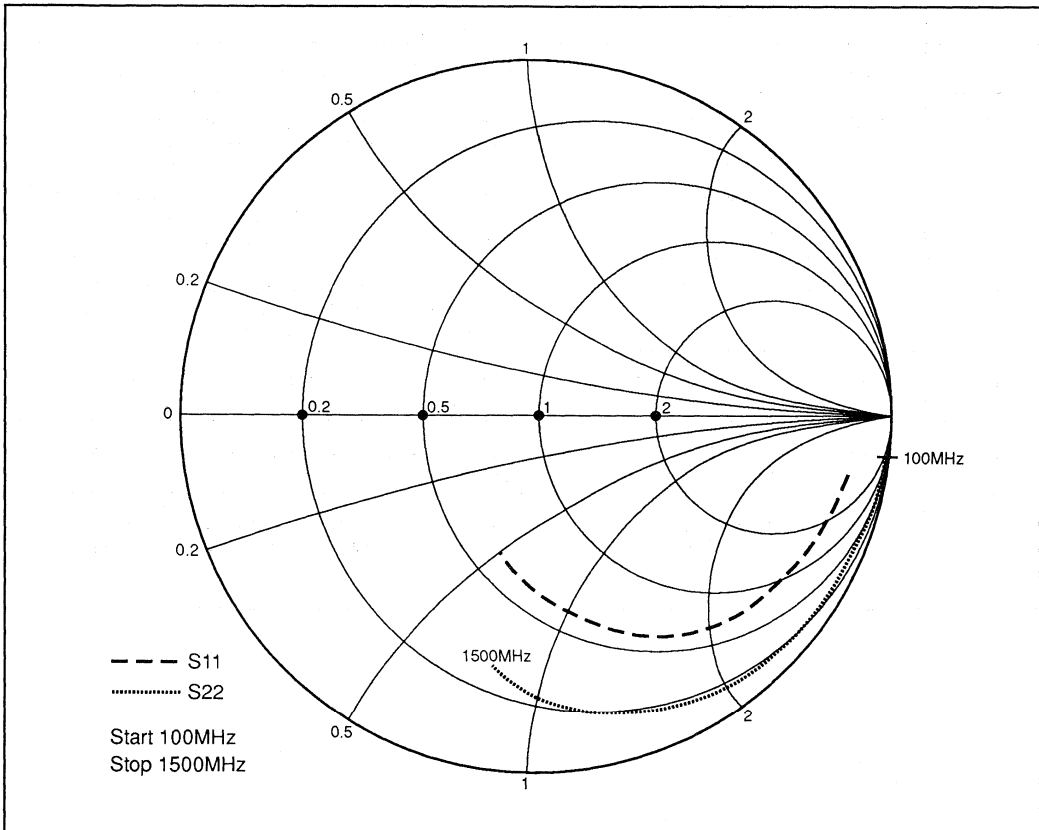


Fig. 3 Typical Input and Output Impedance of SL6444 RF Amplifier (Normalised to 50Ω)

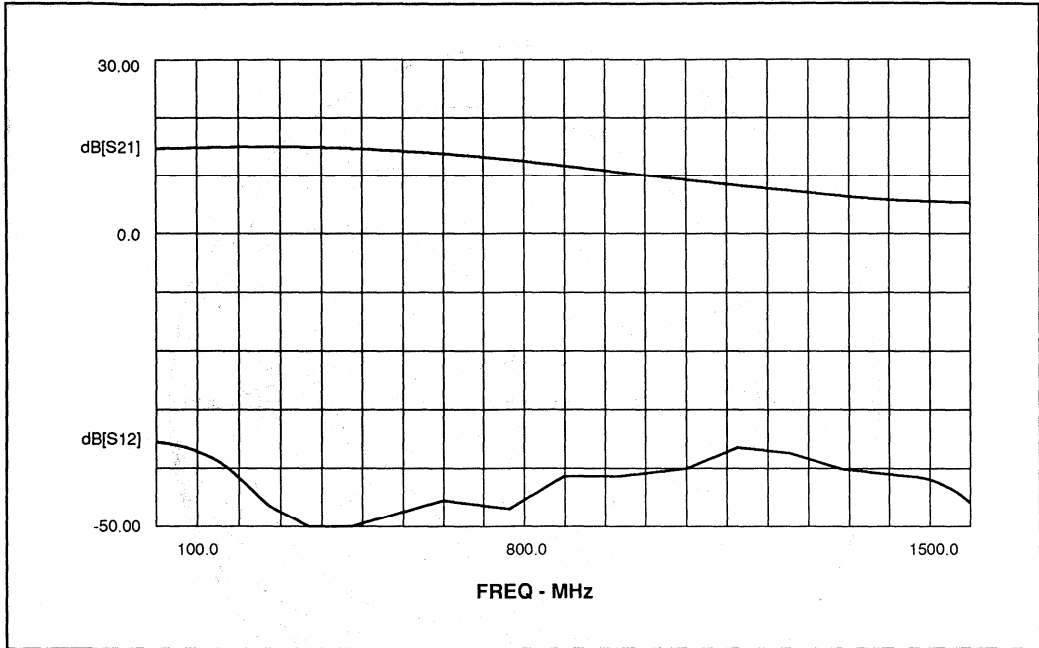


Fig. 3b Typical gain and reverse isolation of SL6444 RF Amplifier in a 50 Ohm test system

VCC = 5V Mixer current 4.4mA. S22 is measured at either MIXOUT or MIXOUTB. S11 is measured at MIXIN.

FREQ-MHz	MAG[S11]	ANG[S11]	MAG [S22]	ANG [S21]
100.000	0.79	-6	1.00	-6
200.000	0.78	-13	0.99	-12
300.000	0.77	-20	0.99	-16
400.000	0.76	-28	0.97	-22
500.000	0.77	-34	0.96	-28
600.000	0.78	-41	0.97	-35
700.000	0.70	-50	0.94	-40
800.000	0.70	-58	0.91	-47
900.000	0.68	-67	0.88	-54
1000.000	0.64	-76	0.86	-60
1100.000	0.61	-86	0.83	-67
1200.000	0.58	-95	0.79	-74
1300.000	0.55	-105	0.75	-82
1400.000	0.51	-117	0.71	-89
1500.000	0.49	-129	0.68	-96

SL6444 Typical Mixer port impedance

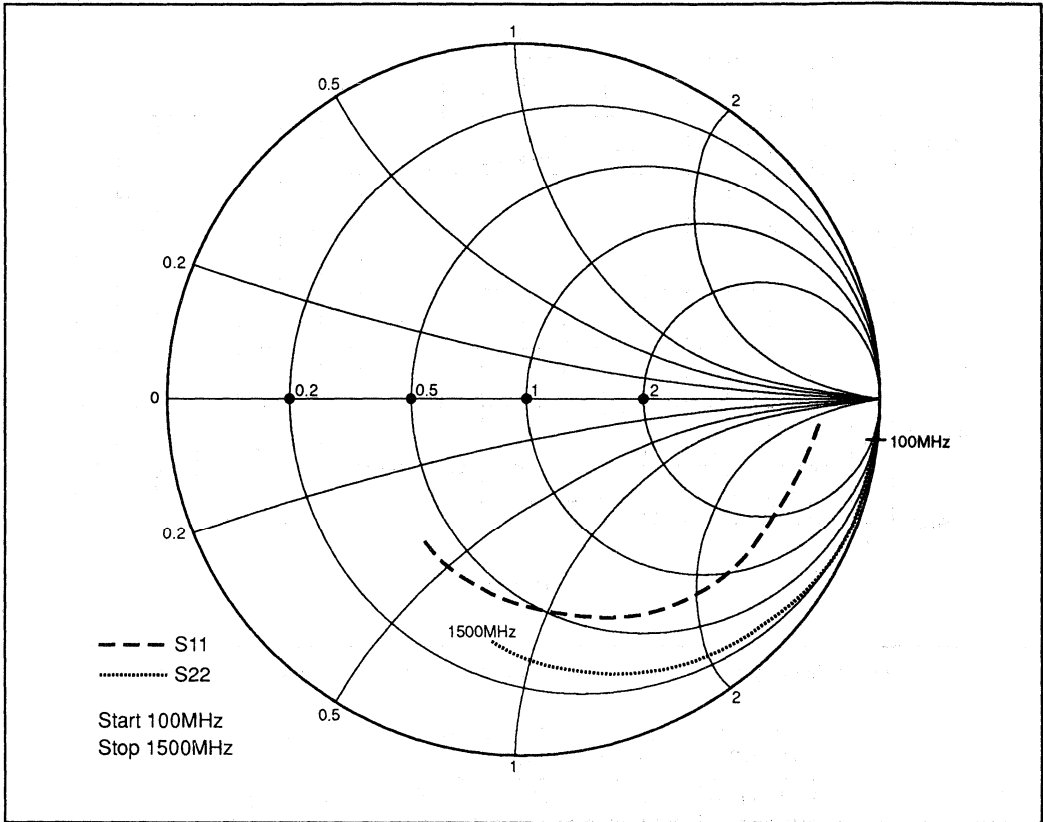
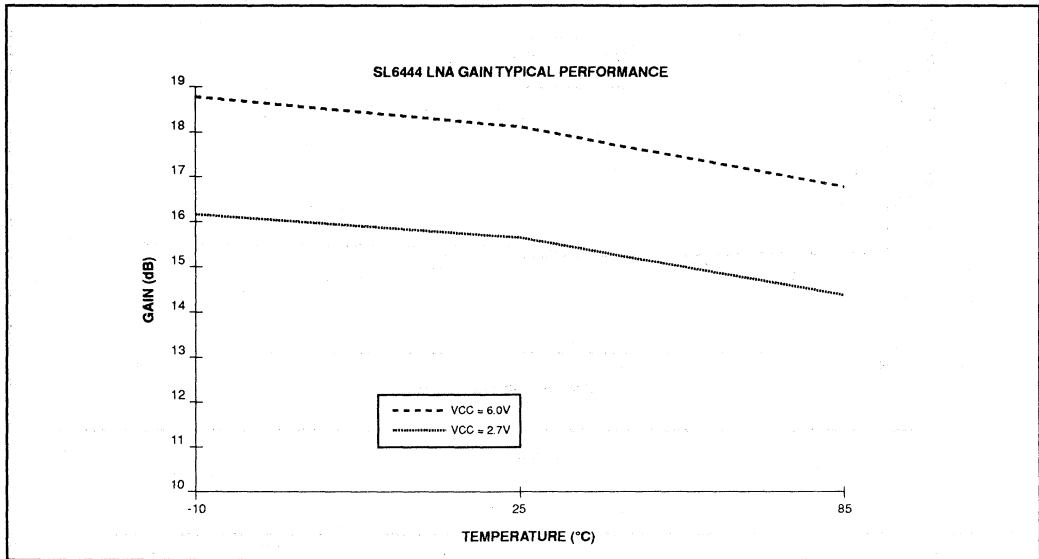


Fig. 4 Typical Input and Output Impedance of SL6444 Mixer (Normalised to 50Ω)

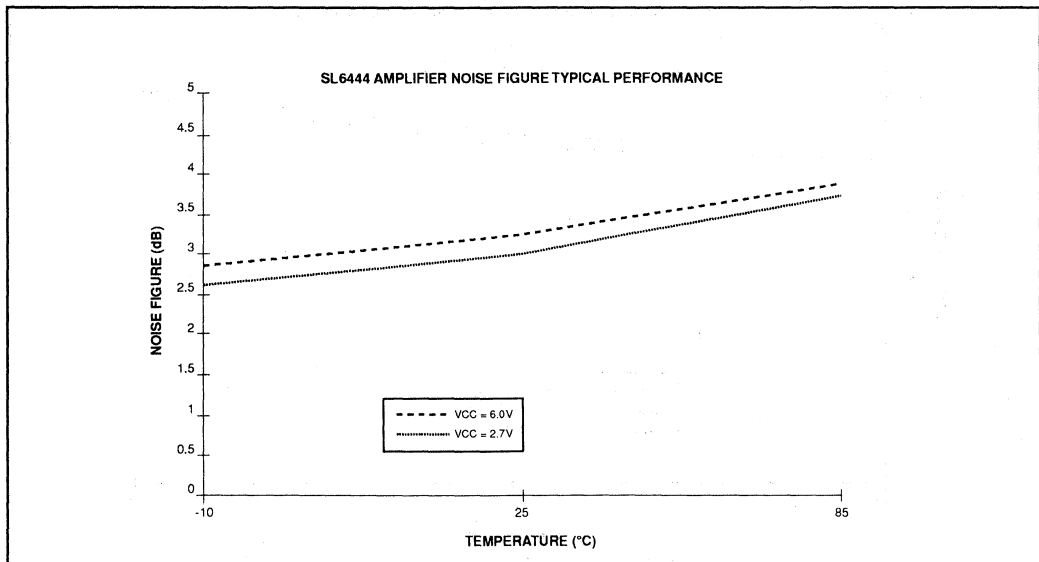


**PERFORMANCE CHARACTERISTICS (GPS Demonstration boards)**

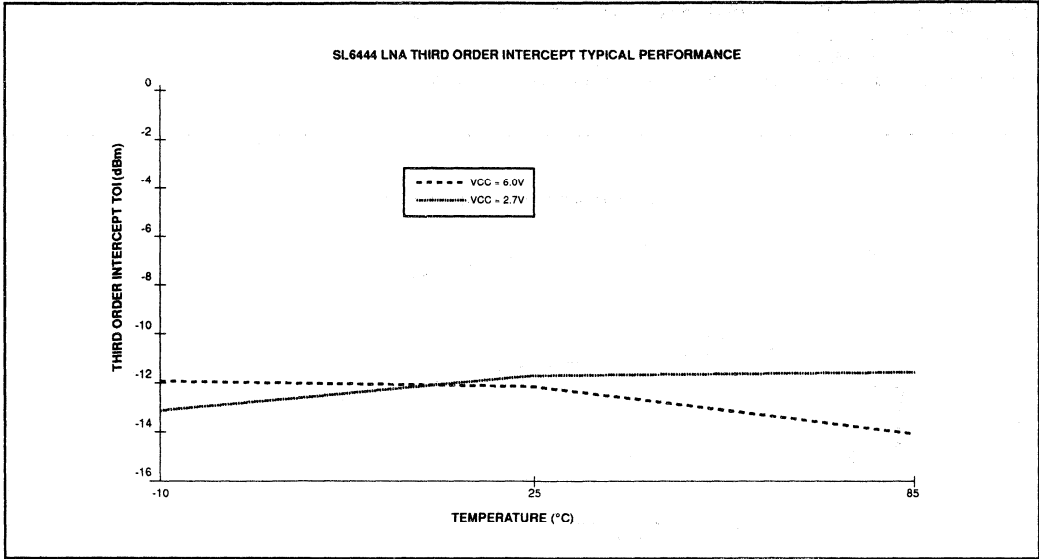
Test conditions (unless otherwise stated)  
 Input frequency 915MHz; Local oscillator frequency 765MHz;  
 Intermediate frequency 150MHz; Local oscillator amplitude 80mV r.m.s.



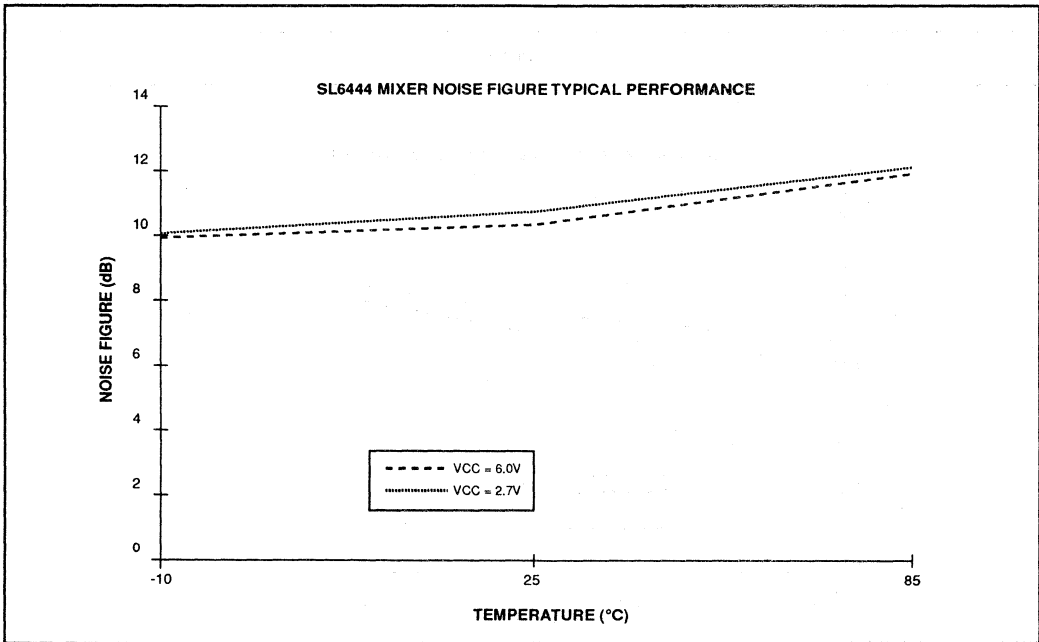
Graph 1



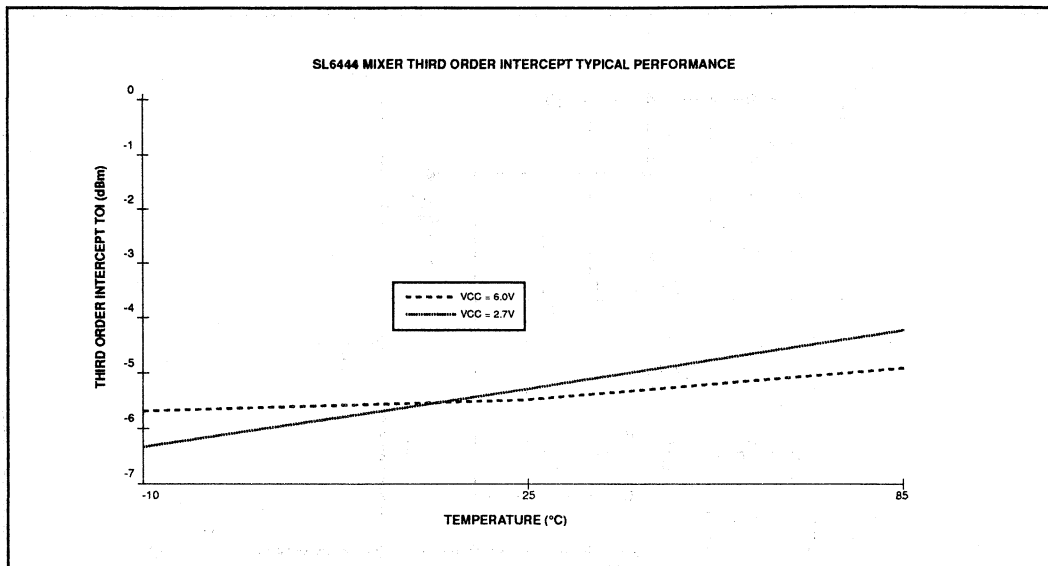
Graph 2



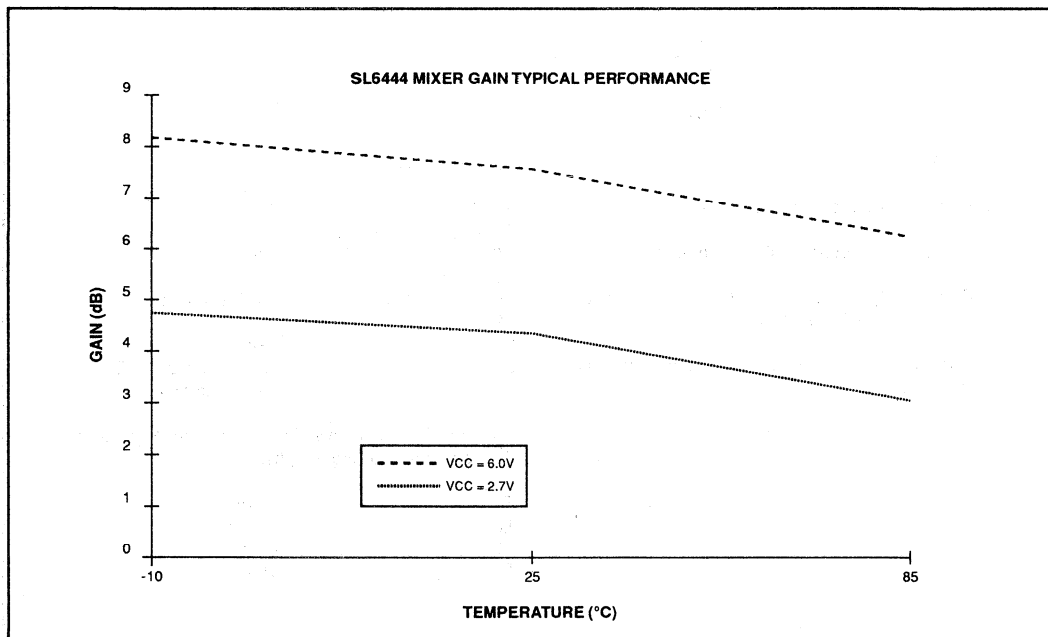
Graph 3



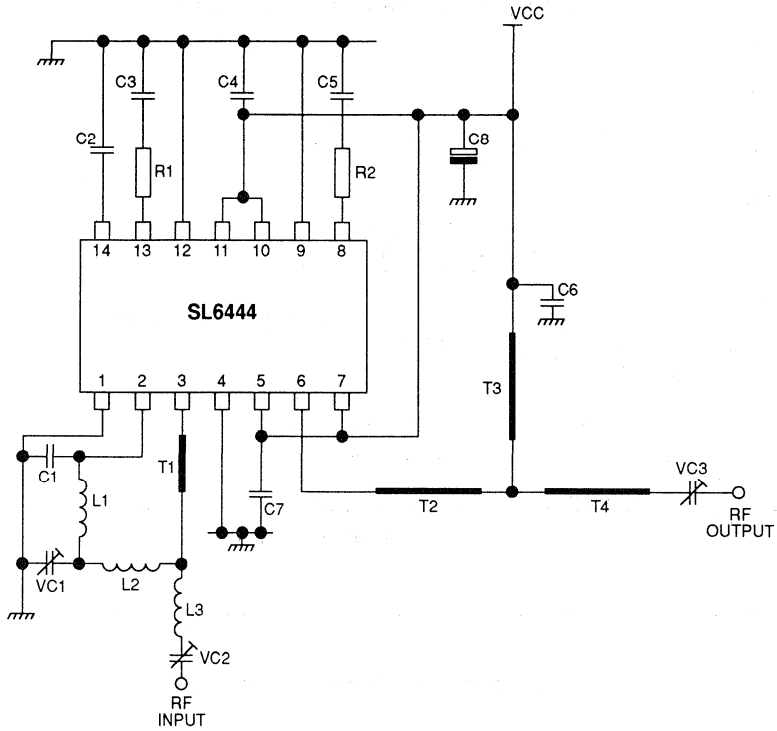
Graph 4



Graph 5



Graph 6



NOTES

1. Double sided board should be used
2. Low inductive resistors should be used
3. Good quality capacitors with high self resonant frequency should be used
4. Components should be placed in close proximity to device

COMPONENT LIST

R1, R2	47 Ohm
C1, C2, C3, C4, C5, C7	1nF
C6	270pF
C8	1μF
VC1, VC2, VC3	20pF Trimmer
L1	56nH
L2	39nH
L3	6nH 1 Turn 24SWG 8mm diameter

Microstrip lines 0.5mm wide on 1.6mm thick glass fibre PCB and the following lengths.

T1	5mm
T2	16mm
T3	8mm
T4	15mm

Fig. 5 SL6444 RF amplifier demonstration circuit

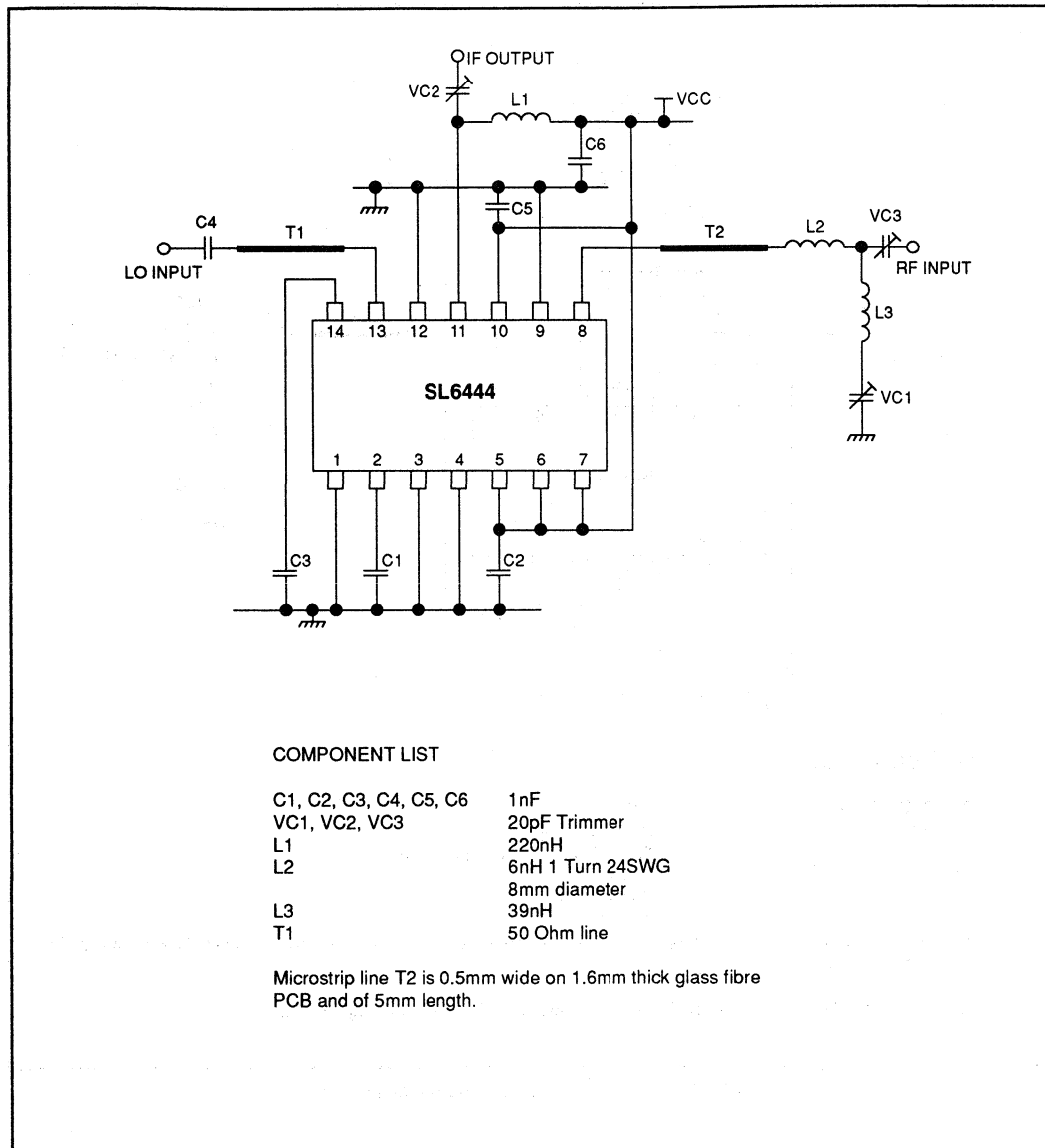


Fig. 6 Single balanced mixer demonstration circuit

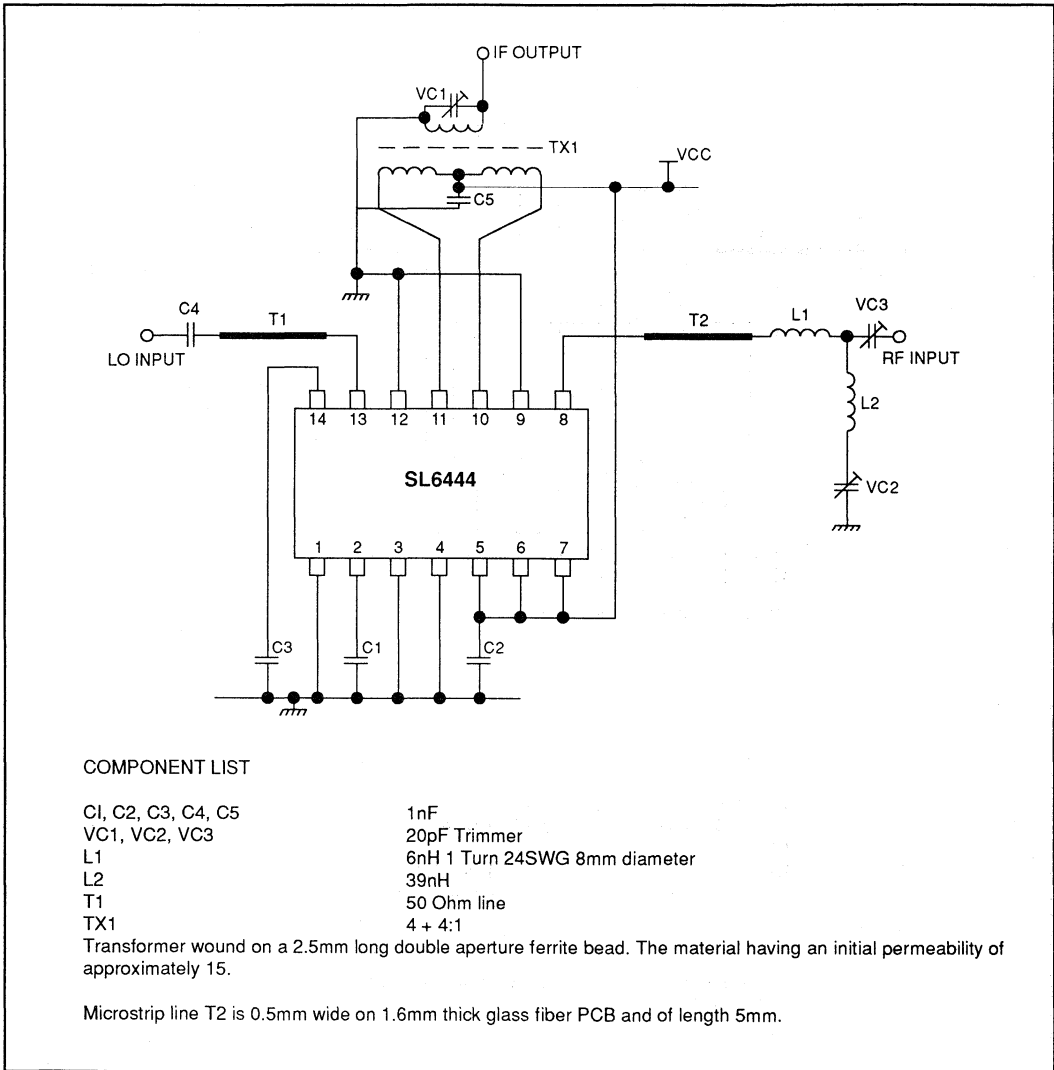


Fig. 7 Double balanced mixer demonstration circuit

# Section 5

## Amplifiers







# SL562

## LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

### FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1 kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- Available In Small Outline

### APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Radio Applications

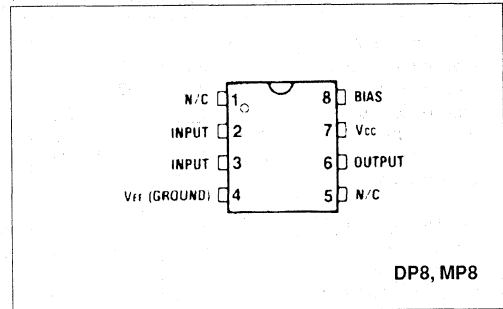


Fig. 1 Pin connections - top view

### QUICK REFERENCE DATA

- Supply Voltages  $\pm 1.5V$  to  $\pm 10V$
- Supply Current  $\pm 40\mu A$  to  $\pm 2mA$
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range  $-40^{\circ}C$  to  $+85^{\circ}C$

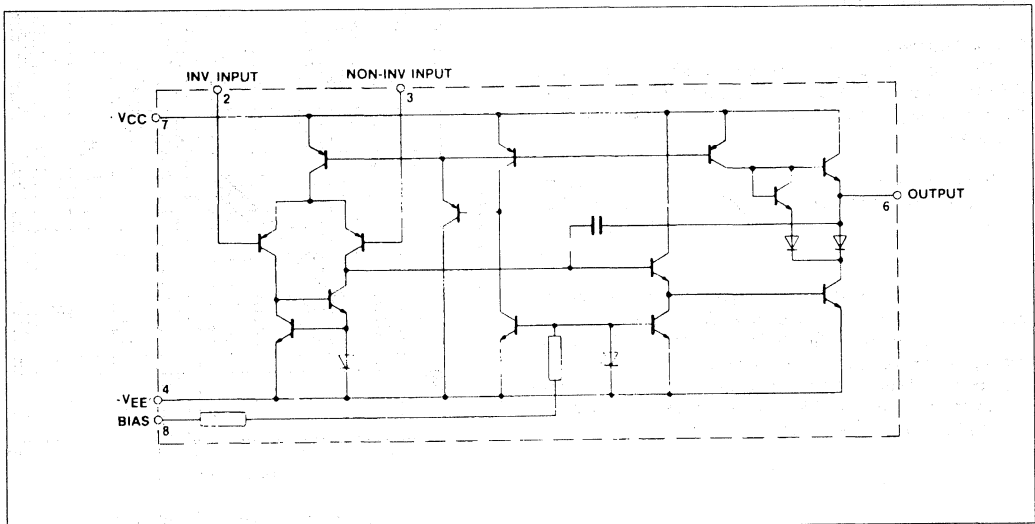


Fig. 2 Circuit diagram.

# SL562

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating mode A : Supply volts ±10V Bias set current 75µA

Operating mode B : Supply volts ±3.5V Bias set current 15µA

Operating mode C : Supply volts ±1.5V Bias set current 1µA

Characteristics	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5							mV	$R_s = 10k\Omega$
Input offset current		20	190		1	5		1	5	nA	
Input bias current		250	800			150			49	nA	
Input resistance		0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	µA	
Large signal voltage gain	74	95		74	90		74	90		dB	
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	
Supply voltage rejection ratio	74			85			85			dB	
Short circuit current	12		40				1	2.2		mA	$T_{amb} = 0^\circ C$ to $+70^\circ C$
Gain bandwidth product		3.5			1			50		kHz	Gain = 20dB
Slew rate		1.5			0.5			0.02		V/µs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	$f_o = 1kHz$
Input noise current		1.6			1.6			1.0		pA√Hz	$f = 1kHz$

## OPERATING NOTES

### Bias set current

The amplifier is programmed by the ISET current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	ISET x 50kHz
Power supply current (each supply)	ISET x 25, µA
Slewrate	ISET x 0.02V/11S (ISET in µA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 1.0, µA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I<sub>SET</sub> current is determined by:

$$I_{SET} = \frac{V_s - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken over than 1V above the negative power supply.

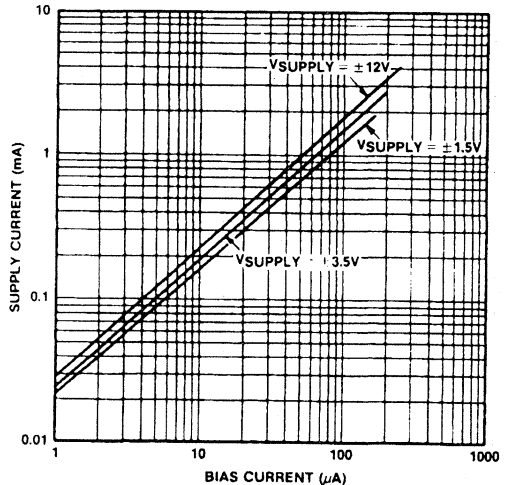


Fig. 3 Supply current v. bias set current

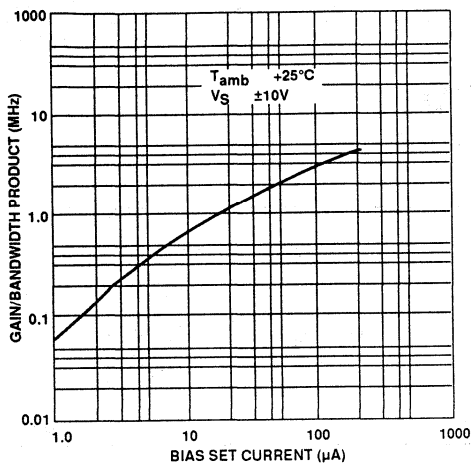


Fig. 4 Gain bandwidth product v.  $I_{SET}$

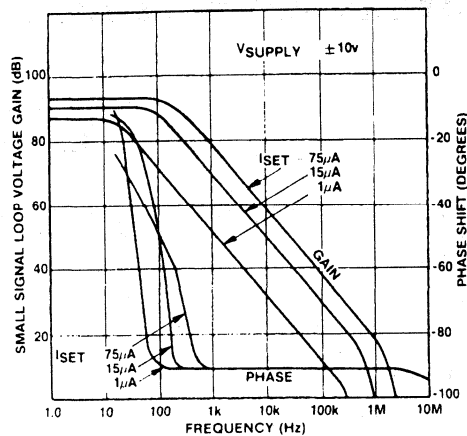


Fig. 5 Typical frequency response

**APPLICATION EXAMPLE**

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the GPS low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

**ABSOLUTE MAXIMUM RATINGS**

Supply voltages	$\pm 15\text{V}$
Common mode input voltage	Not greater than supplies
Differential input voltage	$\pm 25\text{V}$
Bias set current	10mA
Storage	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Power dissipation	800mW at $25^\circ\text{C}$
	Derate at $7\text{mW}/^\circ\text{C}$ above $25^\circ\text{C}$
Operating temperature range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$

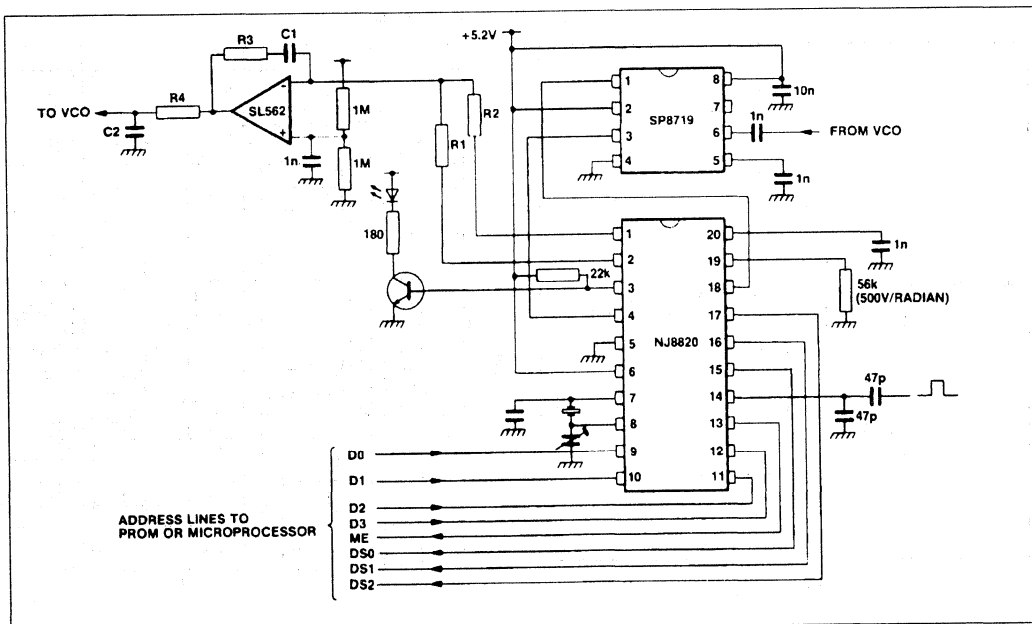


Fig. 6 Application example

# SL1610

## RF/IF AMPLIFIER

The SL1610C RF voltage amplifier with AGC facilities. The voltage gain is 10 and the upper frequency response is 120MHz.

### FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

### APPLICATIONS

- RF Amplifiers
- IF Amplifiers

### QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 17dB to 24dB

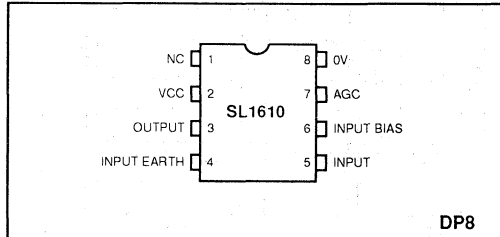


Fig.1 Pin connections (top view)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage:	12V
Storage temperature:	-55°C to +150°C
Operating temperature:	-30°C to +85°C
Chip operating temperature:	+150°C
Thermal Resistance	
Chip - to - ambient	111°C/W
Chip - to - case	71°C/W

### ORDERING INFORMATION

SL1610 NA MP

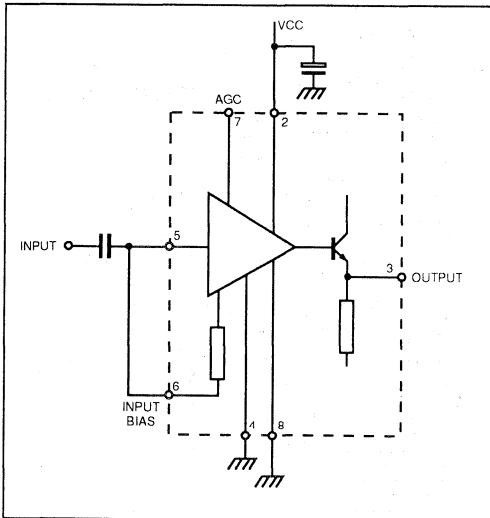


Fig.2 Block diagram

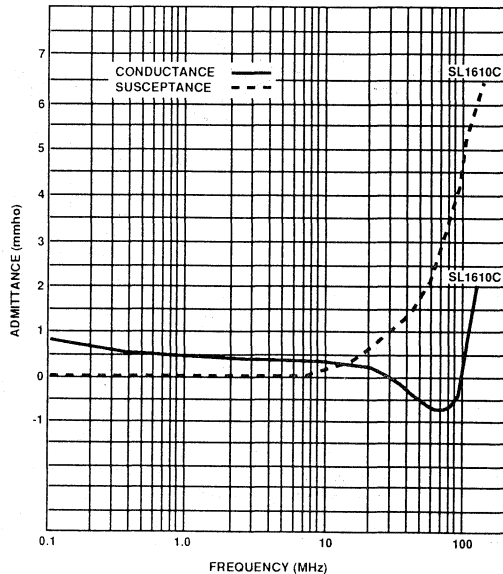


Fig.3 Input admittance with o/c output ( $G_{11}$ )

## ELECTRICAL CHARACTERISTICS

The Characteristics are guaranteed over the following test conditions (unless otherwise stated):

Supply voltage VCC: 6V  
Ambient temperature: +25°C  
Test frequency: 30MHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		15	24	mA	No signal, Pin 3 open circuit
Voltage gain	17	20	24	dB	Rs = 50Ω
Cut-off frequency (-3dB)		120		MHz	RL = 500Ω
Max. output signal (max. AGC)		1.0		V rms	RL = 150Ω
Max. input signal (max. AGC)		250		mV rms	
AGC range	40	50		dB	Pin 7 0V to 5.1V
AGC current		0.15	0.6	mA	Current into pin 7 at 5.1V

## APPLICATION NOTES

### Input circuit

The SL1610C is normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig.2.

The input impedance is negative between 30MHz and 100MHz and is shown in Fig.3. The source and inductive is should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative circuit with improved noise figure is shown in Fig.4.

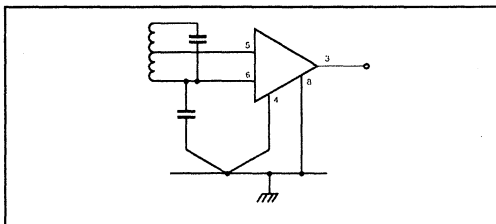


Fig.4 Alternative input circuit

### Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig.5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

## AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

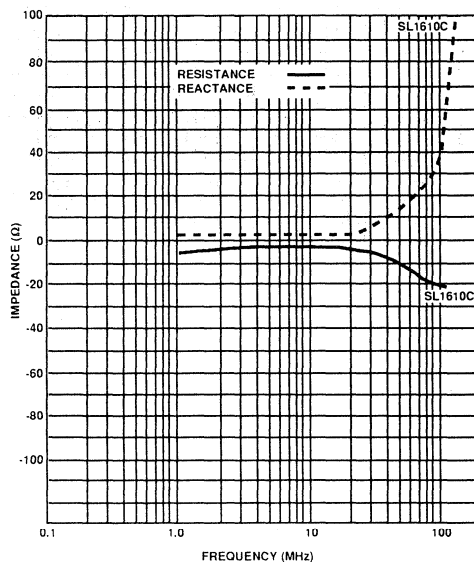


Fig.5 Typical output impedance with s/c input (G22)

# SL1610

## Typical applications

The circuit of Fig.7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig.8.

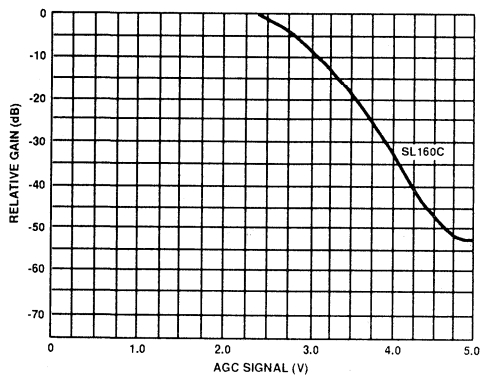


Fig.6 AGC characteristics (typical)

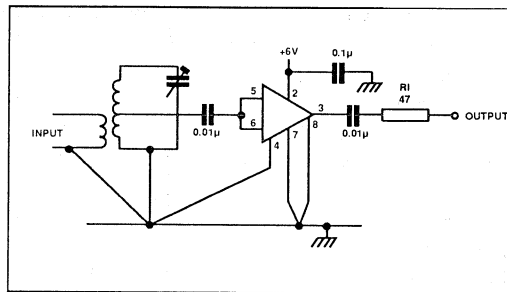


Fig.7 RF preamplifier

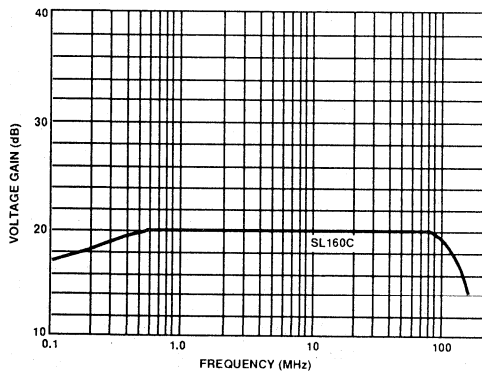


Fig.8 Typical voltage gain (RS = 50Ω)

# SL6140

## 400MHz WIDEBAND AGC AMPLIFIER

(Supersedes Edition in May 1991 Professional Products I.C. Handbook)

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced 3-micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an  $R_L$  of 1kΩ.

### FEATURES

- 400MHz Bandwidth ( $R_L=50\Omega$ )
- High voltage Gain 45dB ( $R_L=1k\Omega$ )
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (CM only)
- MC1590 Replacement with Improved Performance in most applications

### APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

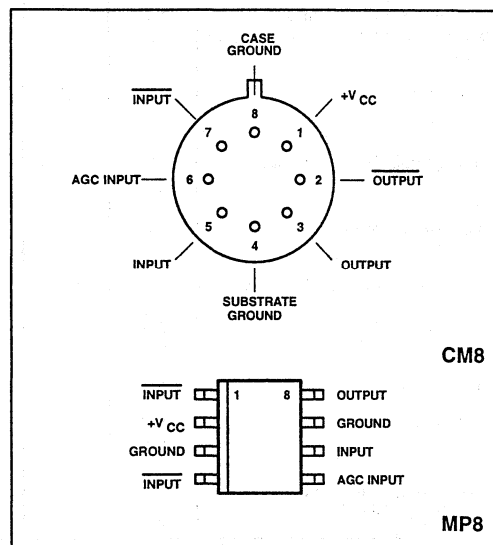


Fig. 1 Pin connections top view

### ORDERING INFORMATION

SL6140/NA/MP Industrial temperature range miniature plastic package.

SL6140A/CM Military temperature range metal can package.

SL6140AC/CM MIL STD 883 "Class B" compliant metal can package.

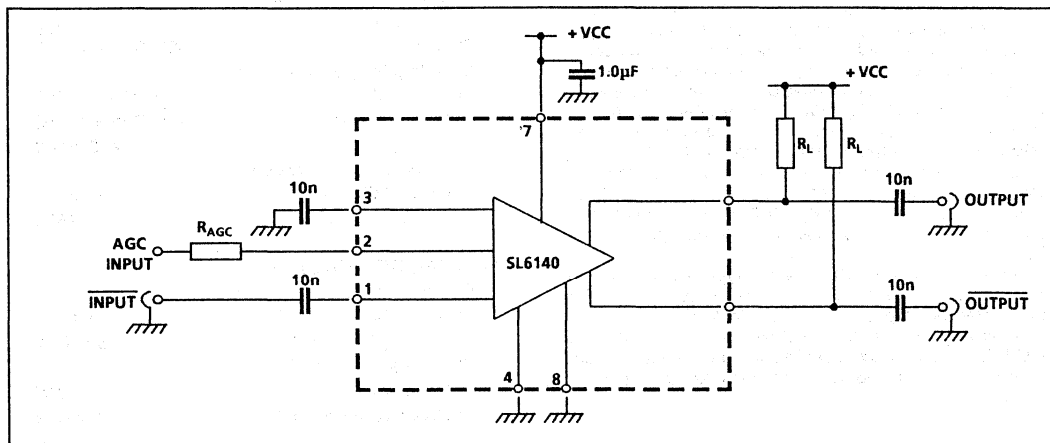


Fig. 2 Typical application (CM pinout)

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated)

 $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V} \pm 5\%$ ,  $V_{IN} = 1\text{mV}_{RMS}$ , Frequency = 6MHz, Load ( $R_L$ ) = 1KOHms,  $R_{AGC} = 22\text{KOHm}$ 

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	See note 2
AGC range	2	60	75		dB	See Fig. 4 & Note 1 ( $V_{AGC} = 0\text{V}$ to 10V)
Voltage gain (single ended)	5,6	40	45		dB	$R_L = 1\text{k}\Omega$ See Fig. 5 & Note 1
	5,6		55		dB	Tuned input and Output
			15		dB	$R_L = 50\Omega$
Bandwidth (-3dB)	5,6		25		MHz	$R_L = 1\text{k}\Omega$ See Fig. 5 See note 2
			400			
Maximum output level (single ended)	5,6	2.5	3.5		V p-p	Note 1
			3.5			
0dB AGC	5,6	2.5	3.5		V p-p	$R_L = 1\text{k}\Omega$ . Note 1
-30dB AGC	5,6	2.5	3.5		V p-p	
Noise figure	5,6		5		dB	Test CCT Fig. 13
Gain change with temp. $V_{AGC} = 9\text{V}$	5,6		+4.5		dB	At $-55^{\circ}\text{C}$ W.R.T R/T See note 2
	5,6		-3		dB	At $+125^{\circ}\text{C}$ W.R.T R/T See note 2
Gain change with temp. $V_{AGC} = 10\text{V}$	5,6		+2		dB	At $-55^{\circ}\text{C}$ W.R.T R/T See note 2
	5,6		-3		dB	At $+125^{\circ}\text{C}$ W.R.T R/T See note 2

Note: 1 Guaranteed but not tested for MP package

Note: 2 Guaranteed but not tested

**DESCRIPTION**

The SL6140 (Fig. 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor ( $R_{AGC}$ ), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by  $R_L$ . With load resistance of 1k $\Omega$  the single ended voltage gain is 45dB and with a load resistance of 50 $\Omega$  the voltage gain is 15dB ( $20\log_{10} V_{OUT}/V_{IN}$ ). Another parameter that depends on the load resistance is the bandwidth: 25MHz for  $R_L = 1\text{k}\Omega$ , as compared with 400MHz for  $R_L = 50\Omega$ .  $R_L$  is chosen to give either the required bandwidth or voltage gain for the circuit.

Figs. 7 through to 10 show the typical S parameters for the device. Figs 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate (pin 4 in CM 8, pin 7 in MP 8) should be connected to the most negative point in the circuit, usually to the same point as pin 8 (pin 3 in MP 8).

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage, $V_{CC}$	+18V
Input voltage (differential)	+5V
AGC supply	$V_{CC}$
Storage temperature	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating temperature range	
SL6140 MP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
SL6140 A CM	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
	at 200mW
Chip operating temperature	
SL6140 MP	+150 $^{\circ}\text{C}$
SL6140 (CM variants)	+175 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

Chip-to-ambient	
SL6140 MP	163 $^{\circ}\text{C}/\text{w}$
SL6140 (CM variants)	225 $^{\circ}\text{C}/\text{W}$
Chip-to-case	
SL6140 MP	57 $^{\circ}\text{C}/\text{W}$
SL6140 (CM variants)	65 $^{\circ}\text{C}/\text{W}$



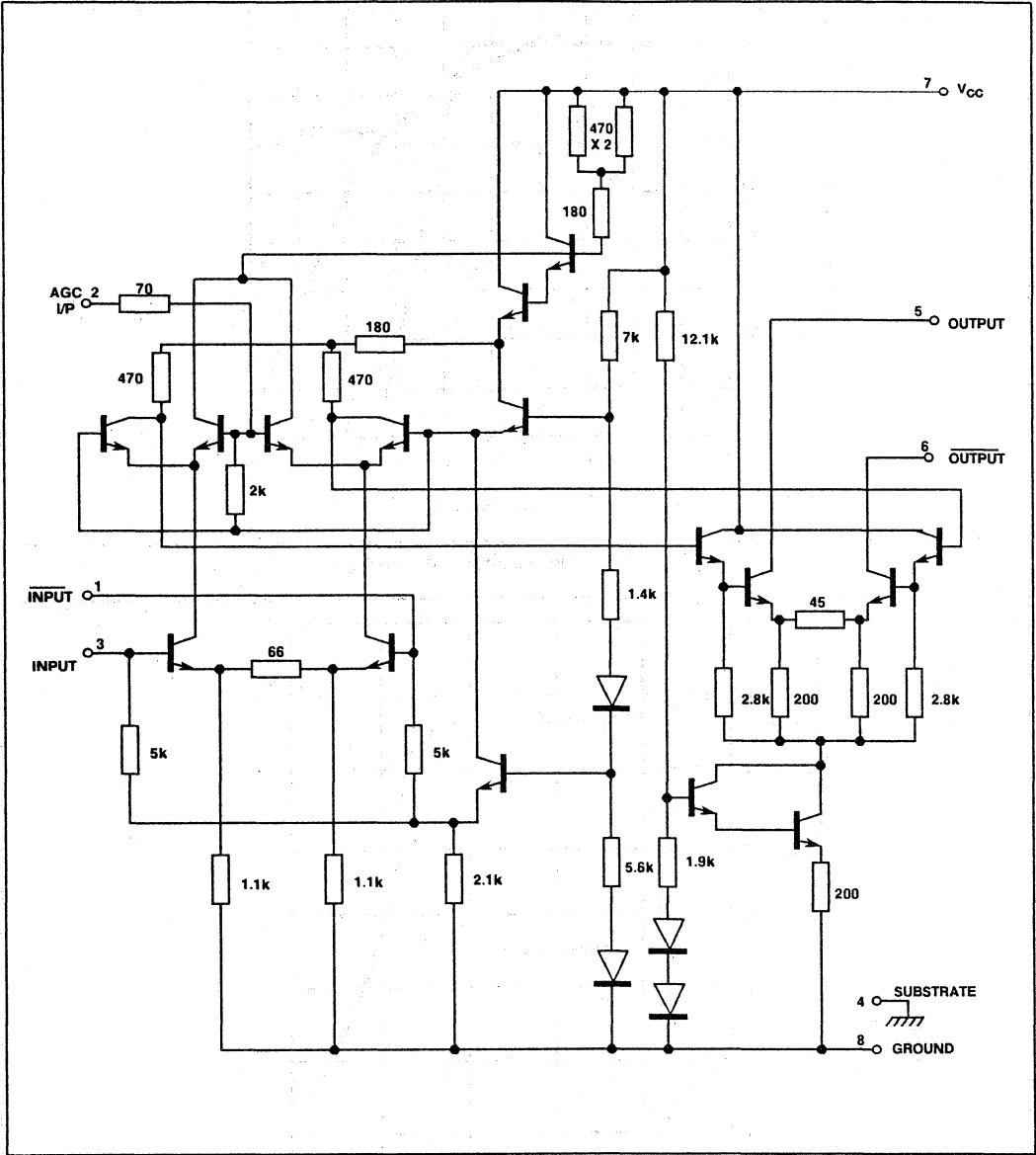


Fig. 3 Full circuit diagram of SL6140 (CM pinout)

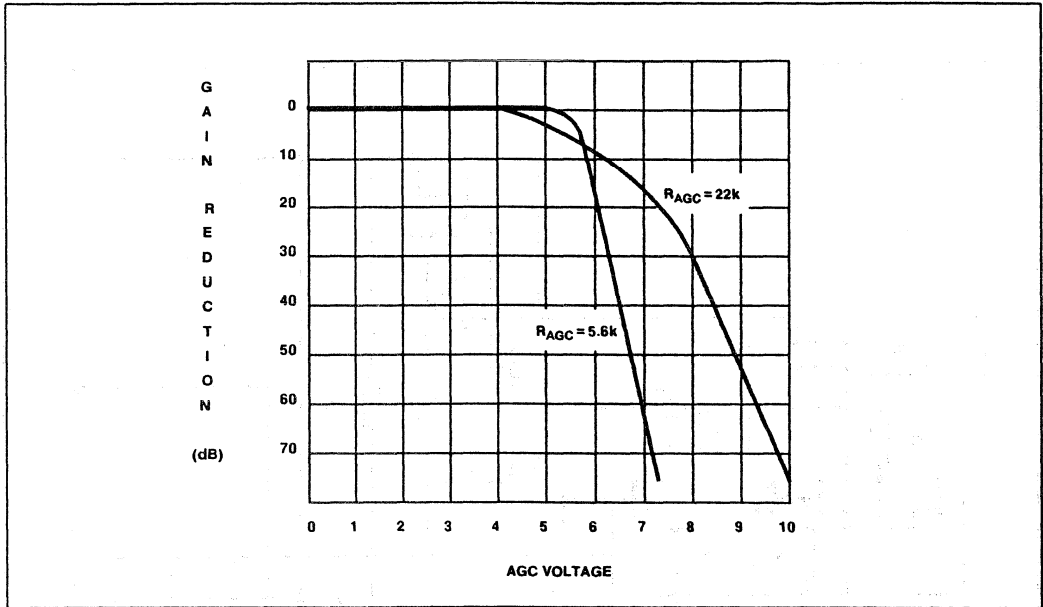


Fig. 4 Gain reduction v. AGC voltage

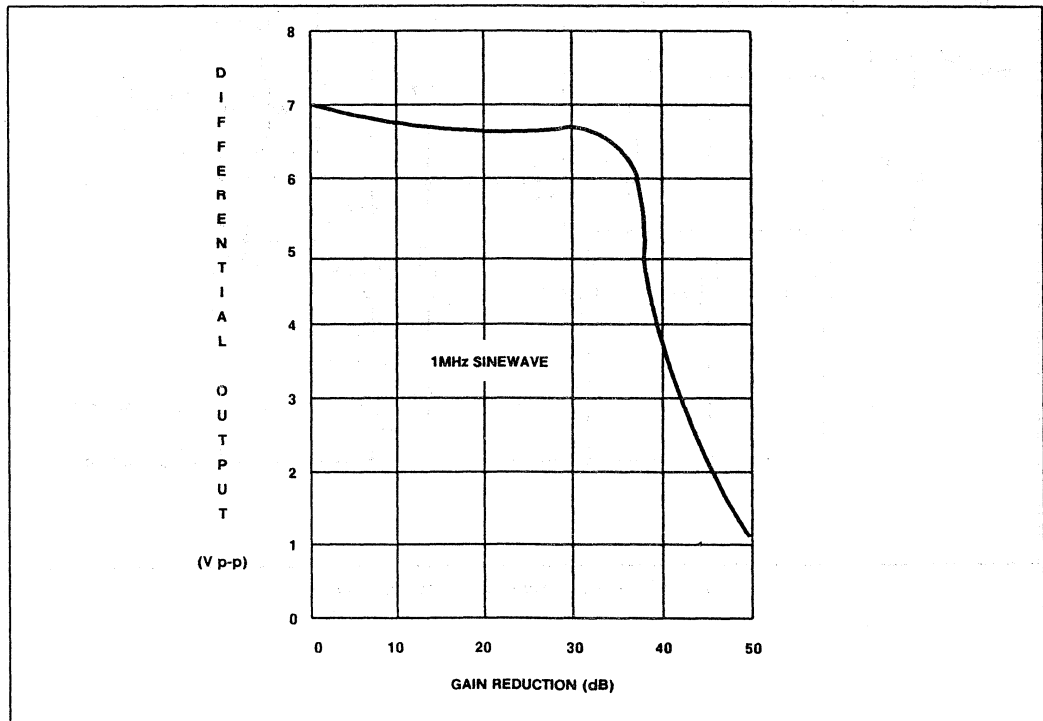


Fig. 5 Max differential O/P voltage v gain reduction

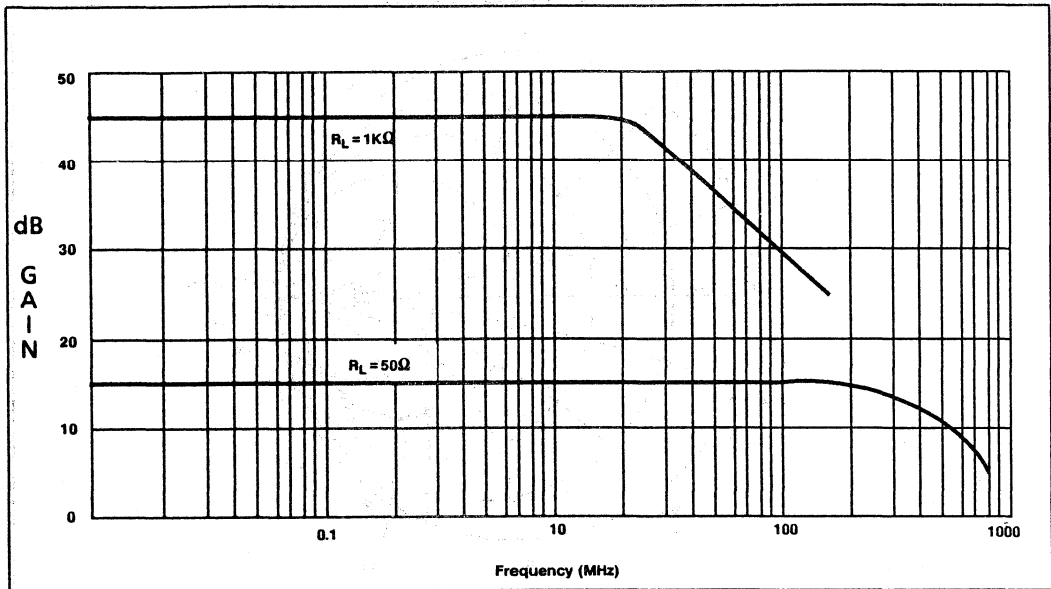


Fig. 6 Voltage Gain V. Frequency

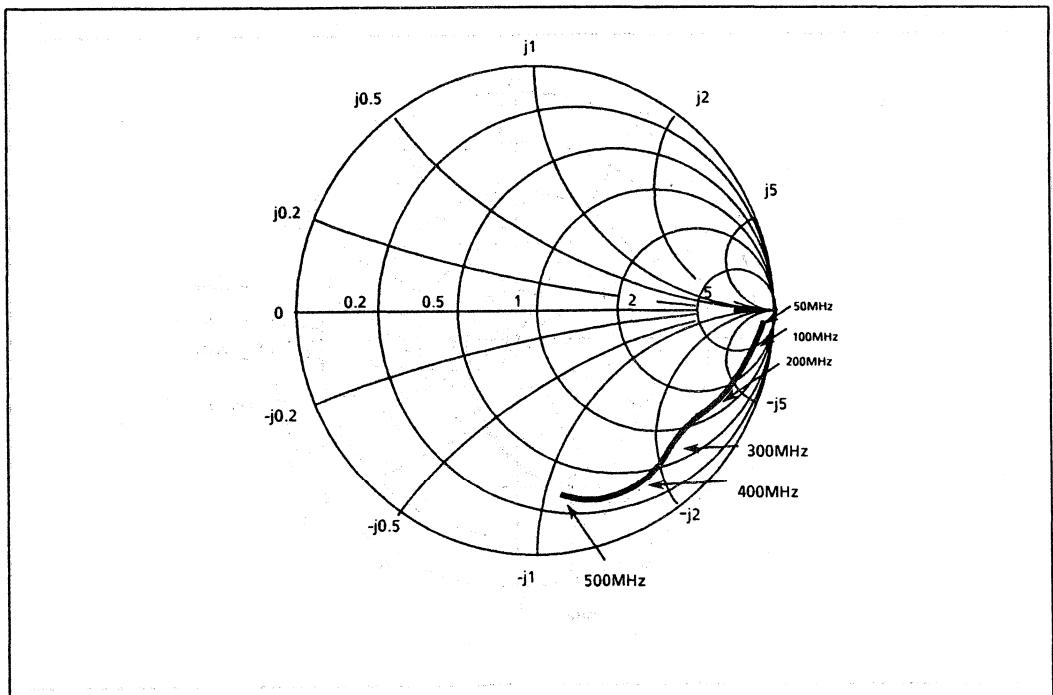


Fig. 7 Input impedance 50Ω system

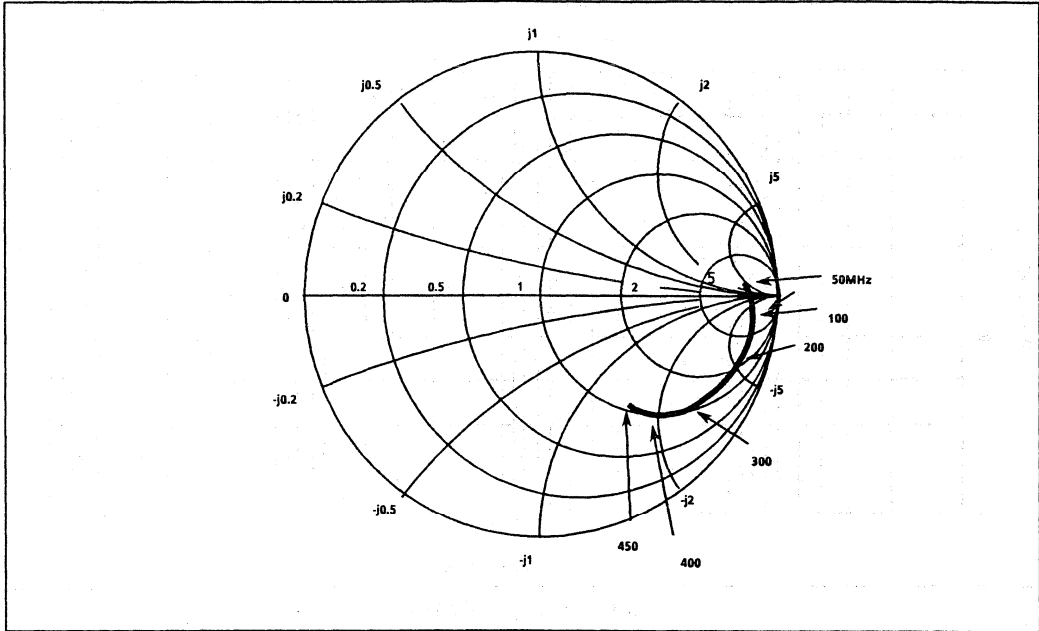


Fig. 8 Output impedance 50Ω system

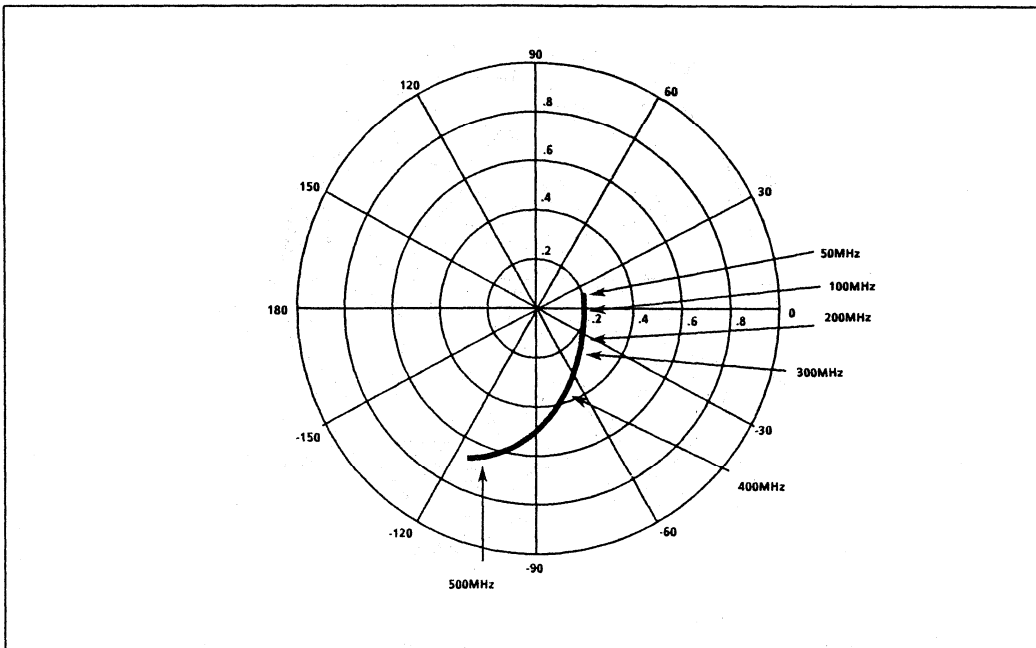


Fig. 9 Reverse transmission coefficient  $S_{12}$  SL6140

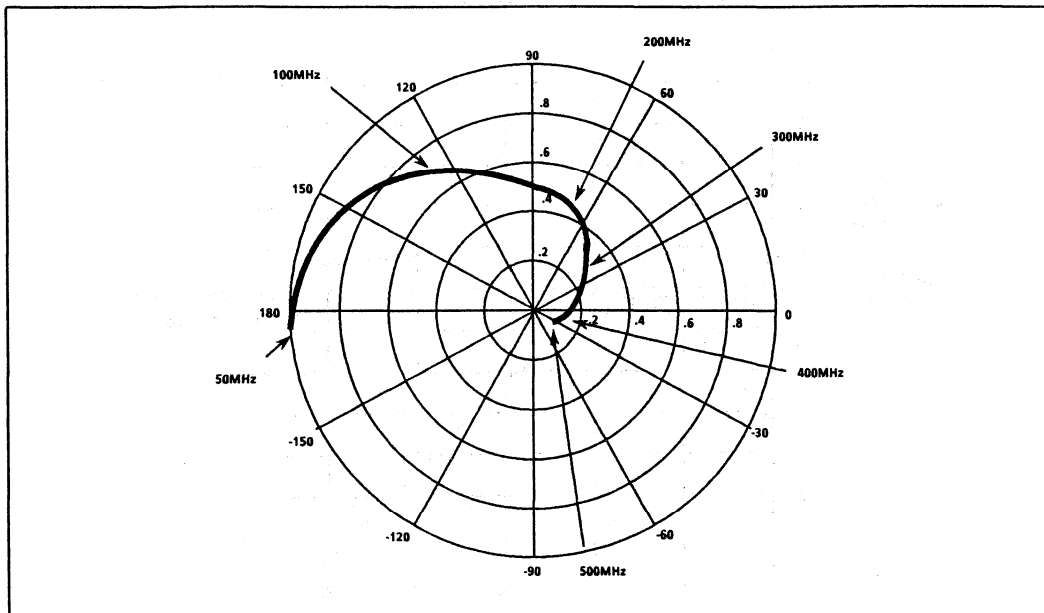


Fig.10 Forward transmission coefficients  $S_{21}$  SL6140

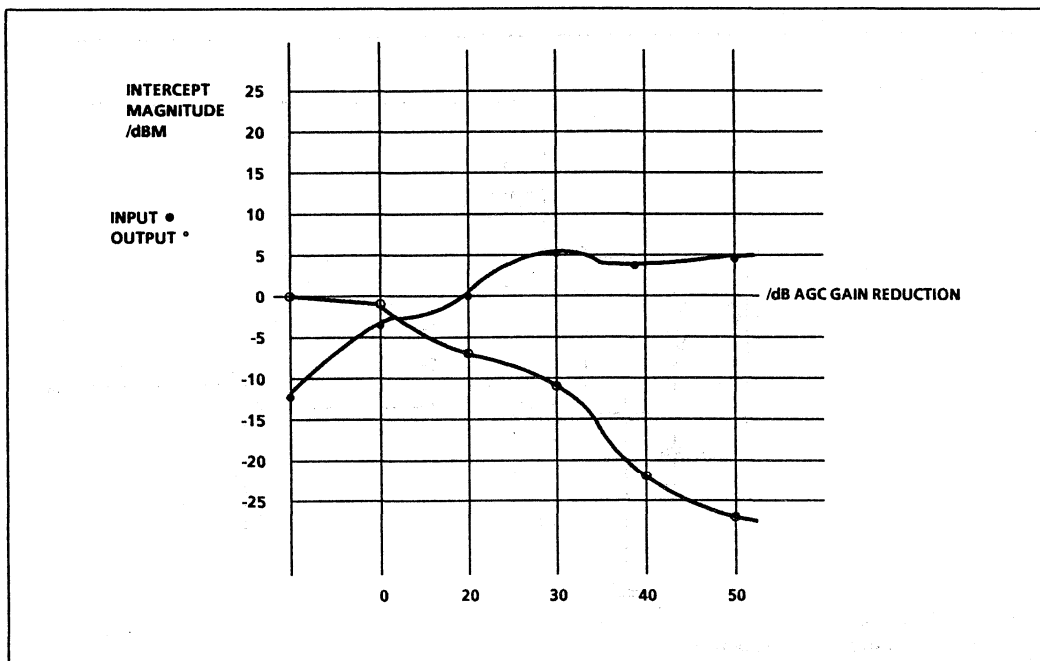


Fig.11 3rd Order intercept point against gain reduction at 250.0MHz and 254.0MHz

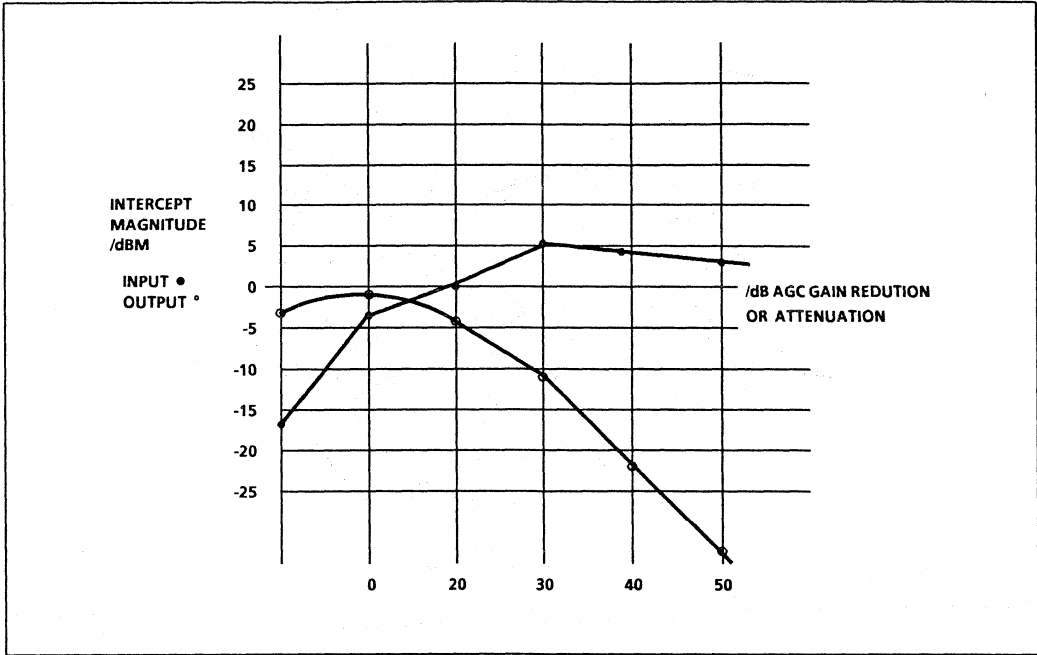


Fig.12 3rd Order intercept point against gain reduction at 100.0Mhz and 104.0MHz

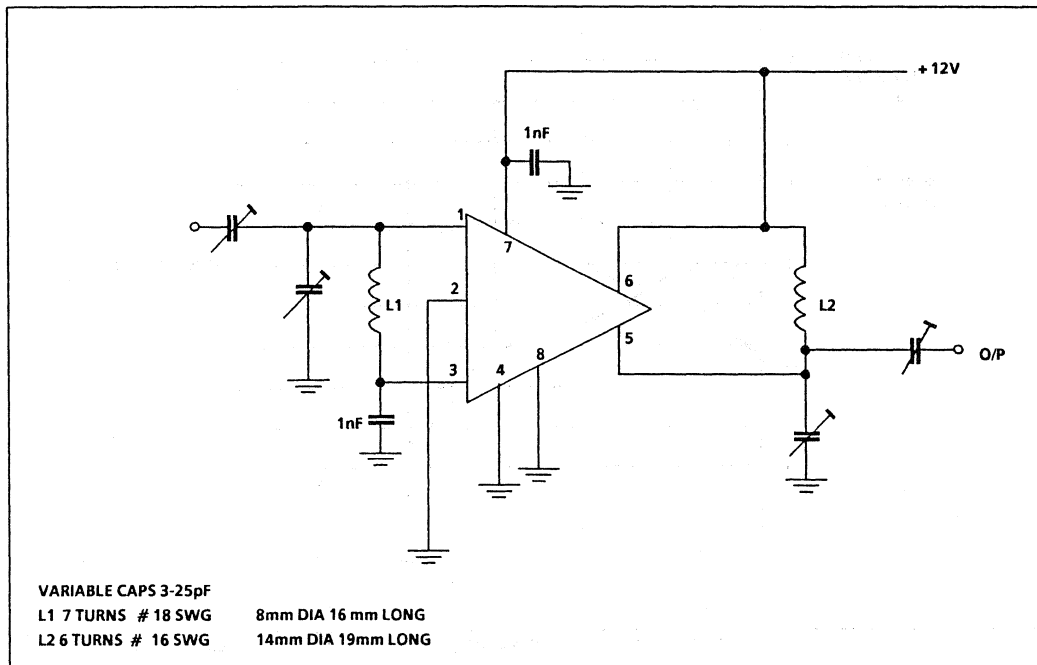


Fig.13 50MHz Noise figure test circuit (CM package)

# SL6270C

## GAIN CONTROLLED MICROPHONE PREAMPLIFIER/VOGAD

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

### FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

### APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

### QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

### ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V  
Storage temperature: -55°C to +125°C

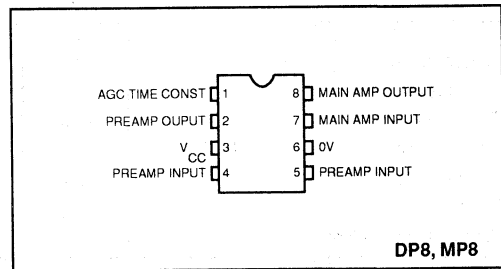


Fig. 1 Pin connections, SL6270 - DP (top view)

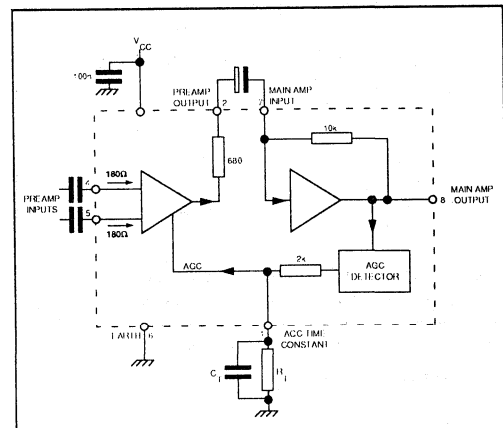


Fig. 2 SL6270 block diagram

# SL6270C

## ELECTRICAL CHARACTERISTICS

### Test conditions (unless otherwise stated):

Supply voltage Vcc: 6V  
 Input signal frequency: 1kHz  
 Ambient temperature: -30°C to +85°C  
 Test circuit shown in Fig. 4

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4MV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth

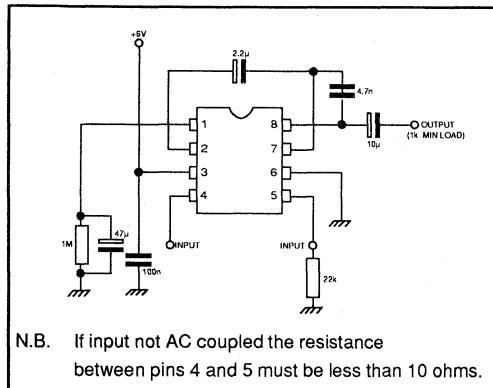


Fig. 3 SL6270 test and application circuit

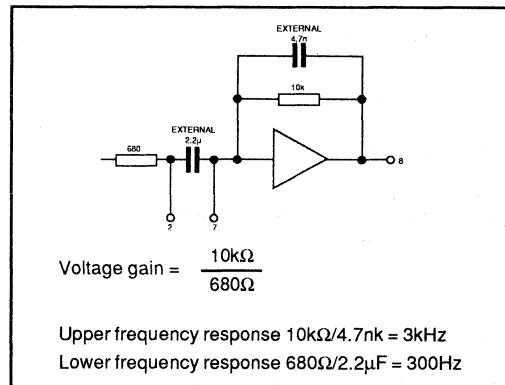


Fig. 4 SL6270 frequency response

## APPLICATION NOTES

### Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

### Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

### Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.



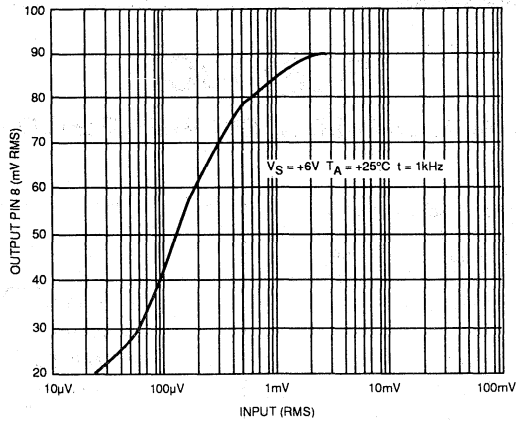


Fig. 5 Voltage gain (single ended input) (typical)

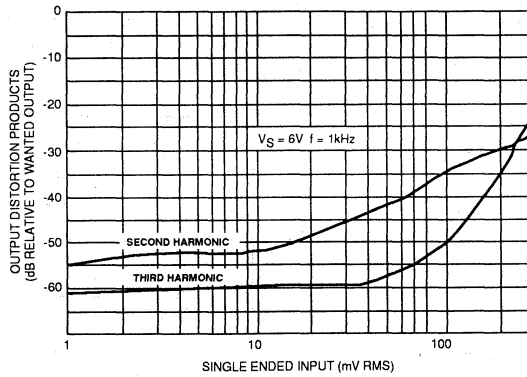


Fig. 6 Overload characteristics (typical)

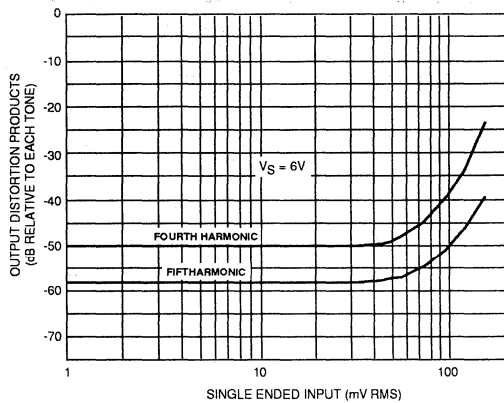


Fig. 7 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

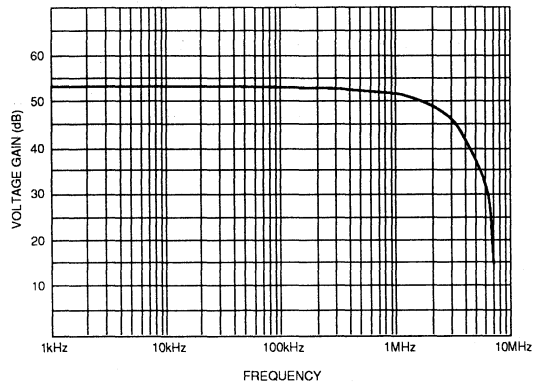


Fig. 8 Open loop frequency response (typical)

# SL6310C

## 500mW SWITCHABLE AUDIO AMPLIFIER/OP AMP

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

### FEATURES

- Can be Muted with High or Low State inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

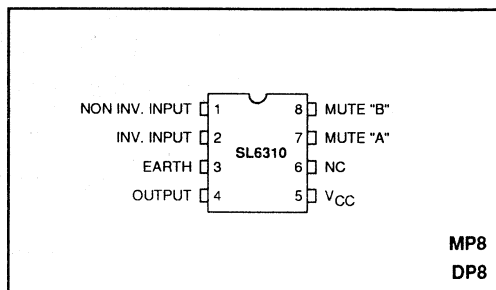


Fig. 1 Pin connections, SL6310 - (top view)

### APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

### QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply : 400mW (min.)

### ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V  
Storage temperature: -55°C to + 125°C

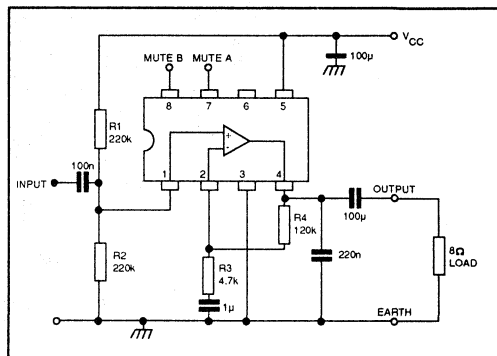


Fig. 2 SL6310 Test Circuit

**ELECTRICAL CHARACTERISTICS****Test conditions (unless otherwise stated):**Supply voltage  $V_{CC}$ : 7V

Ambient temperature: -30°C to +85°C

Mute facility : Pins 7 and 8 open circuit frequency = 1kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current mute (A)		0.55	1	mA	Pin 7 via 470k to earth
Supply current mute (B)		0.6	0.9	mA	Pin 8 = $V_{CC}$
Input offset voltage		2	20	mV	$R_s \leq 10k$
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	$\mu A$	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	$V_{CC} = 4.5V$
		10.6		V	$V_{CC} = 13V$
CMRR	40	60		dB	$R_s \leq 10K$
Output power	400	500		mW	$R_L = 8\Omega$
THD		0.4	3	%	$P_{OUT} = 400mW,$ Gain = 28dB

**NOTE**

- The input bias current flows **out** of pins 1 and 2 due to PNP input stage

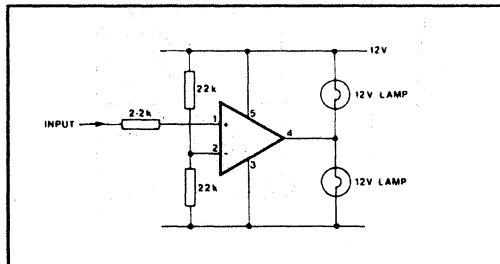


Fig. 3 SL6310 lamp driver

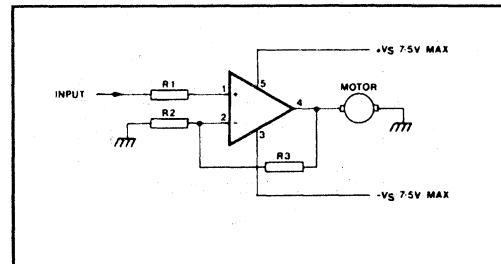


Fig. 4 SL6310 servo amplifier

**OPERATING NOTES****Mute facility**

The SL6310 has two mute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of  $V_{CC}$  (via a 100k $\Omega$  resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100k $\Omega$  resistor) the SL6310 is muted

**Audio amplifier**

As the SL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100k $\Omega$ . The voltage gain is determined by the ratio  $(R_3 + R_4)/R_3$  and should be between 3 and 30 for best results. The capacitor in series with  $R_3$ , together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across  $R_4$ .

**Operational amplifier**

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

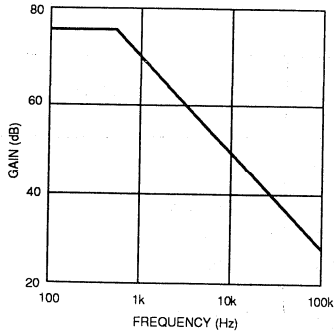


Fig. 5 Gain v. frequency

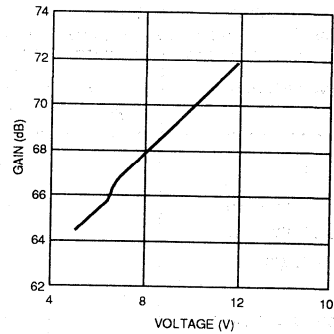


Fig. 6 Gain v. supply voltage

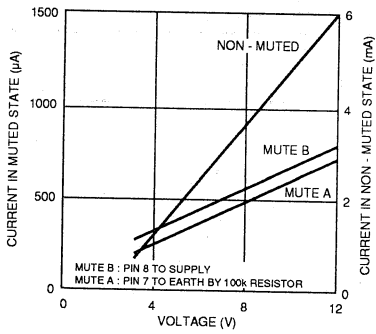


Fig. 7 Supply current v. supply voltage

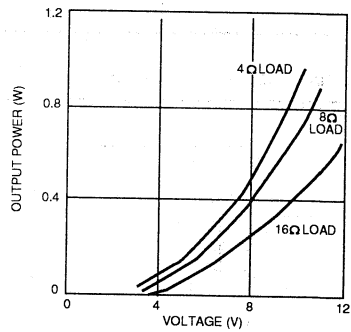


Fig. 8 Output power v. supply voltage at 5% (max) distortion

# Section 6

## CODEC





# MV3100

## 3 VOLT CODEC WITH ANALOG INTERFACE FOR DIGITAL MOBILE TELEPHONES

(Supersedes version in June 1990 Personal Communications IC Handbook)

The MV3100 is a complete integrated audio interface for digital mobile telephones. Using mixed signal CMOS technology the device contains a DSP codec for audio to PCM conversion, together with gain programmable microphone and loudspeaker amplifiers.

The use of a DSP architecture for the codec function enables device operation from supplies of 2.7 to 3.6 volts and allows software programming of gain characteristics. The device requires a minimum of external components giving a physically small solution, ideal for hand-portable telephones.

### FEATURES

- Highly Integrated Solution with On-chip Audio Interface
- Meets Relevant Performance Parameters from MPT1375, I-ETS300 131:1990, BS6833 and CCITT G714
- Low Voltage Operation, 2.7V to 3.6V
- Low Power Consumption, 25mW typ
- Excellent RF Immunity
- 16-Bit Linear/8-Bit Companded A/μ-Law Programmable PCM Interface
- Gain Programmability Supports many Microphone and Loudspeaker Sensitivities
- On-chip PLL Generates all Internal Clocks

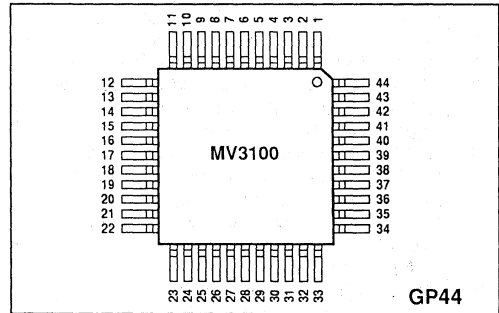


Fig. 1 Pin connections - top view. See pin list, Table 1.

### APPLICATIONS

- Digital Cordless Telephones (CT2, DECT, JDCT, Spread Spectrum)
- Digital Cellular Telephones (GSM, ADC, JDC)
- Digital Mobile Radio

### ORDERING INFORMATION

MV3100 IG GPBR (Industrial - plastic QFP package)

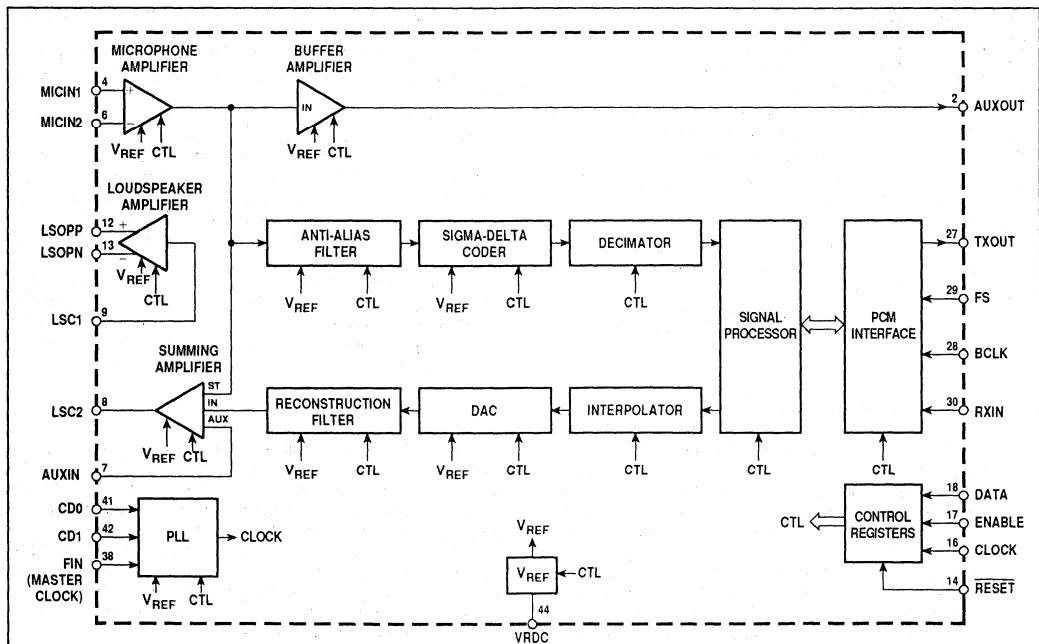


Fig. 2 MV3100 block diagram

Pin	Name	Description
1	V <sub>DD</sub> TX	Transmit path analog V <sub>DD</sub>
2	AUXOUT	Transmit path auxiliary output
3	IC	Internal connection - do not connect
4	MICIN1	Microphone amp. input non-inverting input
5	GNDTX	Transmit path analog ground
6	MICIN2	Microphone amp. inverting input
7	AUXIN	Receive path auxiliary input
8	LSC2	Summing amplifier intermediate output
9	LSC1	Loudspeaker amplifier intermediate input
10	GNDRX	Receive path analog ground
11	V <sub>DD</sub> RX	Receive path analog V <sub>DD</sub>
12	LSOPP	Loudspeaker amp. non-inverting output
13	LSOPN	Loudspeaker amp. inverting output
14	RESET	Master reset (active low)
15	IC	Internal connection - do not connect
16	CLOCK	Control interface data clock
17	ENABLE	Control interface enable
18	DATA	Control interface data input
19	IC	Internal connection - do not connect
20	IC	Internal connection - do not connect
21	IC	Internal connection - do not connect
22	IC	Internal connection - do not connect
23	IC	Internal connection - do not connect
24	NC	No connection
25	V <sub>DD</sub> D	Digital V <sub>DD</sub>
26	NC	No connection
27	TXOUT	PCM interface transmit data output
28	BCLK	PCM interface data clock
29	FS	PCM interface frame sync.
30	RXIN	PCM interface receive data input
31	GNDD	Digital ground
32	NC	No connection
33	IC	Internal connection - do not connect
34	NC	No connection
35	IC	Internal connection - do not connect
36	IC	Internal connection - do not connect
37	IC	Internal connection - do not connect
38	FIN	PLL reference frequency input (Master Clock)
39	V <sub>DD</sub> PL	PLL V <sub>DD</sub>
40	GNDPL	PLL ground
41	CD0	PLL capacitor ground connection
42	CD1	PLL capacitor signal connection
43	NC	No connection
44	VRDC	Voltage reference decoupling

Table 1 Pin list

## FUNCTIONAL DESCRIPTION

The transmit circuit has a low noise differential input microphone amplifier front end and is suitable for use with an electret microphone. For use in cordless or mobile telephone applications the sensitive analog inputs are designed to be immune to RF pickup. The transmit gain may be varied over a range of 22.8 dBm0/dBV to 37.8 dBm0/dBV in 1dB steps. An auxiliary analog output is available.

The analog transmit signal is passed through a simple Anti-alias Filter and is then sampled by the Sigma-Delta Coder which, combined with the Decimator, performs a high linearity analog to digital conversion. This digital signal is then passed to the Signal Processor which performs the transmit filtering. The transmit filter may be set to either of two modes. For handset use the full band-pass filter is implemented, while for base station use the

transmit filter has reduced bass roll-off.

The filtered digital transmit signal from the Signal Processor is output via the serial PCM interface. The PCM interface can be programmed via the control interface to operate in one of three modes, 16-bit 2's complement linear PCM, 8-bit companded A-Law coding or 8-bit companded  $\mu$ -Law coding. In all modes, each word or byte is output as a serial bit stream at a frame rate of 8K words/bytes per second under the control of the bit clock BCLK and the frame sync FS inputs. A mute function is included on the output.

The digital receive signal is input to the Signal Processor via the PCM interface as a series of sixteen-bit words or eight-bit bytes as described above. A separately controlled mute function may also be applied.

The Signal Processor performs the receive band-pass filtering and then passes the filtered digital signal to the Interpolator. The Interpolator in conjunction with the DAC performs a high linearity digital to analog conversion. The resulting analog output is filtered by the Reconstruction Filter to remove the sampling noise.

The Summing Amplifier may optionally add to the received signal the auxiliary analog input and the sidetone signal from the transmit path. The nominal sidetone gain may be varied from 19.7 dB to 28.7 dB in 3dB steps. The Summing Amplifier output is connected externally to the Loudspeaker Amplifier input to enable external filtering components to be added if required. The Loudspeaker Amplifier is a bridge amplifier which has been designed to drive a ceramic loudspeaker. It can produce a low distortion drive into loads of up to 105nF at a peak to peak amplitude near to twice V<sub>DD</sub>.

The Phase Locked Loop generates the internal clock signals from a 32kHz input clock. After power-up the PLL clock must be enabled by programming Control Register 100 bit 3 (PLL Clock Enable) to the on state ('0'). The PLL is specifically designed to extract a low phase error clock in cases where there is jitter on the input clock, provided that there are exactly 64 input clock cycles in every 500Hz period. This ensures accurate clock extraction from the CT2 'ping-pong' signalling system.

The on-chip bandgap voltage reference provides the necessary biasing and reference voltages required by the analog circuitry.

Programming of the various gains and operating modes for the device is by means of a three-wire serial interface to the Control Registers. Data is clocked into the Data input under control of the Clock and Enable inputs. The digital circuitry and various parts of the analog circuitry may be powered down individually by means of the control interface. This may be used to minimise power consumption during various phases of call set-up and standby operation.

The device is designed to operate from a nominal 3 volt supply. Separate supply and ground pins are provided for the transmit analog, receive analog and digital circuits to improve decoupling between transmit and receive paths and reduce digital noise breakthrough into the analog circuitry.

## DETAILED DESCRIPTION

### Microphone Input

The Microphone Amplifier was designed to meet the CT2 Common Air Interface specification MPT1375 Part 4. With the transmit gain set to its nominal value, an input of -34.8dBV will produce a digital output of 0dBm0. The circuit was designed for a microphone with a nominal sensitivity of -41.8dBV/Pa. This gain may be varied by +3.0dB to -12.0dB in steps of 1dB by means of the control interface. This gain range is intended to provide for a microphone sensitivity tolerance of  $\pm 3$ dB and permits a gain reduction of up to 9dB to reduce sensitivity for use in conditions of high ambient noise.

The Microphone Amplifier may be powered down by means of the control interface when not in use to reduce power consumption.



**Auxiliary Output**

The auxiliary output has a nominal gain of 19.9 dB from the microphone input. The output level is dependent on the gain setting giving a gain range of 7.9dB to 22.9dB. The output is designed to be able to deliver a 500 mV rms signal into a 30kΩ +20 pF load.

The auxiliary output may be turned off by means of the control interface when not in use to reduce power consumption.

**Loudspeaker Output**

The Loudspeaker Amplifier was designed to meet the CT2 Common Air Interface specification MPT1375 Part 4. With the receive gain set to its nominal value, an output of -6.1dBV will be produced for a digital input of 0dBm0. The circuit was designed for a loudspeaker with a nominal sensitivity of +12.0 dBPa/V. The gain may be varied by +9.0dB to -22.0dB in steps of 1dB by means of the control interface. This gain range is intended to provide for a loudspeaker sensitivity tolerance of ± 3dB and permit a gain variation of +6dB to -18dB to enable the implementation of a user volume control.

The Loudspeaker Amplifier may be powered down when not in use by means of the control interface to reduce power consumption.

The nominal gain from the auxiliary input to the loudspeaker output is 13.4dB. This gain is dependent on the receive gain setting giving a gain range of +22.4dB to -8.6dB. The auxiliary input may be disconnected by means of the control interface if not required.

The nominal sidetone gain from the microphone input to the loudspeaker output (with both transmit and receive gains set to nominal) is 25.7dB. This gain may be varied by +3.0dB to -6.0dB in 3.0dB steps by means of the control interface. If not required, the sidetone may be turned off by means of the control interface.

**PCM INTERFACE**

The PCM Interface inputs the received digital signal RXIN and outputs the transmit digital signal TXOUT in the form of sixteen-bit words or eight-bit bytes as a serial bit stream under the control of the two timing signals FS and BCLK.

Three PCM coding options are programmable via the control interface, linear sixteen-bit 2's complement PCM, eight-bit A-Law companded PCM or eight bit μ-Law companded PCM. It is normal in a system to have a single coding scheme; for this reason Transmit and Receive coding are programmed simultaneously to work with the same scheme.

The serial PCM interface thus consists of four pins; three inputs and one output.

- BCLK PCM data clock input
- FS PCM frame sync input
- TXOUT PCM transmit data output
- RXIN PCM receive data input

Interface timings are shown in Figs. 3 and 4.

**NOTES**

1. The Sync pulse is nominally one clock pulse wide, changes in state nominally coinciding with the rising edge of the clock. Jitter on the FS rising edge can occur up to ±5μs on the actual and ideal edge positions.
2. The Data bits are nominally one clock cycle wide, nominally changing on the rising edge of the clock.
3. Data bits (RXIN) will be latched nominally on the falling edge of the clock.
4. The data output (TXOUT) will be high impedance between the end of the last data bit of one word/byte and the beginning of the first data bit of the next word/byte.
5. The RXIN signal must always be at a solid logic level, even though it is only the data at the times indicated which is used. In the case of RXIN the mid-line should be taken to indicate a 'don't care' state, not a high impedance state.
6. The Clock signal BCLK may consist of either a train of at least seventeen pulses in linear PCM mode or nine pulses in A/μ-Law companded PCM mode (one for FS and one for each data bit), or be a continuous clock.

This block is the interface between parallel 2's complement sixteen-bit linear PCM data and serial sixteen-bit linear 2's complement or serial eight-bit A/μ-Law companded PCM data, performing parallel-to-serial conversion in the transmit direction and serial-to-parallel conversion in the receive direction. In addition to the conversion and coding function the PCM block implements a mute function. Both TX and RX can be independently muted. The mute functions are controlled from the micro-processor bus control interface.

**A-Law and μ-Law Codes (8 Bit)**

These are non-linear codes in which the signal is described in terms of a sign bit plus segment and chord bits which denote the magnitude. There are 7 segments for A-Law and 8 for μ-Law. The size of the segment increases in approximately exponential steps. Each segment is divided up linearly into chords (except the zero level in μ-Law). This means that the resolution is finer at smaller input voltages than at larger. Tables detailing these

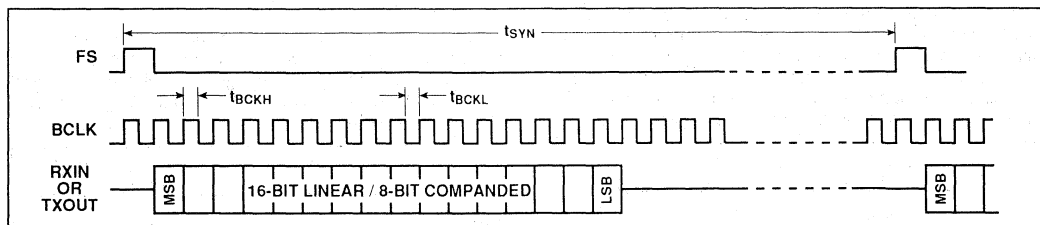


Fig. 3 PCM Interface timing diagram

Parameter	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
BCLK frequency (linear mode)	$f_{BCK}$	256		2048	kHz	FIN = 32kHz
BCLK frequency (companded mode)	$f_{BCK}$	128		2048		
BCLK rise time	$t_{BCKR}$		5		ns	
BCLK fall time	$t_{BCKF}$		5		ns	
BCLK high time	$t_{BCKH}$	200			ns	
BCLK low time	$t_{BCKL}$	200			ns	
FS pulse period	$t_{SYN}$		125		μs	

NOTE 1: The Frame Sync (FS) MUST be frequency locked to the 32kHz PLL Master Clock (FIN). The phase relationship is not important.

Table 2 PCM Interface timings

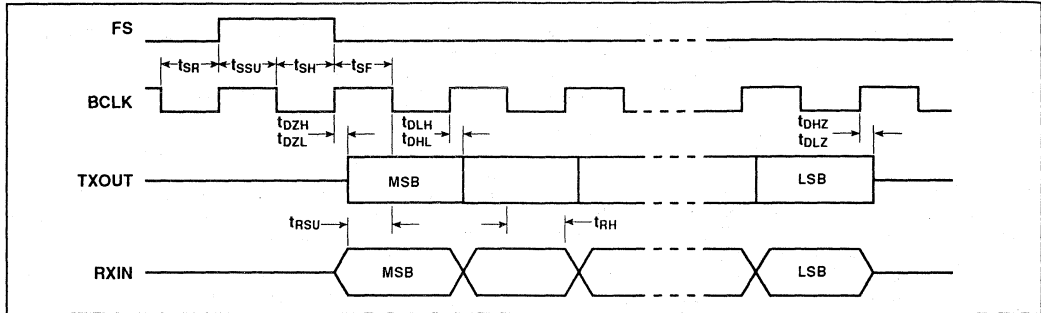


Fig. 4 PCM Interface timing diagram (expanded)

Parameter	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
FS to BCLK set-up time	$t_{SR}$	10			ns		2
FS to BCLK hold time	$t_{SH}$	15			ns		2
BCLK to FS rising time	$t_{SR}$	25			ns		2
FS falling to BCLK time	$t_{SF}$	25			ns		2
Output delay from Z to high	$t_{DZH}$			25	ns		2
Output delay from Z to low	$t_{DZL}$			25	ns		2
Output delay from high to Z	$t_{DZH}$			25	ns		2
Output delay from low to Z	$t_{DLZ}$			25	ns		2
Output delay from high to low	$t_{DLH}$			30	ns		2
Output delay from low to high	$t_{DLH}$			30	ns		2
RXIN set-up time	$t_{RSU}$	10			ns		2
RXIN hold time	$t_{RH}$	15			ns		2

Table 3 PCM Interface timings (see Fig. 4)

NOTE 2. Not production tested

codes can be found in CCITT G711.

In both codes positive values are represented by a sign bit of 1. The A-Law data is alternate digit inverted (ADI) and the  $\mu$ -Law magnitude data is in effect inverted. These techniques are used to ensure that there are sufficient data transitions for good clock recovery (not performed by the MV3100) on the Received side of the digital trunk lines when the channel is quiet.

**CONTROL INTERFACE (SEE FIGS. 5 AND 6))**

The Control Interface essentially has two sections. Firstly the serial/parallel input shift and address decode section, which controls the control registers. This is the Control Interface proper. Secondly, the reset section which generates a digital chip reset from the combination of 'hard' (i.e., power-on/pin generated) and 'soft' (i.e., programmed into the control registers) resets.

The data is serially clocked into the DATA input by the CLOCK input. The first 5 bits are the data to be stored and the second 3 bits identify which register is to be addressed. After the data has been clocked in, a separate ENABLE pulse stores the data in the appropriate register.

- The Control Interface has four inputs:
- CLOCK Control Interface clock
  - DATA Serial data input for the control registers
  - ENABLE Control Interface enable Signal
  - RESET See below

The RESET input is used to provide a full chip reset. The general rule is that, on reset, the chip is set to handset operation, minimum gain settings and all parts powered down, with the exception of the PLL and the  $V_{REF}$  ( $CR0 < 1$ ) which is powered up.

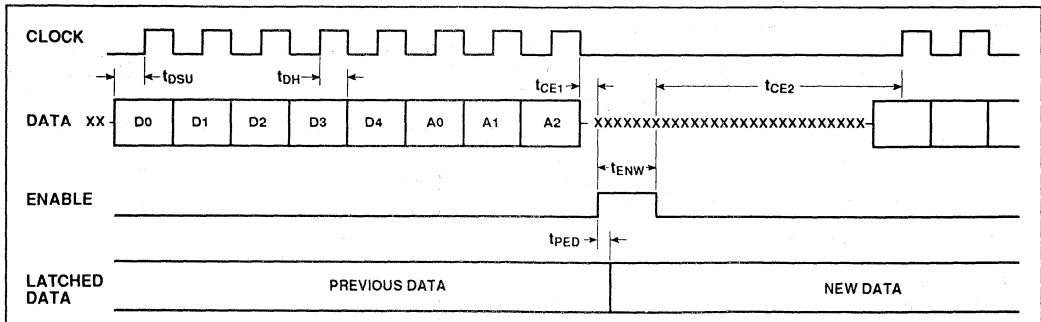


Fig. 5 Control Interface timing diagram

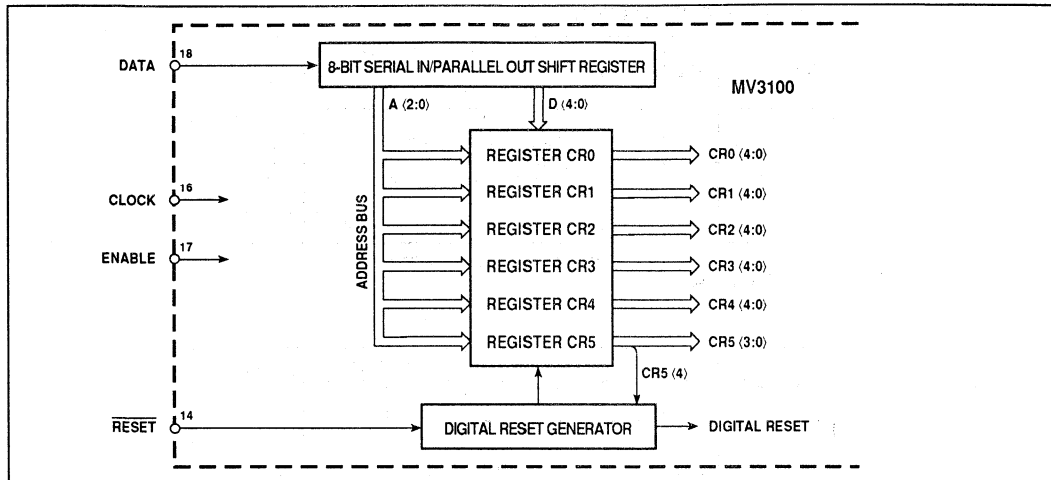


Fig. 6 Control Interface timing diagram

Parameter	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
CLOCK frequency	$f_{CK}$	32		2048	kHz		
CLOCK rise time	$t_{CKR}$		5		ns		
CLOCK fall time	$t_{CKF}$		5		ns		
CLOCK high time	$t_{CKH}$	200			ns		
CLOCK low time	$t_{CKL}$	200			ns		
DATA set-up time	$t_{DSU}$	3			ns		2
DATA hold time	$t_{DH}$	10			ns		2
CLOCK low to ENABLE high time	$t_{CE1}$	20			ns		2
ENABLE low to CLOCK high time	$t_{CE2}$	10			ns		2
ENABLE pulse width	$t_{ENW}$	200			ns		

Table 4 Control Interface timings

NOTES

- CLOCK must be low during the ENABLE pulse, otherwise false data will be stored.
- It is not strictly necessary for the clock pulses to be identical. So long as  $t_{DSU}$ ,  $t_{DH}$ , and min.  $t_{CKH}/t_{CKL}$  are met for every data bit, the waveform could actually be irregular.

CONTROL REGISTER FUNCTIONS (Tables 5 to 10)

Address	Bit	Function	Bit state		Reset value
			0	1	
000	0	Digital circuitry	Active	Standby	1
	1	PLL/V <sub>REF</sub>	Active	Standby	0
	2	Microphone amplifier	Active	Standby	1
	3	Loudspeaker amplifier	Active	Standby	1
	4	Auxiliary amplifier	Active	Standby	1

Table 5 Control register CR0 functions

Address	Bit	Function	Bit state		Reset value
			0	1	
001	0	Undefined			1
	1	Undefined			1
	2	Undefined			1
	3	Undefined			1
	4	Base Station mode	Off	On	0

Table 6 Control register CR1 functions

CONTROL REGISTER FUNCTIONS (continued)

Address	Bit	Function	Bit state		Reset value
			0	1	
010	0	Microphone amplifier (Transmit) gain setting bits (3:0) (See Table 14)			0
	1				0
	2				0
	3				0
	4	Reserved		Note 4	0

Table 7 Control register CR2 functions

NOTE 4: Not allowed

Address	Bit	Function	Bit state		Reset value
			0	1	
011	0	Loudspeaker amplifier (Receive) gain setting bits (4:0) (See Table 21)			0
	1				0
	2				0
	3				0
	4			0	

Table 8 Control register CR3 functions

Address	Bit	Function	Bit state		Reset value
			0	1	
100	0	Sidetone gain bits (1:0) (See Table 26)			1
	1				1
	2	Sidetone path	On	Off	1
	3	PLL clock enable	On	Off	1
	4	Auxiliary input	On	Off	1

Table 9 Control register CR4 functions

Address	Bit	Function	Bit state		Reset value
			0	1	
101	0	Transmit mute	Normal	Mute	1
	1	Receive mute	Normal	Mute	1
	2	PCM mode	Compand	Linear	1
	3	A/μ-Law	A-Law	μ-Law	1
	4	Digital reset	Normal	Reset	0

Table 10 Control register CR5 functions

**DETAILED SPECIFICATION**

These characteristics are guaranteed over the following conditions (unless otherwise stated):

$V_{DD} = 2.7V$  to  $3.6V$ ,  $T_{AMB} = -30^{\circ}C$  to  $+70^{\circ}C$  (see note 5)

**DC CHARACTERISTICS**

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Supply voltage	$V_{DD}$	2.7		3.6	V		8
Operating temperature	$T_{AMB}$	-30		+70	$^{\circ}C$		
Active power dissipation	$P_{OP}$		25	30	mW	$V_{DD} = 2.7V$	
			40	48	mW	$V_{DD} = 3.6V$	
Standby power dissipation	$P_{SB}$		3.8	4.0	mW	$V_{DD} = 2.7V$	9
			6.5	6.8	mW	$V_{DD} = 3.6V$	9
Powered down dissipation	$P_{DN}$		25	30	$\mu W$	$V_{DD} = 2.7V$	
			30	50	$\mu W$	$V_{DD} = 3.6V$	

Table 11

**NOTES**

- All electrical testing is performed at  $T_{AMB} = 25^{\circ}C$ .
- All detailed specification parameters apply for Linear PCM, A-Law PCM and  $\mu$ -Law PCM modes.
- Typical values shown are for the MV3100 operating in Linear mode only.
- All ground pins (pins 5, 10, 31 and 40) must be connected together to minimise any voltage difference between them. Similarly, all  $V_{DD}$  pins (pins 1, 11, 25 and 39) must be connected together.
- The Standby mode is with the PLL and  $V_{REF}$  powered up only.

**DIGITAL CHARACTERISTICS**

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Input low voltage	$V_{IL}$			0.2	$V_{DD}$		
Input high voltage	$V_{IH}$	0.75			$V_{DD}$		
Low level input current	$I_{IL}$			5	$\mu A$		10
High level input current	$I_{IH}$			5	$\mu A$		11
Output low voltage (TXOUT)	$V_{OL}$		0.2	0.4	V		
Output high voltage (TXOUT)	$V_{OH}$	0.75	0.9		$V_{DD}$		
Tristate leakage current (TXOUT)	$I_{OZ}$			< 10	$\mu A$		
Input capacitance	$C_{IN}$		5		pF		12
Output capacitance	$C_{OUT}$		5		pF		12

Table 12

**NOTES**

- All digital input pins except  $\overline{RESET}$ , which has a  $10k\Omega$  pull up resistor giving  $I_{IL\ max} = 400\mu A$ .
- All digital input pins.
- Not production tested.

**Master Clock Input**

The PLL Master Clock input (FIN, pin 38) will be capable of accepting a clock with jitter to the following specification:

- Over a defined 2ms period there will be exactly 64 cycles of the 32kHz clock.
- The maximum error between the ideal and actual clock edges will be three periods of 1.44MHz (2.1 $\mu s$ ).

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage, $V_{DD}$	-0.3V to +6V
Input voltage	-0.3V to $V_{DD}+0.3V$
Operating temperature	-40 $^{\circ}C$ to +85 $^{\circ}C$
Storage temperature	-55 $^{\circ}C$ to +125 $^{\circ}C$

**MV3100**

**TRANSMIT CHARACTERISTICS**

Transmit gain = nominal (see Table 14)

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Gain (MICIN to TXOUT)	A <sub>VTX</sub>		34.8		dBm0/dBV	1kHz	
Gain (MICIN to AUXOUT)	A <sub>VTA</sub>		19.9		dB	1kHz	
Gain variation with temperature	A <sub>VT</sub>	-1.0		+1.0	dB	-30°C to +70°C	13
Gain variation with supply	A <sub>VST</sub>	-0.5		+0.5	dB	2.7V to 3.6V	
Clipping level distortion	D <sub>CLT</sub>			1	%	Output = 3dBm0	13
Wide band noise	N <sub>WBT</sub>			-69	dBm0p		14
Narrow band noise	N <sub>NBT</sub>			-76	dBm0		13, 15
Power supply rejection ratio	PSRR	60			dB		13, 16
MICIN input impedance	Z <sub>IN</sub>		20		kΩ		13
AUXOUT load resistance	R <sub>LA</sub>	30			kΩ		
AUXOUT load capacitance	C <sub>LA</sub>			20	pF		
MICIN common mode rejection ratio	CMRR	40			dB		17

**NOTES**

- 13. Not production tested.
- 14. Bandwidth 300Hz to 3400Hz, psophometrically weighted
- 15. Any 10Hz band centred over the frequency range 305Hz to 3395Hz.
- 16. 20mVp-p sinewave at 500Hz applied to the positive supply.
- 17. 20mVp-p sinewave at 500Hz applied to both microphone input pins.

Table 13

**TRANSMIT GAIN CONTROL RANGE**

Nominal gain is highlighted

Control Word 2					Main path (dBm0/dBV)			Auxiliary path (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.	Min.	Typ.	Max.
X	0	0	0	0	22.6	22.8	23	7.7	7.9	8.1
X	0	0	0	1	23.6	23.8	24	8.7	8.9	9.1
X	0	0	1	0	24.6	24.8	25	9.7	9.9	10.1
X	0	0	1	1	25.6	25.8	26	10.7	10.9	11.1
X	0	1	0	0	26.6	26.8	27	11.7	11.9	12.1
X	0	1	0	1	27.6	27.8	28	12.7	12.9	13.1
X	0	1	1	0	28.6	28.8	29	13.7	13.9	14.1
X	0	1	1	1	29.6	29.8	30	14.7	14.9	15.1
X	1	0	0	0	30.6	30.8	31	15.7	15.9	16.1
X	1	0	0	1	31.6	31.8	32	16.7	16.9	17.1
X	1	0	1	0	32.6	32.8	33	17.7	17.9	18.1
X	1	0	1	1	33.6	33.8	34	18.7	18.9	19.1
X	1	1	0	0	34.6	34.8	35	19.7	19.9	20.1
X	1	1	0	1	35.6	35.8	36	20.7	20.9	21.1
X	1	1	1	0	36.6	36.8	37	21.7	21.9	22.1
X	1	1	1	1	37.6	37.8	38	22.7	22.9	23.1

Table 14

**TRANSMIT GAIN VARIATION WITH AMPLITUDE**

Frequency = 700Hz to 1100Hz

Input amplitude		Relative gain (dB)		
dBV	mVrms	Min.	Typ.	Max.
-89.4	0.034	-1.6		+1.6
-84.4	0.06	-0.6		+0.6
-74.4	0.19	-0.3		+0.3
-64.4	0.6	-0.3		+0.3
-54.4	1.9	-0.3		+0.3
-44.4	6.0		0	
-34.4	19.0	-0.3		+0.3
-31.4	27.0	-0.3		+0.3

Table 15

**TRANSMIT DISTORTION VARIATION WITH AMPLITUDE**

Frequency = 1020Hz

Input amplitude		Signal to distortion (dBp)		
dBV	mVrms	Min.	Typ.	Max.
-79.4	0.11	24		
-74.4	0.19	29		
-64.4	0.6	35		
-54.4	1.9	35		
-44.4	6.0	35		
-34.4	19.0	35		

Table 16

**TRANSMIT FREQUENCY RESPONSE -  
HANDSET MODE (SEE FIG. 7)**

Response relative to 1kHz. Input signal level = -34.8dBV.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		-22.3	-20
200		-13	-3
300	-10	-7.4	-2
1000	-3	0	
3000	-4	0	3.5
3400	-6	0	4
4000		-3.0	2

Table 17

**TRANSMIT FREQUENCY RESPONSE -  
BASE STATION MODE (SEE FIG. 8)**

Response relative to 1kHz. Input signal level = -34.8dBV.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		-14.2	-12
200		-5.9	-2
300	-5	-1.9	0
500	-1	0	1
1000	-1	0	1
3000	-1	0	1
3400	-6	-0.1	1
4000		-3.0	0

Table 18

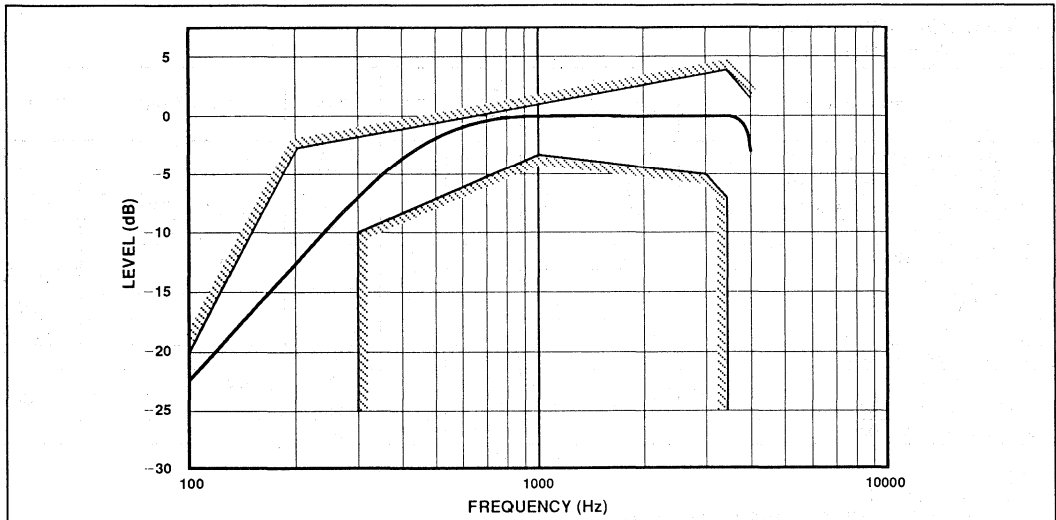


Fig. 7 Typical transmit frequency response - handset mode

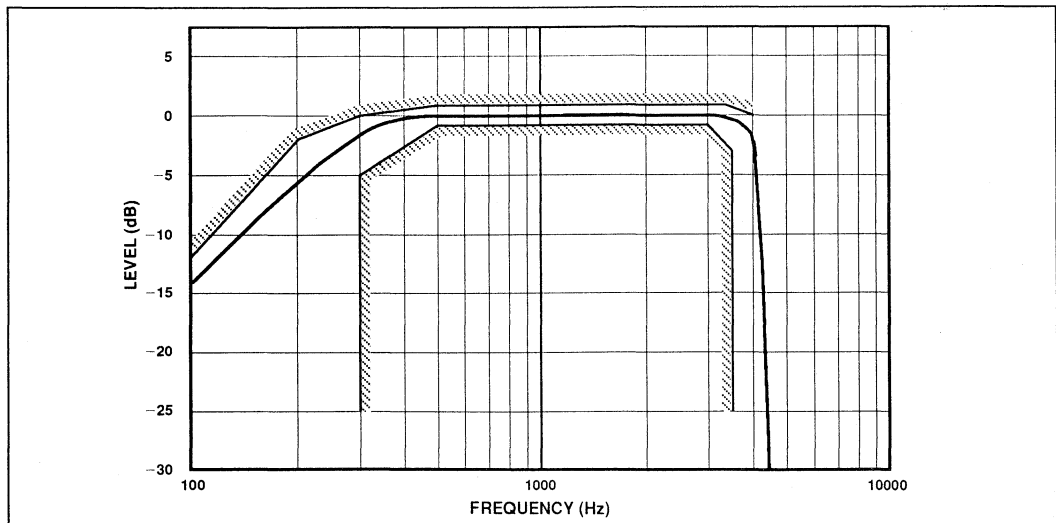


Fig. 8 Typical transmit frequency response - base station mode

**TRANSMIT OUT-OF-BAND SIGNAL**

Response relative to 1kHz. Input signal level = -34.8dBV.  
Output is total power relative to that for 1kHz.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
4650			-30
5000			-31.5
6000			-35
6500			-36
7000			-37.5
7500			-39

Table 19

**RECEIVE CHARACTERISTICS**

Receive gain = nominal (see Table 21)

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Gain (RXIN to LSOPP/LSOPN)	A <sub>VRX</sub>		-6.1		dBV/dBm0	1kHz	
Gain (AUXIN to LSOPP/LSOPN)	A <sub>VRA</sub>		13.4		dB	1kHz	
Gain variation with temperature	A <sub>VTR</sub>	-1.0		+1.0	dB	-30°C to +70°C	18
Gain variation with supply	A <sub>VSR</sub>	-0.5		+0.5	dB	2.7V to 5.5V	
Clipping level distortion	D <sub>CLR</sub>			<0.5	%	3dBm0, 1kHz	18
Wide band noise	N <sub>WBR</sub>			-72	dBVp		19
Narrow band noise	N <sub>NBR</sub>			-76	dB		18, 20
Signal out-of-band noise	N <sub>OBR</sub>	45			dB		21
AUXIN input impedance	Z <sub>INA</sub>		20		kΩ		
Sampling noise	N <sub>S</sub>			-79	dBV	At 8kHz	
Power supply rejection ratio	PSRR	26			dB		18, 22
Loudspeaker output load	Z <sub>L</sub>		88	105	nF		

Table 20

**NOTES**

- 18. Not production tested.
- 19. Bandwidth 300Hz to 3400Hz psophometrically weighted.
- 20. Any 10Hz band centred over the frequency range 305Hz to 3395Hz.
- 21. For an input signal of 0dBm0 at 1kHz, the ratio between the signal at 1kHz and any signal between 4kHz and 8kHz at the loudspeaker.
- 22. 20mVp-p sinewave at 500Hz applied to the positive supply.



**RECEIVE GAIN CONTROL RANGE**  
Nominal gain is highlighted

Control Word 3					Main path (dBV/dBm0)			Auxiliary path (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.	Min.	Typ.	Max.
0	0	0	0	0	-28.3	-28.1	-27.9	-8.8	-8.6	-8.4
0	0	0	0	1	-27.3	-27.1	-26.9	-7.8	-7.6	-7.4
0	0	0	1	0	-26.3	-26.1	-25.9	-6.8	-6.6	-6.4
0	0	0	1	1	-25.3	-25.1	-24.9	-5.8	-5.6	-5.4
0	0	1	0	0	-24.3	-24.1	-23.9	-4.8	-4.6	-4.4
0	0	1	0	1	-23.3	-23.1	-22.9	-3.8	-3.6	-3.4
0	0	1	1	0	-22.3	-22.1	-21.9	-2.8	-2.6	-2.4
0	0	1	1	1	-21.3	-21.1	-20.9	-1.8	-1.6	-1.4
0	1	0	0	0	-20.3	-20.1	-19.9	-0.8	-0.6	-0.4
0	1	0	0	1	-19.3	-19.1	-18.9	0.2	0.4	0.6
0	1	0	1	0	-18.3	-18.1	-17.9	1.2	1.4	1.6
0	1	0	1	1	-17.3	-17.1	-16.9	2.2	2.4	2.6
0	1	1	0	0	-16.3	-16.1	-15.9	3.2	3.4	3.6
0	1	1	0	1	-15.3	-15.1	-14.9	4.2	4.4	4.6
0	1	1	1	0	-14.3	-14.1	-13.9	5.2	5.4	5.6
0	1	1	1	1	-13.3	-13.1	-12.9	6.2	6.4	6.6
1	0	0	0	0	-12.3	-12.1	-11.9	7.2	7.4	7.6
1	0	0	0	1	-11.3	-11.1	-10.9	8.2	8.4	8.6
1	0	0	1	0	-10.3	-10.1	-9.9	9.2	9.4	9.6
1	0	0	1	1	-9.3	-9.1	-8.9	10.2	10.4	10.6
1	0	1	0	0	-8.3	-8.1	-7.9	11.2	11.4	11.6
1	0	1	0	1	-7.3	-7.1	-6.9	12.2	12.4	12.6
1	0	1	1	0	-6.3	-6.1	-5.9	13.2	13.4	13.6
1	0	1	1	1	-5.3	-5.1	-4.9	14.2	14.4	14.6
1	1	0	0	0	-4.3	-4.1	-3.9	15.2	15.4	15.6
1	1	0	0	1	-3.3	-3.1	-2.9	16.2	16.4	16.6
1	1	0	1	0	-2.3	-2.1	-1.9	17.2	17.4	17.6
1	1	0	1	1	-1.3	-1.1	-0.9	18.2	18.4	18.6
1	1	1	0	0	-0.3	-0.1	0.1	19.2	19.4	19.6
1	1	1	0	1	0.7	0.9	1.1	20.2	20.4	20.6
1	1	1	1	0	1.7	1.9	2.1	21.2	21.4	21.6
1	1	1	1	1	2.7	2.9	3.1	22.2	22.4	22.6

Table 21

**RECEIVE GAIN VARIATION WITH AMPLITUDE**

Frequency = 700Hz to 1100Hz

Input level (dBm0)	Relative gain (dB)		
	Min.	Typ.	Max.
-55	-1.6		+1.6
-50	-0.6		+0.6
-40	-0.3		+0.3
-30	-0.3		+0.3
-20	-0.3		+0.3
-10		0	
0	-0.3		+0.3
3	-0.3		+0.3

Table 22

**RECEIVE DISTORTION VARIATION WITH AMPLITUDE**

Frequency = 1020Hz

Input level (dBm0)	Signal to distortion (dBp)		
	Min.	Typ.	Max.
-45	24		
-40	29		
-30	35		
-20	35		
-10	35		
0	35		

Table 23

**RECEIVE FREQUENCY RESPONSE (SEE FIG. 9)**

Response relative to 1kHz. Signal level = -16dBm0.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		-22.2	-20
160		-11	-6
300	-5	-2	0
500	-1	0.2	1
1000		0	
3000	-1	0	1
3400	-6	0.2	1
4000		-3.0	0

Table 24

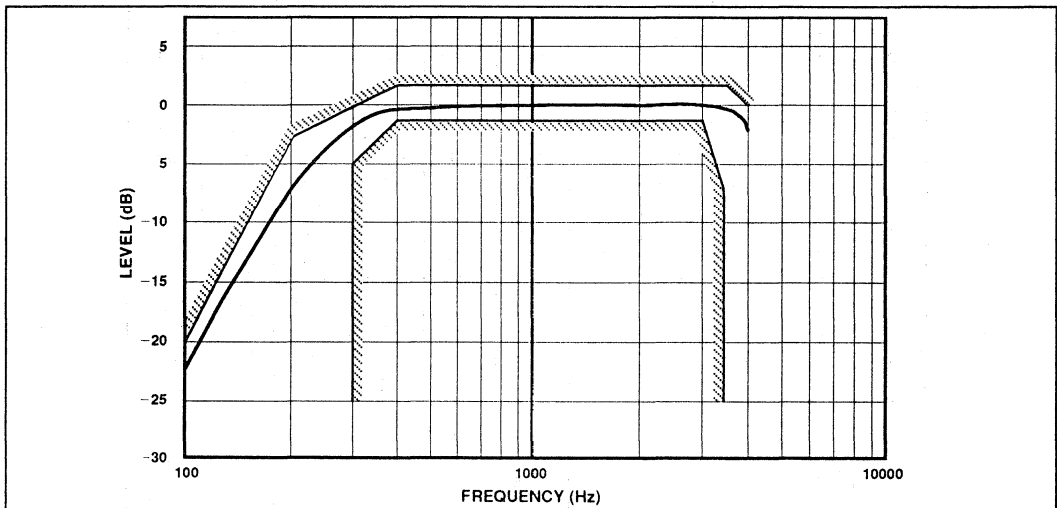


Fig. 9 Typical receive frequency response

**BIDIRECTIONAL CHARACTERISTICS**

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Sidetone gain	A <sub>S</sub>		25.7		dB		
Gain variation with temperature	A <sub>ST</sub>	-2.0		+2.0	dB		23
Gain variation with supply	A <sub>SS</sub>	-1.0		+1.0	dB		
Crosstalk, Tx to Rx	X <sub>TR</sub>		-60		dB	No sidetone	
Crosstalk, Rx to Tx	X <sub>RT</sub>		-60		dB		

Table 25

NOTE 23. Not production tested.

**SIDETONE GAIN CONTROL RANGE**

Nominal gain is highlighted

Control Word 4					Sidetone gain (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.
X	X	0	1	1	28.3	28.7	29.1
X	X	0	1	0	25.3	25.7	26.1
X	X	0	0	1	22.3	22.7	23.1
X	X	0	0	0	19.3	19.7	20.1
X	X	1	X	X			-35

Table 26

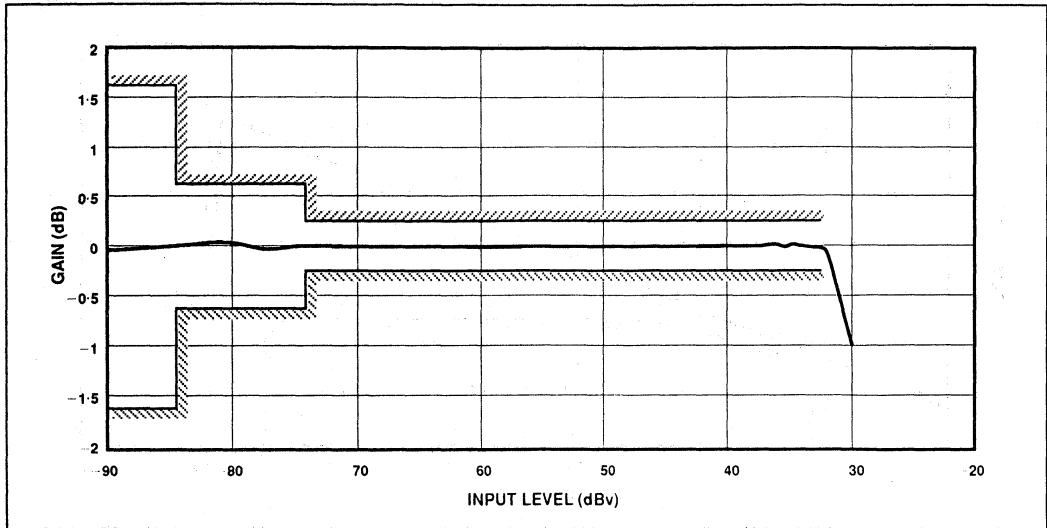


Fig. 10 Typical transmit path gain v. input level. Signal frequency = 1.0kHz

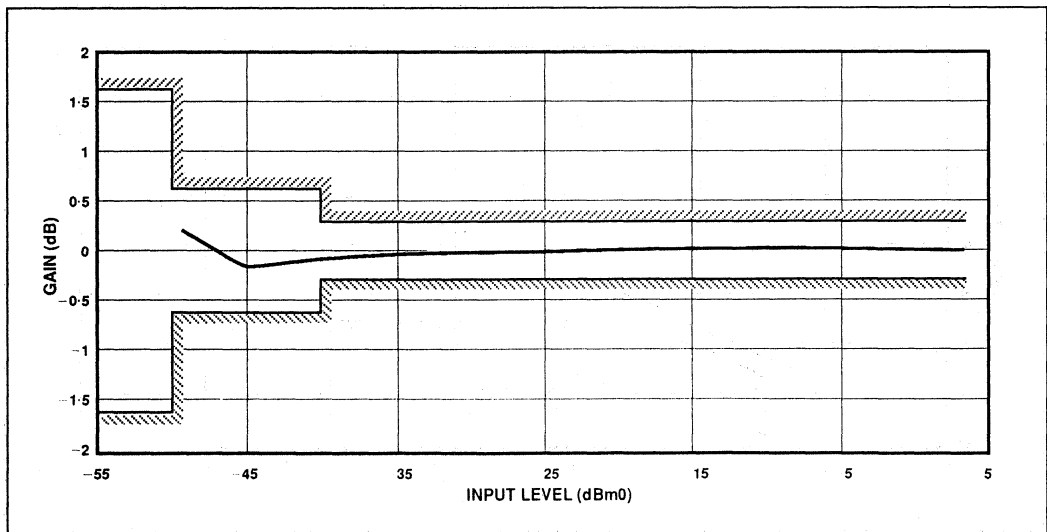


Fig. 11 Typical receive path gain v. input level. Signal frequency = 1.0kHz

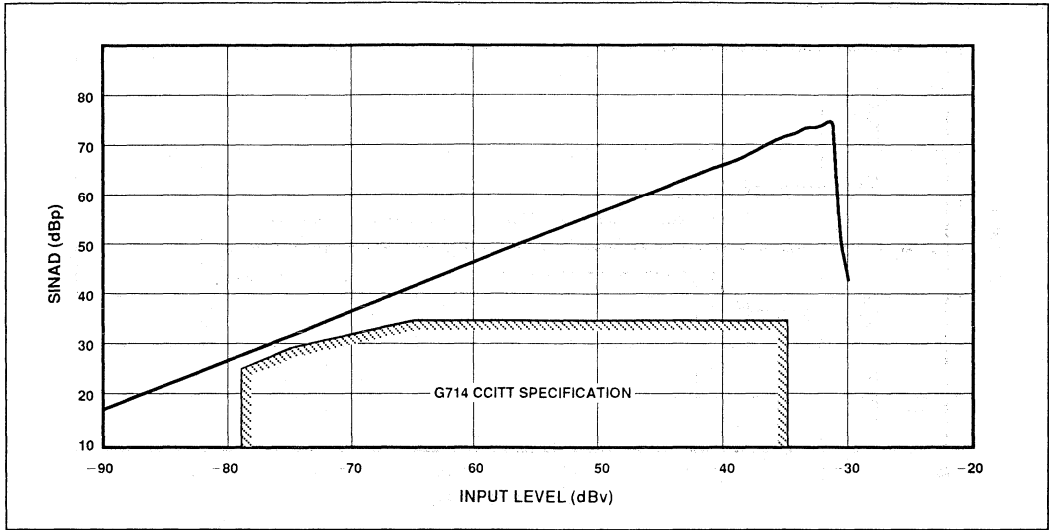


Fig. 12 Typical transmit path SINAD v. input level. Signal frequency = 1.0kHz

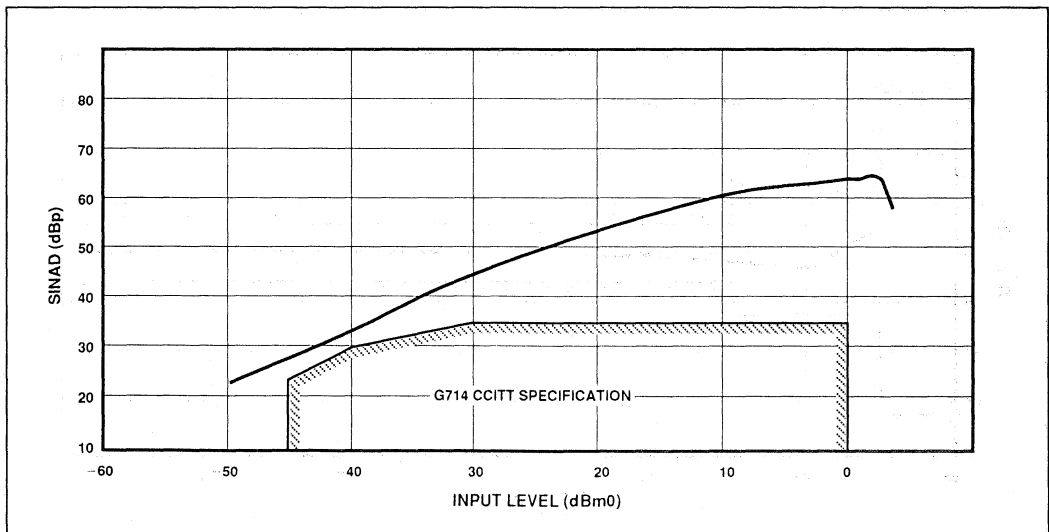


Fig. 13 Typical receive path SINAD v. input level, over full specification range. Signal frequency = 1.0kHz

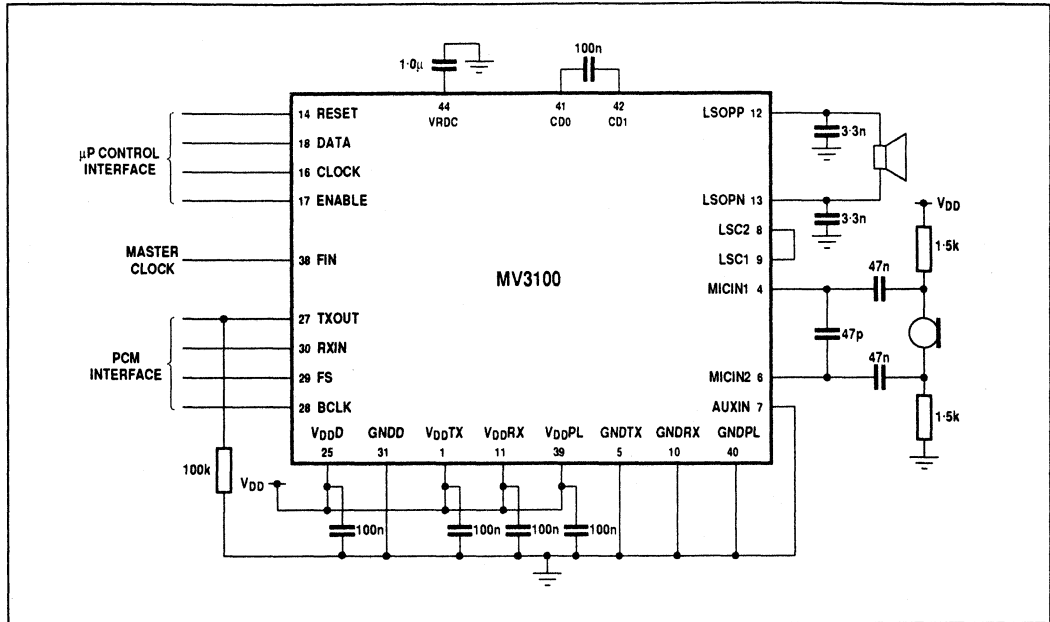


Fig. 14 Typical handset application circuit



# Section 7

## Paging Receivers & Decoders



1. The first part of the document discusses the importance of maintaining accurate records of all transactions.

2. It also emphasizes the need for regular audits to ensure the integrity of the financial data.

3. Finally, it concludes by stating that these practices are essential for the long-term success of any business.



# MV6639

## POCSAG DECODER

(Supersedes November 1992 edition - DS2464 - 3.3)

The MV6639 POCSAG decoder is capable of operating at 512 or 1200 baud. This device together with a suitable receiver, provides the major components for a POCSAG pager.

POCSAG is the acronym for Post Office Code Standardisation Advisory Group. The POCSAG code is the most accepted radio paging standard, (CCIR RPC No.1) and provides for over 2 million pager IDs, two of which may be held in this device. The POCSAG code format is shown in figure 3.

The design is optimised for very low power, low voltage use. Advanced features allow the decoder to be used in a wide range of applications.

The pinout and architecture are shown in figures 1 and 2.

### FEATURES

- Low voltage supply (1V min, 3.5V max)
- Low current consumption (Typically 15µA)
- Voltage doubler for radio receiver or µP and Display
- True 2 bit CRC error correction
- Tone only and/or messaging pager at 512 or 1200 baud using a single 32768Hz crystal
- Silent call storage
- Directly drives tone transducer
- Programmable tone generator output frequency (2048 or 2731 Hz)
- Interface to SL6609 radio receiver chip
- Low battery alert

### APPLICATIONS

- Wrist watch pager
- Message display pager
- Tone only pager
- Data receivers

### ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD2 - GND)	-0.5V to 5V
Voltage on any pin	-0.3V to VDD2 + 0.3V
Operating temperature	-20°C to + 70°C
Storage temperature	-55°C to +125°C

### ORDERING INFORMATION

- MV6639/KG/NPDS - devices in anti-static sticks
- MV6639/KG/NPDE - devices in tape & reel

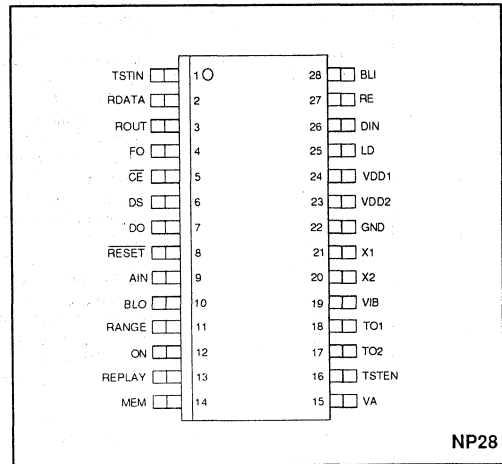


Fig. 1 Pin connection (top view - not to scale)

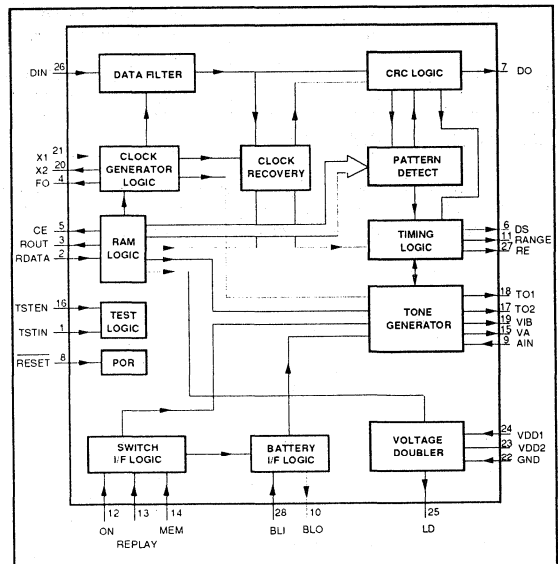


Fig. 2 MV6639 Block Diagram

# MV6639

## Pin Description.

Pin No	Pin Name	Pin Description
1	TSTIN	Test input. Held low for normal operation.
2	RDATA	Data input from external E <sup>2</sup> PROM.
3	ROUT	Reset to external E <sup>2</sup> PROM.
4	FO	Crystal frequency divided by two clock output. Mainly used for reading data from an external E <sup>2</sup> PROM into the internal memory.
5	CE	Chip enable signal for external E <sup>2</sup> PROM.
6	DS	Data Strobe. This output goes active high prior to each bit of valid message data being transmitted on DO.
7	DO	Data Output. Valid address and message data is output on this pin.
8	RESET	This pin is used to activate the power on reset circuit. A capacitor between this pin and GND sets the reset time when powered up. The device may also be externally reset from this input.
9	AIN	Alert in. One of two inputs to the tone generator circuit. This input when high produces a continuous tone at the two tone outputs.
10	BLO	Battery level output. This goes high if battery level input (BLI) is high for 8ms.
11	RANGE	If no preamble or sync word is detected for 60 batches, the range output goes high.
12	ON	Decoder is switched 'ON' by holding this pin high.
13	REPLAY	Pulsed high to cancel tones or replay calls.
14	MEM	Decoder is switched to 'MEM' (memory or 'silent' mode) by holding this pin high.
15	VA	Visual alert. Pulses high to indicate incoming call when in silent mode. Can be used to drive an LED.
16	TSTEN	Test input active high. Hold low during normal operation.
17	TO2	The beep codes and alerts are output on this pin. The output configuration and tone output frequencies are programmable.
18	TO1	The beep codes and alerts are output on this pin. The output configuration and tone output frequencies are programmable.
19	VIB	Output to external bipolar vibrator driver when in silent mode.
20	X2	Crystal oscillator output.
21	X1	Crystal oscillator input.
22	GND	Negative supply input.
23	VDD2	Positive supply, doubled if voltage doubler active, otherwise connected to VDD1.
24	VDD1	Positive supply input (1V min).
25	LD	Connect external inductor and diode for voltage doubler if required.
26	DIN	This is the serial data input to the device. 512 or 1200 baud non-inverted POCSAG data.
27	RE	Receiver Enable. This output when low powers down or disables the receiver to save power.
28	BLI	Battery level input from receiver. Normally low. The high level indicates battery flat and triggers a tone if high for 8ms.

## DECODER APPLICATIONS

The MV6639 can be used in either a "Tone Only" or a "Tone and Message" pager. When used in tone only applications, the only additional IC requirements are a receiver (such as the SL6609) and a small E<sup>2</sup>PROM (primarily for holding the pager identification). A full tone and message pager can be implemented with the addition of a simple microprocessor/LCD driver.

**THE POCSAG CODE**

A transmission of POCSAG code consists of at least 576 bits of preamble, i.e. alternate 1010s, followed by batches of codewords, each batch starting with a synchronisation codeword (SC) followed by 8 frames of data. (see figure 3a).

Each frame consists of 2 codewords, where the pager ID's 3 least significant bits correspond to the frame number in the batch.

Each codeword consists of 32 bits as shown in figure 3b. There are two types of codeword, address and message.

The SC and IC are special cases of address codewords. Bits 20-21 of the address codeword transmitted determine the tone cadence pattern to be output by the decoder.

Message codewords immediately follow their particular address and are only displaced by the SC. An idle codeword (IC) is transmitted in the absence of an address or message codeword. In a message sequence, the end of the message is denoted by another address or idle codeword.

The format of message data output by the decoder is shown in figure 3d.

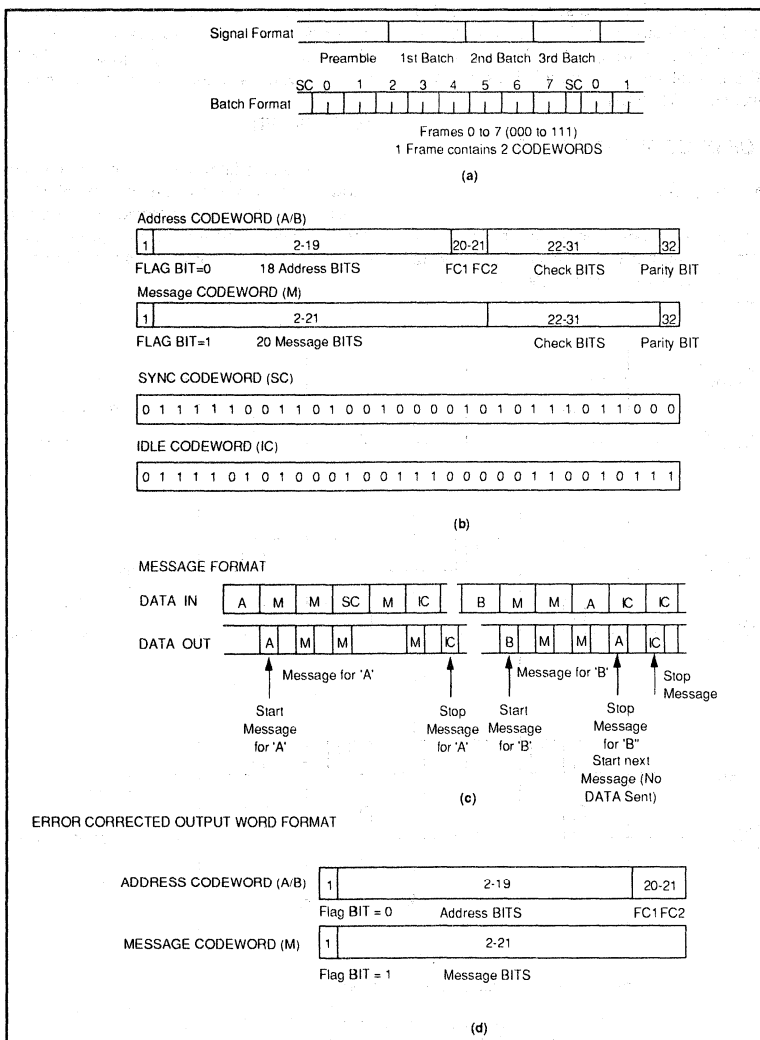


Fig. 3 POCSAG Data Format

**POCSAG CODE SYNCHRONISATION**

After the decoder has been powered up and the 2 ID's programmed, synchronisation to the incoming POCSAG data is performed. Once bit synchronisation is achieved by the clock recovery circuit, the data stream is checked bitwise for the sync codeword (SC).

When the SC is found, the receiver is disabled until the frame in which either of the two ID's occurs. The receiver (RX), is then turned on to look for an ID and any valid message is decoded.

If SC is not found, a search procedure is initiated. The receiver is enabled for one frame in 9 to search for either SC or preamble. If, after 60 such search cycles, SC or preamble have not been detected, the out of range (RANGE) signal goes active high. RANGE is reset if SC or preamble is detected or the decoder is switched to STANDBY.

**DESCRIPTION OF DECODER CIRCUITS**

**CLOCK GENERATOR LOGIC**

Most of the required clock signals for the chip are produced by the clock generator circuit, from the 32768Hz crystal controlled oscillator. These are as follows:-

- 32.768 kHz for clock recovery
- 16.384 kHz clock ref. output (FO)
- 2048/2731 Hz (programmable) for the tone generator
- 16 Hz to control tone cadencing

Clocks will be disabled as required depending on the mode of operation of the device.

An external clock may be applied to X1 if X2 is left open circuit. Note that X1 has non-standard input thresholds.

**CLOCK RECOVERY**

The clock recovery circuit produces a clock signal correctly synchronised to the incoming data. The circuit is similar in operation to a digital phase locked loop. This circuit together with the timing logic monitors and maintains bit sync.

**DATA FILTER**

The data filter digitally cleans up the incoming data as shown in figure 4 and works with the clock recovery circuit to synchronise the internal clocks to the incoming data. The circuits minimise the effects of edge jitter and "drop-outs" in the data, which can occur at low signal levels.

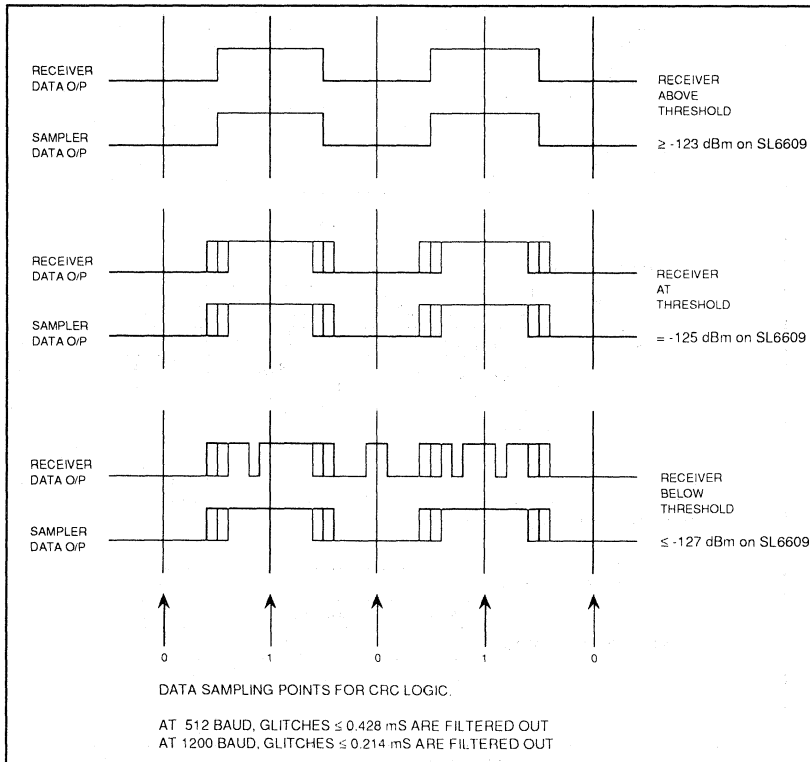


Fig. 4 Data Filter Operation

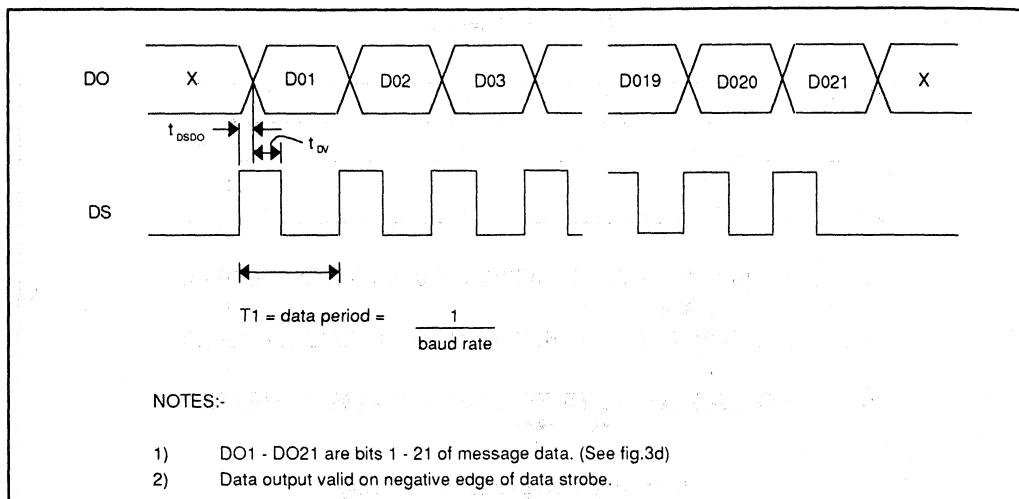


Fig. 5 Data Output Timing

### CRC LOGIC

This circuit receives the incoming serial data and performs 2 bit CRC error correction according to the POCSAG standard on all incoming data. Together with the timing logic and pattern detector, this circuit maintains word sync and outputs corrected message data clocked on a positive edge of data strobe (DS) as shown in figure 5. If more than two errors are detected, no attempt is made at corrections and the data is outputted uncorrected with no indication of error.

### PATTERN DETECTOR

This circuit operates on checked and corrected data. It receives data and checks for SC, IC or either of the two programmed pager addresses.

### TIMING LOGIC

This logic provides the bit, word and batch frame sync in conjunction with the pattern detector, CRC logic and clock recovery circuit. The timing logic also generates the receiver enable (RE), data strobe (DS) and out-of-range (RANGE), output signals. RE goes active one word at 1200 baud, half word at 512 baud, before the address is expected to allow time for the receiver to power up.

### RAM LOGIC

The RAM stores 48 control bits which are automatically read from an external E<sup>2</sup>PROM on power up. The first 18 bits are address A (A0-17) which is read in LSB first. This is followed by 3 frame position bits (AF2-0) which tell the device which frame to look in for address A. These are read in MSB first. These values are followed by address B and its frame position bits. The last 6 bits are function bits which are used

to configure the device. FB1 is read first. If addresses are expected in only one particular frame, the AF and BF bits should be set to the same value to conserve power. The function bits are used for programming silent override of selected pager ID's, 512/1200 baud operation, voltage doubler enable/disable and tone generator operation. Figure 6 shows the function bit allocation. The decoder RAM and E<sup>2</sup>PROM timing is shown in figure 7.

Function Bit	Feature
FB 1	Data rate select 0: 1200 baud. 1: 512 baud.
FB 2	Voltage Doubler 0: Disabled. 1: Enabled.
FB 3	Silent Override on addr 'A'. 0: Enabled. 1: Disabled.
FB 4	Silent Override on addr 'B'. 0: Enabled. 1: Disabled.
FB 5	Tone Gen Freq 0: 2048Hz 1: 2731Hz
FB 6	Tone output configuration 0: Two Tone Levels 1: Single Tone Level

Fig. 6 Function BIT Allocation

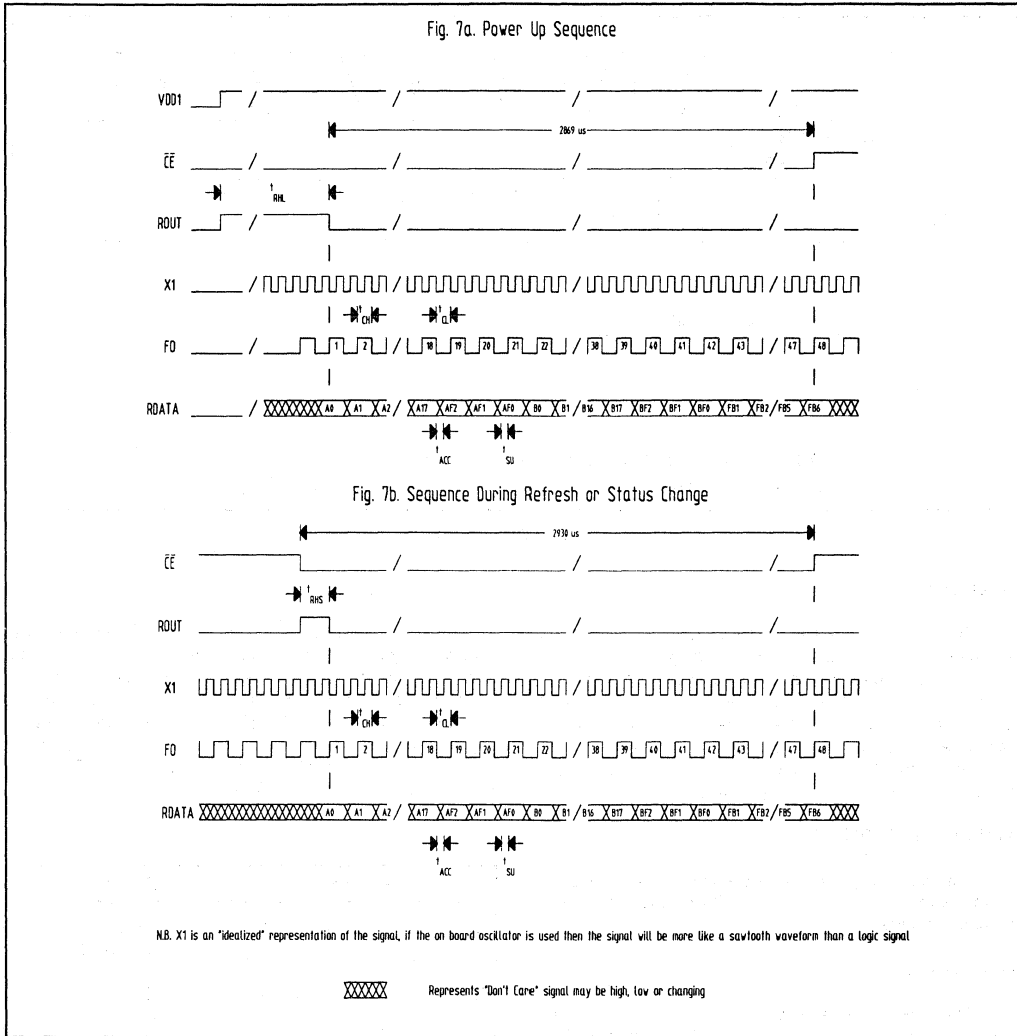


Fig. 7 E<sup>2</sup>PROM Read Operation

On power up, a reset pulse is generated from the charging of a capacitor connected to the decoder RESET pin. This pulse sets the decoder in a defined state and initiates the loading of the E<sup>2</sup>PROM contents into the decoder's internal memory. The reset pulse ROUT is high for approximately 3 seconds. This extended period is to allow the on chip voltage doubler (if enabled) to attain its correct doubled output voltage. The E<sup>2</sup>PROM used may only operate down to a minimum supply of 2V, thus any attempt to read data from the memory before this voltage is available from the doubler may result in corrupt data being loaded into the decoder. Even an

E<sup>2</sup>PROM operating down to 1V supply could give a faulty read output if the ROUT hold off pulse is short as the limited voltage out of the doubler at power up is below VDD1 (battery) voltage. Fig.7a shows the E<sup>2</sup>PROM read operation for the power up sequence. CE is low and a reset pulse is output to the external memory device. Then data is clocked into the MV6639 on positive edges of the 16384 Hz output pin 'FO'. After 48 bits have been written into chip memory, CE goes high to disable the external memory and the programming sequence is terminated.

Mechanical shock can cause a temporary disconnection of the pager power supply. To guard against the decoder RAM contents being corrupted, the RAM is automatically reloaded every four minutes. If the pager is receiving at the 4 minute refresh time, the reload is delayed until the receiver is disabled. In addition, a reload operation is performed whenever the status of the decoder is switched from STANDBY to ON or MEM modes.

For the automatic and change of status reloads, the doubler (if enabled) will already have achieved its correct output voltage and it is unnecessary to provide a long holdoff ROUT pulse to the E<sup>2</sup>PROM. The memory read sequence for the 4 minute refresh or status change is shown in Fig. 7b.

### BATTERY INTERFACE LOGIC

The decoder will accept a 'battery low' flag from a radio receiver on the BLI pin. The decoder samples the state of this pin at 256 Hz when the receiver is enabled, as shown in figure 8. The tone generator will output a 16 second continuous signal if BLI input is high (battery fail condition) for 3 or more consecutive samples. In addition, a battery low flag is output on the BLO pin. Note that any active tone generator and BLO output can be cancelled by pulsing the REPLAY/CANCEL input pin. The low battery detection circuit will be re-armed whenever decoder status is changed from STANDBY to ON or MEM.

### TEST LOGIC

Test logic is included as required to supplement the inherent testability and fault coverage of the device during manufacture.

### POWER ON/OFF AND SWITCH INTERFACE LOGIC

There are three operating modes for the decoder, STANDBY, ON and MEM (memory). When the decoder is required to be OFF it is preferable to disconnect the battery supply to the decoder, as shown in figure 14, to conserve battery power. If STANDBY mode is used the crystal oscillator and voltage doubler (if programmed ON) continue to operate but FO output is disabled.

MEM or 'Silent' mode is selected if the user wishes to store incoming calls rather than producing alert tones immediately the pager recognises a valid address. MEM mode is activated with a logic '1' on the MEM pin. The tone outputs TO1, TO2 are inhibited and the vibrator (VIB) and Visual Alert (VA) outputs enabled. The silent mode can be overridden on either address A or B by setting the appropriate silent override bit read into the internal RAM (see figure 6). In the MEM mode up to four incoming calls can be stored.

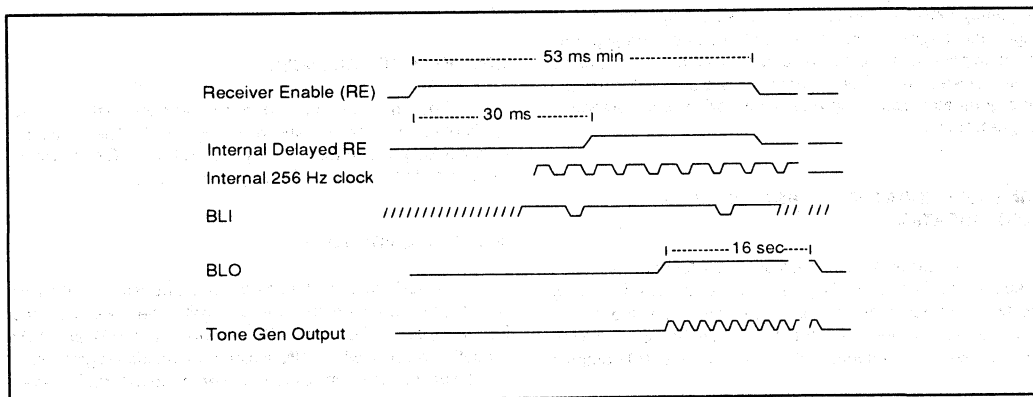


Fig. 8 Battery Low Detect Circuit Timing

## MV6639

The Switch Interface logic truth table is shown in figure 9 below:



ON	MEM	REPLAY	Decoder Status
0	0	0	Decoder off. No messages received. (STANDBY mode)
1	0	0	Decoder active. Messages received and decoded. (ON mode)
X	1	0	Decoder active and in silent / store call mode. (MEM mode)
1	0		Replay stored calls / cancel current tones.
X	1		Cancel current tones or Vibrator and Visual Alert outputs.

Fig. 9 Decoder Status Truth Table

In ON mode pulsing REPLAY to a logic '1' replays stored call(s). Pulsing the REPLAY input will also cancel any current tone, vibrator or visual alert outputs.

Further details on the MEM and REPLAY tone vibrator and visual alert output cadences are covered in the next section.

Different tone patterns are generated when changing the status of the pager (eg from 'ON' to 'MEM'). These too are covered in the tone generation section.

Contact debounce circuitry is included in all switch and push button interfaces.

### tone vibrator and visible alert signal generation

The tone generator block produces audio or low frequency vibrator signals in response to the state of the pager, messages, or battery level (if low). Four paging tone cadence patterns are provided and also the ability to output a continuous alert tone. Two volume levels are available and the tone generator frequency and output drive configuration is programmable.

### tone and vibrator generator output configuration

The internal tone generator circuit feeds an external beeper via the TO1 and TO2 pins. Figures 10 (a) and (b) show the two common methods of beeper interface. Fig 10 (a) shows a high efficiency resonant drive circuit with one fixed volume level. In this configuration the TO1 and TO2 outputs

are push - pull, switching in anti - phase. Fig 10 (b) shows a more flexible drive network which delivers two different power levels to the transducer. This mode is selected by clearing bit 6 of the function register low (Figure 6). When an alert tone is output, TO2 stays low for the first six seconds and TO1 switches in accordance with the cadence pattern, producing a low level tone. For the next ten seconds TO2 also switches, producing a high tone level.

The vibrator output VIB drives an external bipolar transistor with vibrator alerter as shown in figure10(c).

### tone frequency

This can be customer specified at either 2048Hz or 2731Hz. The control bit FB5 which determines which frequency is used, is set in the external E<sup>2</sup>PROM and read into the decoder memory (see figure 6).

### paging tone cadences

Four different paging tone cadence patterns are available and these are shown in Figure 12. The particular cadence output is determined by the FC1 and FC2 bits which form part of the address codeword (Figure 3).

### alert override tone

Direct input of cadence patterns is possible via the AIN pin. A high input on this pin will gate the selected tone frequency to the TO1 and TO2 outputs. Both TO1 and TO2 outputs are active when AIN is high and function register bit 6 is set high, to deliver maximum power to the external beeper.

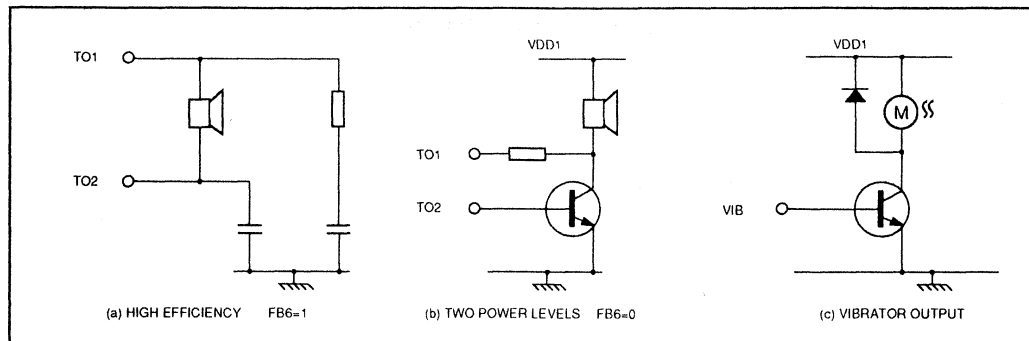


Fig. 10 Tone Generator / Vibrator Interface Circuits



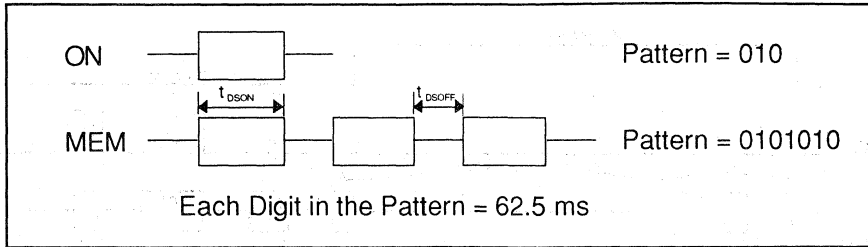


Fig. 11 Decoder Status Tones

**PAGER STATUS TONE GENERATION**

The decoder produces tones to acknowledge a change in its status. When ON is selected the decoder will output a single short tone as shown in figure 11. In the ON, (or active) mode the decoder is able to receive and decode messages. Received calls are compared with the two user addresses assigned to the pager. These are programmed into the external E<sup>2</sup>PROM and read into the decoders internal memory.

receiving a message in the MEM mode, the device can be switched to ON mode to hear the remainder of the 16 second tone. The tone is also stored for REPLAY at a more convenient time. Pulsing REPLAY before the 16 second tone cadence has been completed will automatically cancel the current tone and replay the next tone as shown in figure 13. Whatever the pager status, a tone output, vibrator or visible alert can be cancelled by pulsing the REPLAY input.

Setting the decoder to the MEM (or SILENT) state is indicated by three short tones. This operating mode is similar to the ON condition except that audio alert tones (cadences) are inhibited. Instead, the external vibrator alerter is activated by providing an 8Hz drive signal out of the VIB pin (see figure 10). A visible alert can be generated by feeding the VA output into the external buffer transistor and LED. VA is pulsed high as shown in figure 13. Up to four alert cadence calls can be stored in the decoder and these calls can be successively replayed by switching from MEM to ON and supplying pulses to the REPLAY input. When the vibrator output is active after

Priority messages can be programmed to override the silent mode. Two of the six 'Function bits' (figure 6) programmed into the external E<sup>2</sup>PROM, control the silent override for address A and B.

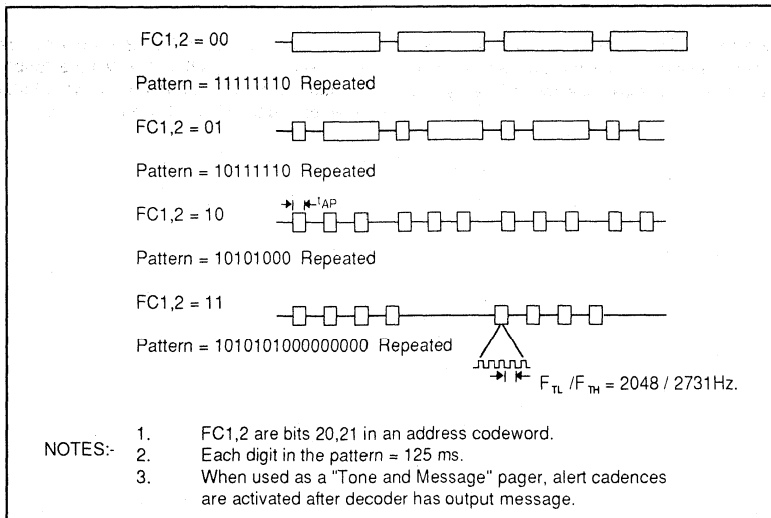


Fig. 12 Alert Cadences

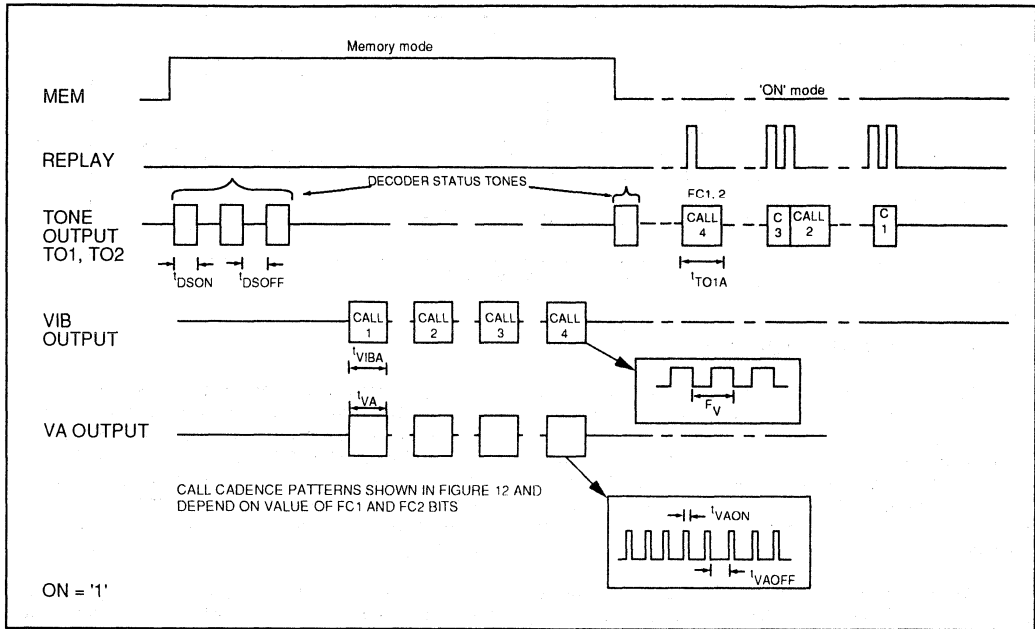


Fig. 13 Recall / Cancel of Stored Calls

**VOLTAGE DOUBLER**

The decoder is capable of operating with a supply between 1 and 3.5V. Other devices in the pager, for example the receiver, may require a higher voltage than 1V. The voltage doubler enables these devices to be used without additional circuitry.

The voltage conversion is performed by charging an inductor, then discharging it through a diode onto a reservoir capacitor on the output. To maximise the efficiency the

resistance of the inductor and the forward voltage drop of the diode should be as low as possible. The diode should therefore be a schottky diode. The inductor used in the test and evaluation circuits has a DC resistance of less than 20 ohms.

The voltage on VDD2 should not exceed 3.5V, so VDD1 should be less than 1.75V if the doubler is enabled. If the doubler is not used VDD1 and VDD2 should be shorted together and the LD pin left open circuit.

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
<b>SUPPLY CURRENT</b>						
Decoder on	$I_{VDD}$		10	14	$\mu\text{A}$	
<b>INPUT LOGIC HIGH</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IH}$	0.90			V	
BLI, DIN	$V_{IH}$	0.70			V	
NRESET	$V_{IH}$	0.90			V	
X1	$V_{IH}$	0.90			V	
<b>INPUT LOGIC LOW</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IL}$			0.20	V	
BLI, DIN	$V_{IL}$			0.30	V	
NRESET	$V_{IL}$			0.30	V	
X1	$V_{IL}$			0.20	V	
<b>LOGIC HIGH INPUT CURRENT</b>						
ON, MEM, REPLAY	$I_{IH}$		0.01	1	$\mu\text{A}$	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	$I_{IH}$		0.13	1	$\mu\text{A}$	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	$I_{ILH}$		0.01	1	$\mu\text{A}$	$V_{IH} = V_{VDD1}$
<b>LOGIC LOW INPUT CURRENT</b>						
All inputs except NRESET	$I_{ILL}$		-0.01	-1	$\mu\text{A}$	$V_{IL} = 0\text{V}$
NRESET	$I_{IL}$		-5.48	-10	$\mu\text{A}$	$V_{IL} = 0\text{V}$ internal pullup
<b>OUTPUT LEVELS, HIGH</b>						
All outputs except TO1, TO2, VIB	$V_{OH}$	0.90	0.99		V	$I_{LOAD} = 10\mu\text{A}$
TO1, TO2, VIB	$V_{OH}$	0.90	0.98		V	$I_{LOAD} = 10\mu\text{A}$
<b>OUTPUT LEVELS LOW</b>						
All outputs	$V_{OL}$		0.03	0.10	V	$I_{LOAD} = -10\mu\text{A}$
<b>OUTPUT CURRENTS LOW</b>						
TO1	$I_{OL}$	1.50			$\text{mA}$	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	$I_{OL}$	0.30			$\text{mA}$	$V_{OUT} = V_{DD1}/2$
<b>OUTPUT CURRENTS HIGH</b>						
TO1, TO2, VIB	$I_{OH}$	0.30			$\text{mA}$	$V_{OUT} = V_{DD1}/2$
VA	$I_{OH}$	0.20			$\text{mA}$	$V_{OUT} = V_{DD1}/2$

**NOTES**

1. These inputs have internal pullup or pulldown resistors.

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
<b>SUPPLY CURRENT</b>						
Decoder on	$I_{VDD}$		14	22	$\mu\text{A}$	
<b>INPUT LOGIC HIGH</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IH}$	1.2			V	
BLI, DIN	$V_{IH}$	1.0			V	
NRESET	$V_{IH}$	1.2			V	
X1	$V_{IH}$	0.9			V	
<b>INPUT LOGIC LOW</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IL}$			0.3	V	
BLI, DIN	$V_{IL}$			0.5	V	
NRESET	$V_{IL}$			0.5	V	
X1	$V_{IL}$			0.2	V	
<b>LOGIC HIGH INPUT CURRENT</b>						
ON, MEM, REPLAY	$I_{IH}$		0.01	1	$\mu\text{A}$	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	$I_{IH}$		0.6	5	$\mu\text{A}$	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	$I_{ILH}$		0.01	1	$\mu\text{A}$	$V_{IH} = V_{VDD1}$
<b>LOGIC LOW INPUT CURRENT</b>						
All inputs except NRESET	$I_{ILL}$		0.01	-1	$\mu\text{A}$	$V_{IL} = 0\text{V}$
NRESET	$I_{IL}$		-20	-40	$\mu\text{A}$	$V_{IL} = 0\text{V}$ internal pullup
<b>OUTPUT LEVELS, HIGH</b>						
All outputs except TO1, TO2, VIB	$V_{OH}$	1.3	1.5		V	$I_{LOAD} = 10\mu\text{A}$
TO1, TO2, VIB	$V_{OH}$	1.3	1.5		V	$I_{LOAD} = 10\mu\text{A}$
<b>OUTPUT LEVELS LOW</b>						
All outputs	$V_{OL}$		0.03	0.15	V	$I_{LOAD} = -10\mu\text{A}$
<b>OUTPUT CURRENTS LOW</b>						
TO1	$I_{OL}$	5			mA	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	$I_{OL}$	1			mA	$V_{OUT} = V_{DD1}/2$
<b>OUTPUT CURRENTS HIGH</b>						
TO1, TO2, VIB	$I_{OH}$	1.5			mA	$V_{OUT} = V_{DD1}/2$
VA	$I_{OH}$	1			mA	$V_{OUT} = V_{DD1}/2$

## NOTES

- These inputs have internal pullup or pulldown resistors.

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 3.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
<b>SUPPLY CURRENT</b>						
Decoder on	$I_{VDD}$		41	71	$\mu A$	
<b>INPUT LOGIC HIGH</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IH}$	2.8			V	
BLI, DIN	$V_{IH}$	2.0			V	
NRESET	$V_{IH}$	3.0			V	
X1	$V_{IH}$	0.9			V	
<b>INPUT LOGIC LOW</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IL}$			0.8	V	
BLI, DIN	$V_{IL}$			1.2	V	
NRESET	$V_{IL}$			1.5	V	
X1	$V_{IL}$			0.2	V	
<b>LOGIC HIGH INPUT CURRENT</b>						
ON, MEM, REPLAY	$I_{IH}$		0.1	1	$\mu A$	Note 1. $V_{IH} = V_{VDD1}$
TSTIN, TSTEN, AIN, NRESET	$I_{IH}$		5.5	10	$\mu A$	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	$I_{ILH}$		0.05	1	$\mu A$	$V_{IH} = V_{VDD1}$
<b>LOGIC LOW INPUT CURRENT</b>						
All inputs except NRESET	$I_{ILL}$		-0.05	-1	$\mu A$	$V_{IL} = 0V$
NRESET	$I_{IL}$		-180	-300	$\mu A$	$V_{IL} = 0V$ internal pullup
<b>OUTPUT LEVELS, HIGH</b>						
All outputs except TO1, TO2, VIB	$V_{DH}$	3.2	3.5		V	$I_{LOAD} = 10\mu A$
TO1, TO2, VIB	$V_{OH}$	3.2	3.4		V	$I_{LOAD} = 10\mu A$
<b>OUTPUT LEVELS LOW</b>						
All outputs	$V_{OL}$		0.05	0.3	V	$I_{LOAD} = -10\mu A$
<b>OUTPUT CURRENTS LOW</b>						
TO1	$I_{OL}$	10			mA	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	$I_{OL}$	2			mA	$V_{OUT} = V_{DD1}/2$
<b>OUTPUT CURRENTS HIGH</b>						
TO1, TO2, VIB	$I_{OH}$	2			mA	$V_{OUT} = V_{DD1}/2$
VA	$I_{OH}$	1			mA	$V_{OUT} = V_{DD1}/2$

**NOTES**

- These inputs have internal pullup or pulldown resistors.

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
<b>VOLTAGE DOUBLER</b>						
VDD2 (Doubled Voltage) no ext. load	$V_{VDD2}$		1.95		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	$V_{VDD2}$	1.80			V	
Max external load at VDD2 = 1.8 x VDD1	$I_{VDD1}$	1.20			mA	
<b>SUPPLY CURRENT</b>						
Decoder	$I_{VDD1}$			143	$\mu$ A	
Decoder 1.2mA ext. doubler load	$I_{VDD1}$			4.1	mA	
Decoder Max ext. doubler load	$I_{VDD1}$			5.4	mA	
<b>INPUT LOGIC HIGH</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IH}$	$V_{VDD2}-0.4$			V	
BLI, DIN	$V_{IH}$	$V_{VDD2}-0.5$			V	
NRESET	$V_{IH}$	$V_{VDD2}-0.3$			V	
X1	$V_{IH}$	1.0			V	
<b>INPUT LOGIC LOW</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IL}$			0.4	V	
BLI, DIN	$V_{IL}$			0.6	V	
NRESET	$V_{IL}$			0.5	V	
X1	$V_{IL}$			0.2	V	
<b>LOGIC HIGH INPUT CURRENT</b>						
ON, MEM, REPLAY	$I_{IH}$			1	$\mu$ A	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	$I_{IH}$			6	$\mu$ A	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	$I_{ILH}$			1	$\mu$ A	$V_{IH} = V_{VDD2}$
<b>LOGIC LOW INPUT CURRENT</b>						
All inputs except NRESET	$I_{ILL}$			-1	$\mu$ A	$V_{IL} = 0V$
NRESET	$I_{IL}$			-150	$\mu$ A	$V_{IL} = 0V$ , internal pullup
<b>OUTPUT LEVELS, HIGH</b>						
All outputs except TO1, TO2, VIB	$V_{OH}$	$V_{VDD2}-0.2$			V	$I_{LOAD} = 10\mu A$
TO1, TO2, VIB	$V_{OH}$	0.9			V	$I_{LOAD} = 10\mu A$
<b>OUTPUT LEVELS LOW</b>						
All outputs	$V_{OL}$			0.20	V	$I_{LOAD} = -10\mu A$
<b>OUTPUT CURRENTS LOW</b>						
TO1	$I_{OL}$	7.0			mA	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	$I_{OL}$	1.5			mA	$V_{OUT} = V_{DD1}/2$
<b>OUTPUT CURRENTS HIGH</b>						
TO1, TO2, VIB (current source)	$I_{OH}$	1.2			mA	$V_{OUT} = V_{DD1}/2$
VA (current source)	$I_{OH}$	1.0			mA	$V_{OUT} = V_{DD1}/2$
<b>VOLTAGE DOUBLER FREQUENCY</b>						
	$F_{VD}$	8	11	15	kHz	Note 3 VD Load = 0
	$F_{VD}$	44	68	108	kHz	Note 3 VD Load = 550 $\mu$ A
	$F_{VD}$	96	140	196	kHz	Note 3 VD Load = 1.2mA
	$F_{VD}$	130	166	214	kHz	Note 2, 3 VD Load = Max

**NOTES**

- These inputs have internal pullup or pulldown resistors.
- VD Load = Max is load current such that VDD2 = 1.8 x VDD1.
- Not production tested.

## ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
<b>VOLTAGE DOUBLER</b>						
VDD2 (Doubled Voltage) no ext. load	$V_{DD2}$		2.90		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	$V_{DD2}$	2.75			V	
Max external load at VDD2 = 1.8 x VDD1	$I_{VDD1}$	2.00			mA	
<b>SUPPLY CURRENT</b>						
Decoder	$I_{VDD1}$			240	$\mu$ A	
Decoder 1.2mA ext. doubler load	$I_{VDD1}$			3.8	mA	
Decoder Max ext. doubler load	$I_{VDD1}$			8.6	mA	
<b>INPUT LOGIC HIGH</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IH}$	$V_{VDD2}-0.6$			V	
BLI, DIN	$V_{IH}$	$V_{VDD2}-0.8$			V	
NRESET	$V_{IH}$	$V_{VDD2}-0.4$			V	
X1	$V_{IH}$	1.0			V	
<b>INPUT LOGIC LOW</b>						
RDATA, AIN, ON, REPLAY, MEM	$V_{IL}$			0.60	V	
BLI, DIN	$V_{IL}$			0.80	V	
NRESET	$V_{IL}$			1.50	V	
X1	$V_{IL}$			0.20	V	
<b>LOGIC HIGH INPUT CURRENT</b>						
ON, MEM, REPLAY	$I_{IH}$			1	$\mu$ A	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	$I_{IH}$			8	$\mu$ A	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	$I_{ILH}$			1	$\mu$ A	$V_{IH} = V_{VDD2}$
<b>LOGIC LOW INPUT CURRENT</b>						
All inputs except NRESET	$I_{ILL}$			-1	$\mu$ A	$V_{IL} = 0V$
NRESET	$I_{IL}$			-250	$\mu$ A	$V_{IL} = 0V$ , internal pullup
<b>OUTPUT LEVELS, HIGH</b>						
All outputs except TO1, TO2, VIB	$V_{OH}$	$V_{VDD2}-0.3$			V	$I_{LOAD} = 10\mu A$
TO1, TO2, VIB	$V_{OH}$	1.35			V	$I_{LOAD} = 10\mu A$
<b>OUTPUT LEVELS LOW</b>						
All outputs	$V_{OL}$			0.30	V	$I_{LOAD} = -10\mu A$
<b>OUTPUT CURRENTS LOW</b>						
TO1	$I_{OL}$	10.0			mA	$V_{OUT} = V_{DD1}/2$
TO2, VIB, VA	$I_{OL}$	2.0			mA	$V_{OUT} = V_{DD1}/2$
<b>OUTPUT CURRENTS HIGH</b>						
TO1, TO2, VIB (current source)	$I_{OH}$	2.0			mA	$V_{OUT} = V_{DD1}/2$
VA (current source)	$I_{OH}$	1.0			mA	$V_{OUT} = V_{DD1}/2$
<b>VOLTAGE DOUBLER FREQUENCY</b>						
	$F_{VD}$	8	11	17	kHz	Note 3 VD Load = 0
	$F_{VD}$	27	38	54	kHz	Note 3 VD Load = 550 $\mu$ A
	$F_{VD}$	56	77	116	kHz	Note 3 VD Load = 1.2mA
	$F_{VD}$	119	154	206	kHz	Note 2, 3 VD Load = Max

## NOTES

- These inputs have internal pullup or pulldown resistors.
- VD Load = Max is load current such that VDD2 = 1.8 x VDD1.
- Not production tested.

# MV6639

## AC ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

VDD1 = 1 to 3.5V, VDD2 <= VDD1 <= 3.5V, Tamb = -20 to +70°C.

Parameters	Symbol	Min	Typ	Max	Units	Comments
Crystal Frequency	$F_C$		32768		Hz	
Freq Reference Output	$F_O$		16384		Hz	
<b>SYSTEM INPUTS TO DECODER</b>						
Input Data Rate (Low Speed)	$F_D$		512		baud	Selectable See Fig 6
(High Speed)			1200			
Preamble Time (512 baud)	$t_{PA}$	1.125			s	
(1200 baud)		0.48			s	
Batch Time (512 baud)	$t_B$		1.0625		s	
(1200 baud)			0.4533		s	
<b>TONE GENERATOR</b>						
Output Frequency	$F_{TL}$		2048		Hz	Selectable See Fig 6
	$F_{TH}$		2731		Hz	
Vibrator Output Freq.	$F_V$		8		Hz	Fig 13
Vibrator Alert Period	$t_{VIRA}$		16		s	Fig 13
Visible Alert Period	$t_{VA}$		16		s	Fig 13
Visible Alert LED ON time	$t_{VAON}$		0.25		s	Fig 13
Visible Alert LED OFF time	$t_{VAOFF}$		1.75		s	Fig 13
TO1 Alert Period	$t_{TO1A}$		16		s	Fig 13
TO2 Alert Period	$t_{TO2A}$		10		s	
TO1, TO2 Alert Pulse Time	$t_{AP}$		125		ms	Fig 12
Decoder Status TO1, TO2 on	$t_{DSON}$		62.5		ms	Fig 11
Decoder Status TO1, TO2 off	$t_{DSOFF}$		62.5		ms	Fig 11
REPLAY pulse width	$t_{RPD}$	80			ms	
<b>Decoder RAM / E<sup>2</sup>PROM Timing</b>						
E <sup>2</sup> PROM Reset Pulse Rout	$t_{RHL}$		3		s	Fig 7, Note 1
E <sup>2</sup> PROM Reset Pulse Rout	$t_{RHS}$		61		μs	Fig 7, Note1
Clock High Level Time	$t_{CH}$		30.5		μs	Fig 7
Clock Low Level Time	$t_{CL}$		30.5		μs	Fig 7
E <sup>2</sup> PROM Access Time RDATA	$t_{ACC}$			20.5	μs	Fig 7
Data Setup Time RDATA	$t_{SU}$	10			μs	Fig 7
Data Strobe To Data Output Delay	$t_{DSDO}$			50	μs	Fig 5
Data Valid To Negative Strobe Edge	$t_{DV}$	783			μs	Fig 5
Power On RESET capacitor	$C_{RS}$		10		nF	
Voltage Doubler Output Ripple	$V_D$			1	mV p-p	Note 2

### NOTES

1. A 3 second reset pulse is generated when power is applied to the MV6639. This allows time for the voltage doubler output (if enabled) to stabilise. A shorter (61μs) reset pulse is generated for the automatic 4 minute reload.
2. VDD2 decoupling capacitor 100μF. Output current 10μA - 1.2mA.



**APPLICATION EXAMPLE: 1 VOLT PAGER SYSTEM**

A typical 1 Volt pager system, suitable as a wrist watch application is shown in figures 14 & 15. Only 3 chips are required. GPS's SL6609 Direct Conversion Receiver, MV6639 POCSAG Decoder and a 1 Volt E<sup>2</sup>PROM (e.g. EPSON SPM28C51).

Note that EPSON trades as SEKIO EPSON in Japan and S-MOS in America.

A 32KHz watch crystal is used as the reference frequency to the decoder. The SL6609 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The decoder voltage doubler output  $V_{VDD2}$  is available to power not only the receiver, but alternative higher voltage E<sup>2</sup>PROM and a microprocessor / LCD driver for a full tone and message pager.

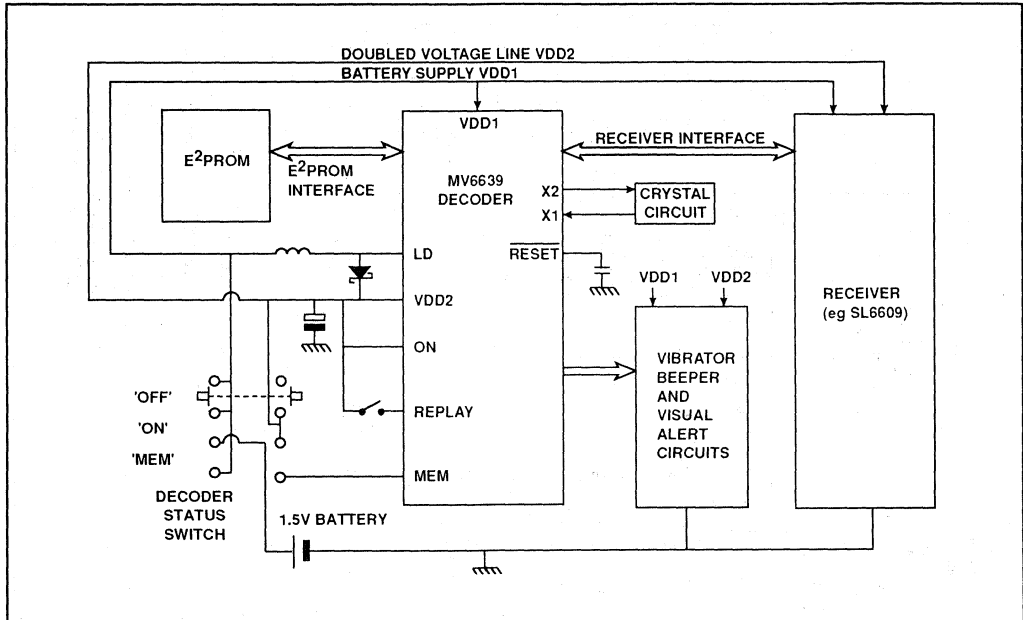
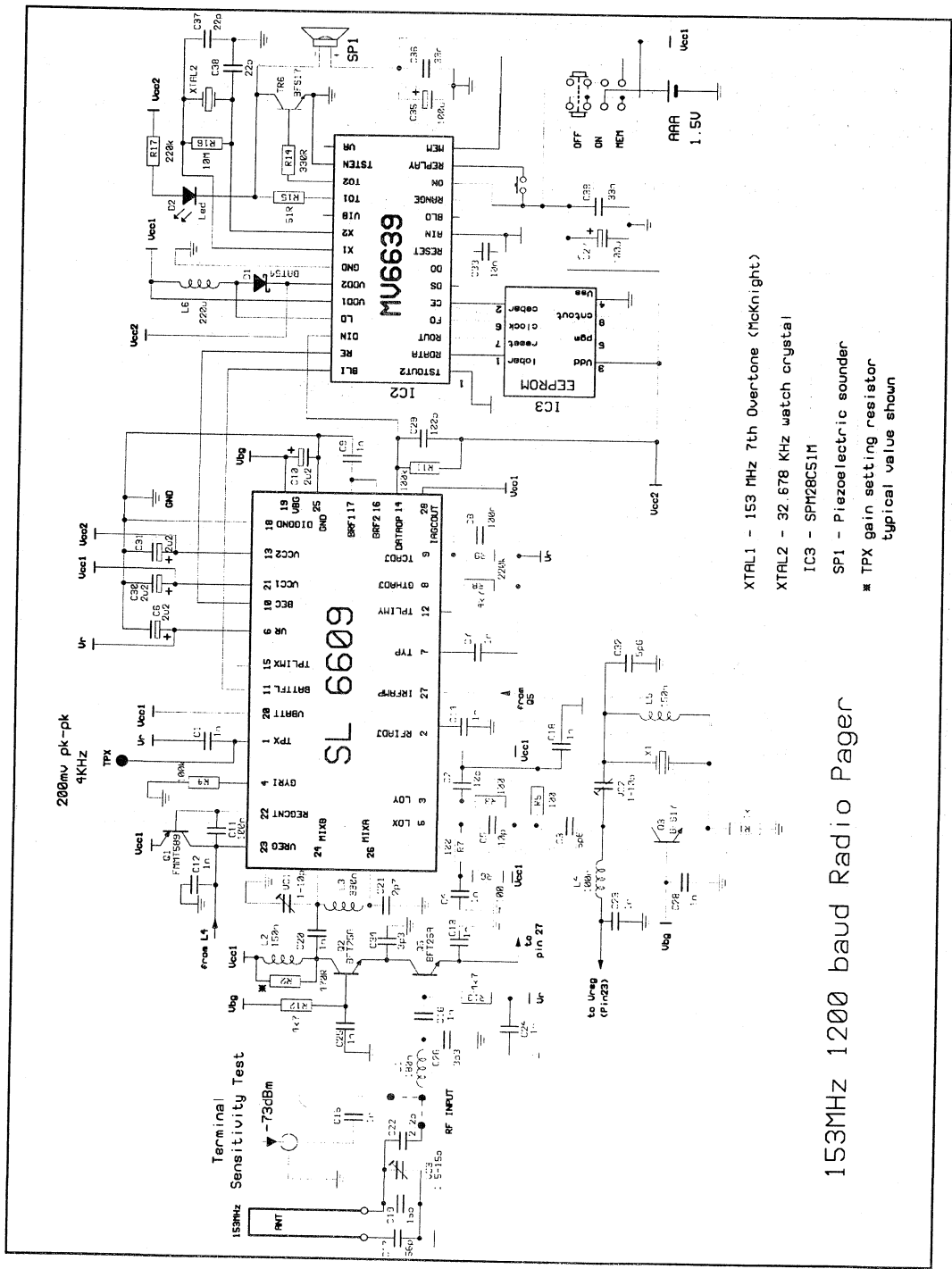


Fig. 14 Tone Pager applications example showing interface with SL6609 receiver



- XTAL1 - 153 MHz 7th Overtone (McKnight)
- XTAL2 - 32.678 KHz watch crystal
- IC3 - SPM28C51M
- SP1 - Piezoelectric sounder
- TPX gain setting resistor  
typical value shown

# 153MHz 1200 baud Radio Pager

Fig. 15

**MV6639 DEMONSTRATION CIRCUIT**

Fig.16 shows a simple demonstration circuit to allow the decoder to be evaluated.

The E<sup>2</sup>PROM is pre-programmed with the necessary addresses plus frame position and function bits which will be read into the MV6639 on power up.

The circuit will demonstrate the voltage doubler, tone outputs and tone cancel.

The required component values together with a suitable printed circuit layout (Fig.17) are shown below.

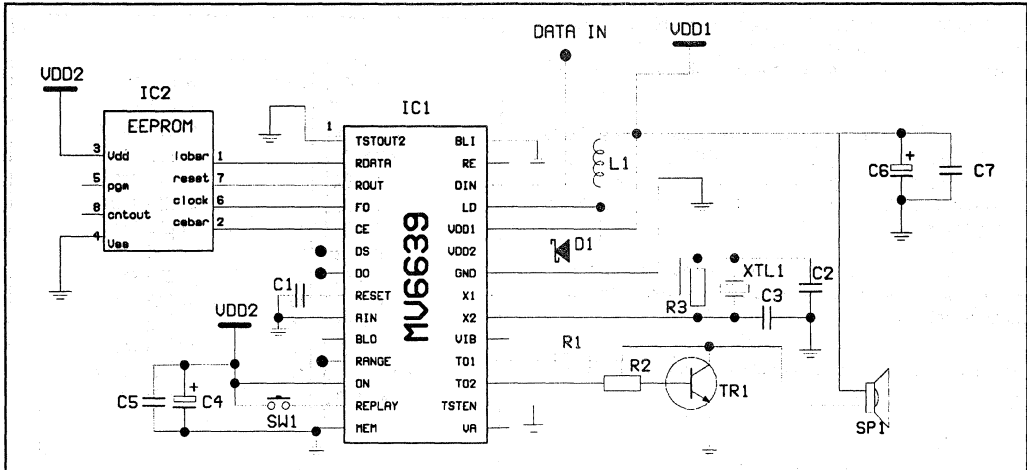


Fig.16 MV6639 Evaluation Circuit

**COMPONENT LIST**

R1	51R	L1	220uH
R2	360R	XTL1	32768Hz Watch Crystal
R3	10M	TR1	BFS17
C1	10nF	D1	ZC2811E schottky diode
C2	22pF	SP1	Miniature Sounder CB-09AP
C3	22pF	SW1	Push Button Switch
C4	100uF	IC1	MV6639
C6	100uF	IC2	SPM28C51M
C5, C7	33nF		

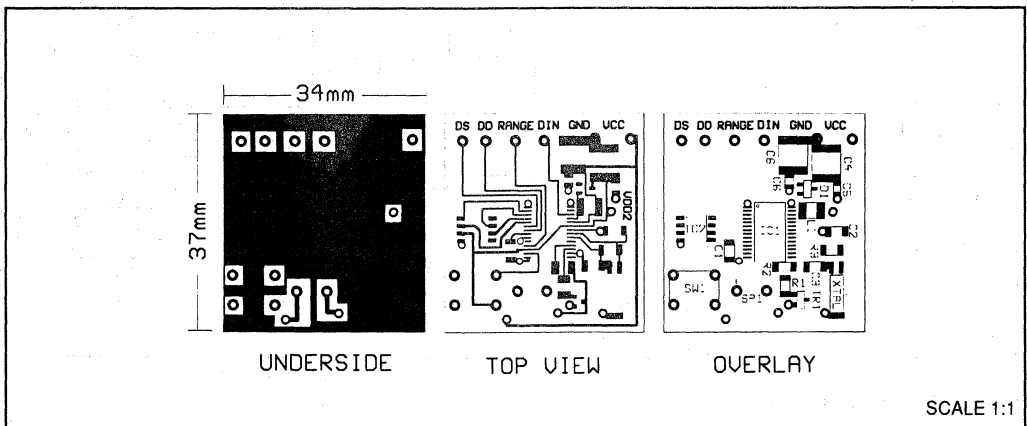


Fig.17 Printed Circuit Details

SCALE 1:1

# MV6640

## POCSAG DECODER

The MV6640 POCSAG decoder is capable of operating at 512 or 1200 baud. This device together with a suitable receiver, provides the major components for a POCSAG pager.

POCSAG is the acronym for Post Office Code Standardisation Advisory Group. The POCSAG code is the most accepted radio paging standard, (CGIR RPC No.1) and provides for over 2 million pager IDs, four of which may be held in this device.

The design is optimised for very low power, low voltage use. Advanced features allow the decoder to be used in a wide range of applications.

The pinout and architecture are shown in figures 1 and 2.

### FEATURES

- Low voltage supply (1V min, 3.5V max)
- Low current consumption (Typically 15µA)
- Voltage doubler for radio receiver or µP and Display
- True 2 bit CRC error correction with error status indication
- Tone only and/or messaging pager at 512 or 1200 baud using a single 32768Hz crystal
- Silent call storage
- Directly drives tone transducer
- Programmable tone generator output frequency (2048 or 2731 Hz)
- Interface to SL6609 radio receiver chip
- Low battery alert
- Interface to Standard 3 wire EEPROM
- True or Invented data

### APPLICATIONS

- Wrist watch pager
- Message display pager
- Tone only pager
- Data receivers

### ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD2 - GND)	-0.5V to 5V
Voltage on any pin	-0.3V to VDD2 + 0.3V
Operating temperature	-20°C to + 70°C
Storage temperature	-55°C to +125°C

### ORDERING INFORMATION

- MV6640/KG/NPDS - devices in anti-static sticks
- MV6640/KG/NPDE - devices in tape & reel

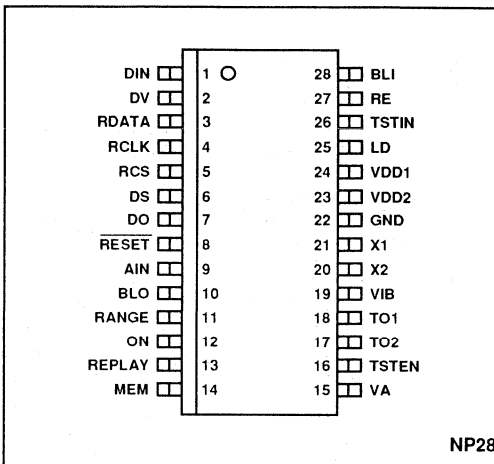


Fig. 1 Pin connection  
(top view - not to scale)

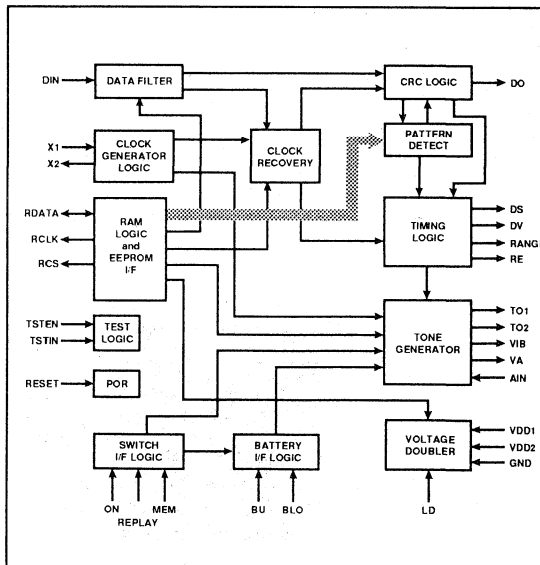


Fig. 2 MV6640 Block Diagram

# SL6609

## DIRECT CONVERSION FSK DATA RECEIVER

This device is an advanced direct conversion receiver for operation up to 470MHz. The device integrates all functions to translate a binary FSK modulated RF signal into a demodulated data stream. Adjacent channel rejection is provided using tuneable gyrator filters. To assist operation in the presence of large interfering signals both RF and audio AGC functions are provided.

The device also includes a 1 volt regulator capable of sourcing up to 5mA, a battery flag and the facility of incorporating a more complex post detection filter off-chip. Both battery flag and data outputs have open collector outputs to ease their interface with other devices.

### FEATURES

- Very low power operation - typ 3.0mW
- Single cell operation for most of the device.  
Limited functional blocks operating via an inverter
- Superior sensitivity of -130dBm
- Operation at wide range of paging data rates  
512, 1200, 2400 baud
- On chip 1 volt regulator
- Small package offering SSOP

### APPLICATIONS

- Credit card pagers
- Watch pagers
- Small form factor pagers i.e. PCMCIA
- Low data rate data receivers i.e. Security/remote control

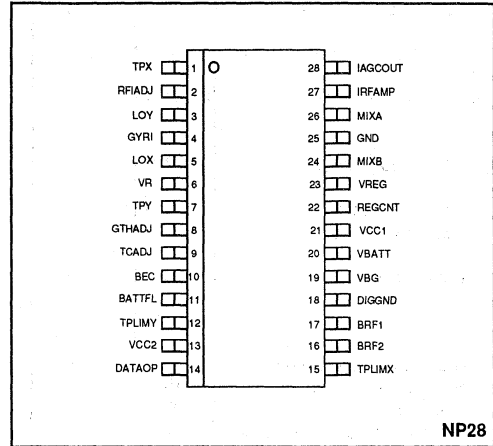


Fig.1 Pin connections

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature	-55°C to +150°C
Operating temperature	-20°C to +70°C

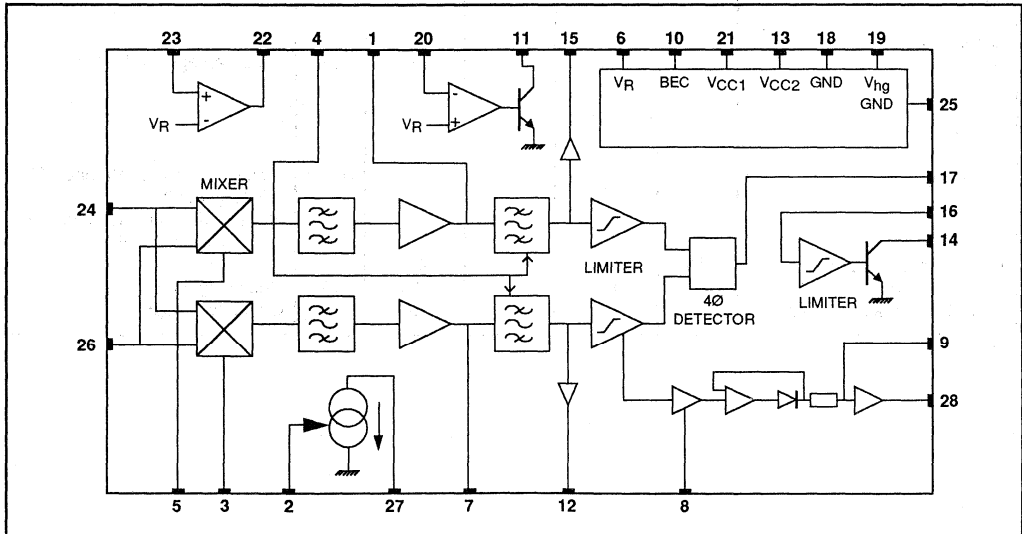


Fig.2 Block diagram of SL6609

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated:

Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
VCC1 - Supply voltage	21	0.95	1.3	2.8	V	VCC1 ≤ VCC2 - 0.7 volts
VCC2 - Supply voltage	13	1.8	2.7	3.5	V	
ICC1 - Supply current	21,27,28		1.5	1.8	mA	Includes 500µA IRF. Does not include regulator supply. Audio AGC inactive
ICC2 - Supply current	11,13,14		550	700	µA	Batt flag & Data O/P high
Power down ICC1	21,27,28			1	µA	Pin 27 voltage: 0.3 - 1.3V
Power down ICC2	11,13,14			8	µA	
1 volt regulator	23	0.95	1.0	1.05	V	I Load = 3mA. Ext PNP. β = 100, V <sub>CE</sub> = 0.1 volt
Band gap voltage reference	19	1.15	1.21	1.27	V	
Band gap current source	19			20	µA	
Voltage reference	6	0.93	1.0	1.07	V	
Voltage reference sink/source	6			10	µA	VCC1 > 1.1V
1 volt regulator load current		0.25	3	5	mA	
Turn on Time			5		mS	Stable data o/p when 3dB above sensitivity. C <sub>BG</sub> and C <sub>VR</sub> = 2.2µF
Turn off Time			1		mS	Fall to 10% of steady state current C <sub>BG</sub> and C <sub>VR</sub> = 2.2µF
Detector output current	17		+/-4		µA	
<b>RF current source</b>						
Current Source (RFAMP)	27	450	520	600	µA	Pin 27 voltage: 0.3 - 1.3V
<b>Decoder</b>						
Sensitivity		40			µVrms	Signal injected at TPX and TPY B.E.R. ≤ 1 in 30 5KHz deviation @ 500 bits/sec BRF capacitor = 2nF
Output mark space ratio	14	7:9		9:7		
Data O/P Sink Current	14	100		500	µA	Output logic low
Data O/P Leakage Current	14			1.0	µA	Output logic high

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated:

Tamb = 25°C, VCC1 = 1.3V, VCC2 = 2.7V

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
<b>Battery Economy</b>						
Input logic high	10	$(V_{CC2} - 0.3)$			V	Powered Up
Input logic low	10			0.3	V	Powered Down
Input current	10		0.05	1	$\mu$ A	Powered Up
Input current	10		6	8	$\mu$ A	Powered down transient initial
<b>Battery Flag Input</b>						
Input current	20			1	$\mu$ A	
<b>Battery Flag Output</b>						
Battfl Sink Current	11	100		500	$\mu$ A	(VBATT-VR) > 20mV
Battfl leakage current	11			1	$\mu$ A	(VBATT-VR) < -20mV
<b>Mixers</b>						
Gain to "IF Test"		34		41	dB	LO inputs driven in parallel with 50mVRMS @ 50MHZ. IF = 2KHz
RF input impedance	24, 26					See Figs.8a, 8b
LO input impedance	3, 5					See Fig.9
LO DC bias voltage	3, 5				V	Equal to Pin 21 (VCC1)
<b>Audio AGC</b>						
Max Audio AGC Sink Current	28	45	65	85	$\mu$ A	

**RECEIVER CHARACTERISTICS (GPS Demonstration board)**

Measurement conditions unless stated Vcc1 = 1.3V, Vcc2 = 2.7V, LNA = 18dB Gain, 2dB Noise figure,

Carrier frequency 153MHz, BER 1 in 30, Tamb = 25°C

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-127.5	-125	dBm	512 bps $\Delta f = 4.5$ kHz LO = -18dBm
		-128	-125.5	-123	dBm	1200 bps $\Delta f = 4$ kHz LO = -18dBm
Intermodulation		54	55		dB	512 bps $\Delta f = 4.5$ kHz LO = -18dBm
Adjacent channel		68	72.5		dB	512 bps $\Delta f = 4.5$ kHz LO = -18dBm Channel spacing 25kHz
Centre frequency acceptance		+/- 2.0	+/- 2.5		kHz	512 bps $\Delta f = 4.5$ kHz
			+/-2		kHz	1200 bps $\Delta f = 4$ kHz LO = -18dBm
Deviation acceptance			+/- 2.5		kHz	512 bps $\Delta f = 4.5$ kHz
			+/-2		kHz	1200 bps $\Delta f = 4$ kHz LO = -18dBm

**RECEIVER CHARACTERISTICS (GPS Demonstration board)**

Measurement conditions unless stated  $V_{CC1} = 1.3V$ ,  $V_{CC2} = 2.7V$ , LNA = 18dB Gain, 2dB Noise figure,  
Carrier frequency 282MHz, BER 1 in 30,  $T_{amb} = 25^{\circ}C$

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-130	-128.5	-125	dBm	512 bps $\Delta f = 4.5kHz$ LO = -15dBm
		-128	-126	-123	dBm	1200 bps $\Delta f = 4.0kHz$ LO = -15dBm
Intermodulation		54	55.5		dB	512 bps $\Delta f = 4.5kHz$ LO = -15dBm
Adjacent channel		68	72		dB	512 bps $\Delta f = 4.5kHz$ LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance		+/- 2.0	+/- 2.5		kHz	512 bps $\Delta f = 4.5kHz$
			+/-2		kHz	1200 bps $\Delta f = 4kHz$ LO = -15dBm
Deviation acceptance			+/- 2.5		kHz	512 bps $\Delta f = 4.5kHz$
			+/-2		kHz	1200 bps $\Delta f = 4kHz$ LO = -15dBm

**RECEIVER CHARACTERISTICS**

Measurement conditions unless stated  $V_{CC1} = 1.3V$ ,  $V_{CC2} = 2.7V$ , LNA = 18dB Gain, 2dB Noise figure,  
Carrier frequency 470MHz, BER 1 in 30,  $T_{amb} = 25^{\circ}C$

Characteristics	Pin	Value			Units	Comments
		Min	Typ	Max		
Sensitivity		-127	-125	-122	dBm	1200 bps $\Delta f = 4kHz$ LO = -15dBm
Intermodulation		50	53		dB	1200 bps $\Delta f = 4kHz$ LO = -15dBm
Adjacent channel		65	70		dB	1200 bps $\Delta f = 4kHz$ LO = -15dBm Channel spacing 25kHz
Centre frequency acceptance			+/- 2		kHz	1200 bps $\Delta f = 4kHz$ LO = -15dBm
Deviation acceptance			+/- 2		kHz	1200 bps $\Delta f = 4kHz$ LO = -15dBm



## OPERATION OF SL6609

The SL6609 is a Direct Conversion Receiver designed for use up to 470MHz. It is available in a 28 pin SSOP package and it integrates all the facilities required for the conversion of an RF FSK signal to a base-band data signal.

### Low Noise Amplifier

To achieve optimum performance it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This is easily biased using the on chip voltage and current sources provided.

All voltages and current sources used for bias of the RF amplifier, receiver and mixers should be RF decoupled using suitable capacitors (see fig.4 for a suitable Low-Noise-Amplifier).

### Local Oscillator

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at the  $-3dB/45^\circ$  transfer characteristic, giving a full  $90^\circ$  phase differential between the LO ports of the device. Each LO port of the device also requires an equal level of drive from the Oscillator. (see Fig.5).

### Gyrator Filters

The on chip filters include an adjustable gyrator filter. This may be adjusted with the use of an additional resistor between pin 4 and GND. This allows flexibility of filter characteristics and also allows for compensation for possible process variations.

### Audio AGC

The Audio AGC fundamentally consists of a current sink which is controlled by the audio (baseband data) signal. It has three parameters that may be controlled by the user. These are the Attack (turn on) time, Decay (duration) time and Threshold level (see Fig.6 and 7). See Application note for details.

### Regulator

The on chip regulator must be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:-

$$H_{FE} > = 100 \text{ for } V_{CE} > = 0.1V$$

Pin Number	Pin Name	Pin Description
1	TPX	X channel pre-gyrator filter test-point. This can be used for input and output
2	RFIADJ	RF current source adjustment pin
3	LOY	LO input channel Y
4	GYRI	Gyrator current adjust pin
5	LOX	LO input channel X
6	VR	VREF 1.0 V internal signal ground
7	TPY	Y channel pre-gyrator filter test point, input or output
8	GTHADJ	Audio AGC gain and threshold adjust. RSSI signal indicator
9	TCADJ	Audio AGC time constant adjust
10	BEC	Battery economy control
11	BATTFI	Battery flag output
12	TPLIMY	Y channel limiter (post gyrator filter) test point, output only
13	VCC2	Supply connection
14	DATAOP	Data output pin
15	TPLIMX	X channel limiter (post gyrator filter) test point, output only
16	BRF2	Bit rate filter 2, input to data output stage
17	BRF1	Bit rate filter 1, output from detector
18	DIG GND	Digital ground
19	VBG	Bandgap voltage output
20	VBATT	Battery flag input voltage
21	VCC1	Supply connection
22	REGCNT	1V regulator control external PNP drive
23	VREG	1V regulator output voltage
24	MIXB	Mixer input B
25	GND	Ground
26	MIXA	Mixer input A
27	IRFAMP	Current source for external LNA. Value of current output will decrease at high mixer input signal levels due to RF AGC
28	IAGCOUT	Audio AGC output current

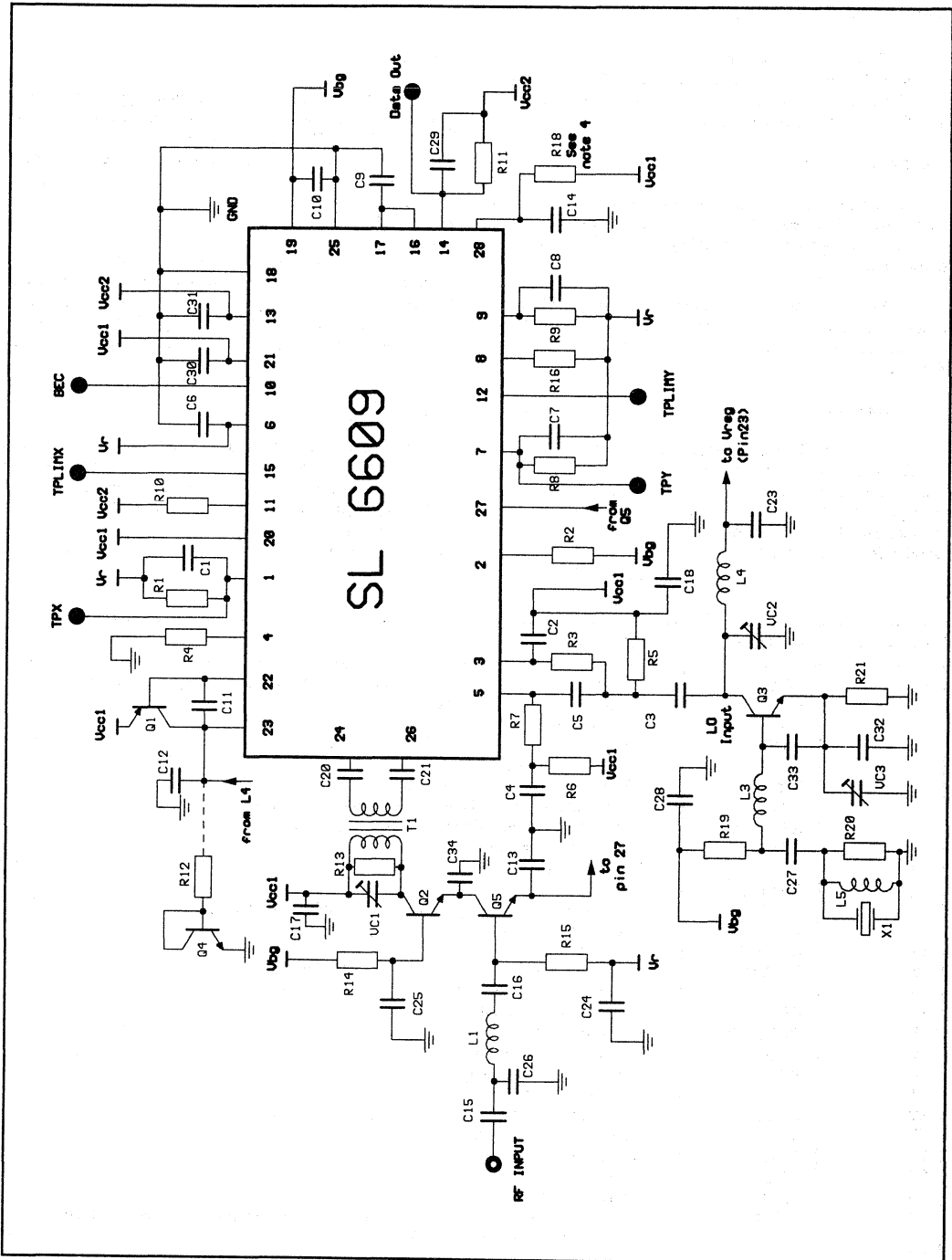


Fig.3 Application circuit board

**COMPONENTS LIST FOR APPLICATION BOARD** At 282MHz, 25kHz Channel Spacing.**Resistors**

R1	open circuit
R2	open circuit
R3	220
R4	100k
R5	1k
R6	1k
R7	220
R8	open circuit
R9	220k
R10	1M
R11	100k <sup>(6)</sup>
R12	not used
R13	2k7
R14	4k7
R15	4k7
R16	33k
R17	not used <sup>(3)</sup>
R18	0R <sup>(3)</sup>
R19	10k
R20	680
R21	1k
R22	open circuit

**Capacitors**

C1	1n
C2	2p7
C3	4p7
C4	1n
C5	2p7
C6	2u2
C7	1n
C8	100n
C9	1n <sup>(2)</sup>
C10	2u2
C11	100n
C12	1n
C13	1n
C14	1n
C15	1n
C16	1n
C17	1n
C17a	1n

**Notes**

- The values of R13 is determined by the set-up procedure. See Application Note.
- The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.
- R17 (See figure.6) forms a part of the audio AGC circuit and is determined by the voltage drop required to make the diode D1, conduct to give the RF attenuation required. R17 should be sufficiently large to ensure the voltage at pin 28 does not drop below 200mV. The maximum AGC current expected is 85µA. For the characteristics of the audio AGC current source see figure 7. If the audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (pin 6) and by connecting Pin 28

C18	1n
C19	not used
C20	1n
C21	1n
C22	not used
C23	1n
C24	1n
C25	1n
C26	5p6 <sup>(4)</sup>
C27	1n
C28	1n
C29	100p
C30	2u2
C31	2u2
C32	4p7
C33	4p7
C34	3p3
C35	not used
VC1	1-10p
VC2	1-10p
VC3	1-10p

**Inductors**

L1	100n <sup>(4)</sup>
L2	not used
L3	470n
L4	39n
L5	680n

**Active Components**

Q1	FMMT589
Q2	BFT25A
Q3	BFT25A
Q4	not used
Q5	BFT25A
D1	Panasonic MA862 <sup>(5)</sup>

**Misc**

T1	30nH 1:1 Coilcraft M1686-A
Xtal	5th Overtone 94.075MHz

- (IAGCOUT) to Vcc1., (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted. See figure.6 for AGC component values.
- L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.
- Suggested diode for use with the Audio AGC circuit (see figure.6) (D1 is not included on the general demonstration circuit).
- The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

## COMPONENTS LIST FOR APPLICATION BOARD

At 470MHz, 25kHz Channel Spacing.  
(LO circuit is 50Ω network as in Fig.5 - crystal oscillator not specified)

### Resistors

R1	open circuit	C14	1n
R2	open circuit	C15	1n
R3	100	C16	1n
R4	100k	C17	1n
R5	100	C18	1n
R6	100	C19	not used
R7	100	C20	1n
R8	open circuit	C21	1n
R9	220k	C22	not used
R10	1M	C23	not used
R11	100k <sup>(2)</sup>	C24	1n
R12	300 <sup>(3)</sup>	C25	1n
R13	open circuit <sup>(1)</sup>	C26	2.2pF <sup>(5)</sup>
R14	4k7	C27	not used
R15	4k7	C28	not used
R16	33k	C29	100p
R17	open circuit <sup>(4)</sup>	C30	2u2
R18	0R <sup>(4)</sup>	C31	2u2
R22	open circuit	C34	not used
		VC1	1-3pF

### Capacitors

C1	1n
C2	3.3pF
C3	1n
C4	1n
C5	3.9pF
C6	2u2
C7	1n
C8	100n
C9	1n <sup>(2)</sup>
C10	2u2
C11	100n
C12	1n
C13	1n

### Notes

- The values of R13 is determined by the set-up procedure. See Application Note.
- The value of "C9" is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.
- R12 & Q4 form a dummy load for the regulator. Permitted load currents for the regulator are 250μA to 5mA. The 1V regulator (output pin 23) can be switched off by connecting pin 23 directly to VCC2. Q1, Q4, R12 and C12 must then be omitted
- R17 forms a part of the audio AGC circuit (see figure 6) and is determined by the voltage drop required to make the PIN diode D1, conduct to give the RF attenuation required. R17 should be sufficiently large to ensure the voltage at pin 28 does not drop below 200mV. The maximum AGC current expected is 85μA. For the characteristics of the audio AGC current source see

### Inductors

L1	39nH <sup>(5)</sup>
L2	short circuit
T1	18nH 2 Turn 1:1 (Coilcraft) Q4123-A

### Active Components

Q1	Zetex FMMT589
Q2	Philips BFT25A
Q3	Not Used
Q4	Philips BFT25A <sup>(3)</sup>
Q5	Philips BFT25A
D1	Panasonic MA862 <sup>(6)</sup>

- figure 7. If the audio AGC is not required then the current source (Pin 28) may be disabled by connecting Pin 9 (TCADJ) to VR (pin 6) and by connecting Pin 28 (IAGCOUT) to Vcc1., (R18). The voltage at Pin 8 may still be used as an RSSI. R9, C8, C14, C19, R17 and D1 may then be omitted.
- L1 and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected. i.e. R17 and D1 omitted.
- Suggested diode for use with the Audio AGC circuit (D1 is not included on the general demonstration circuit).
- The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.

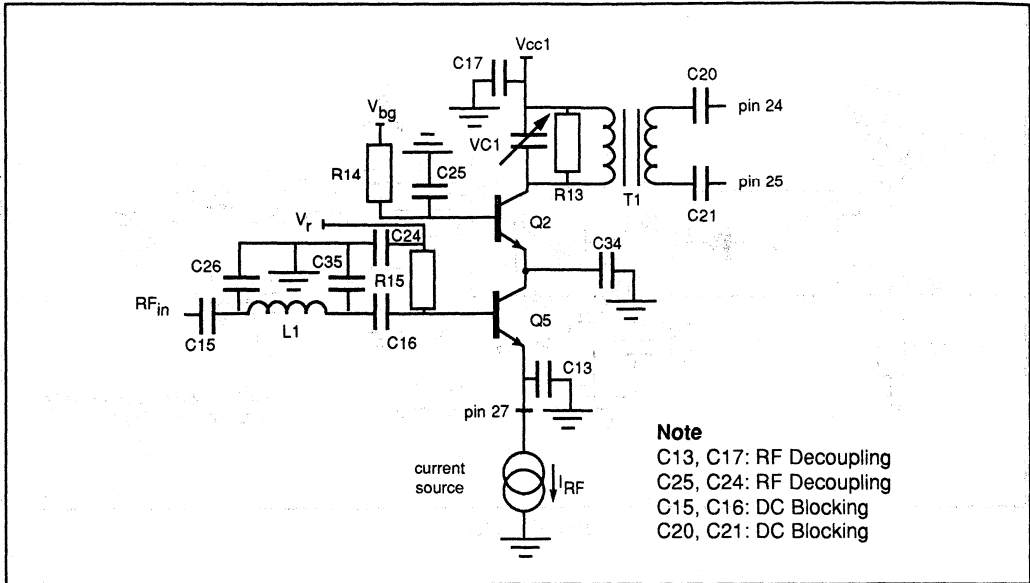


Fig.4 RF Amplifier

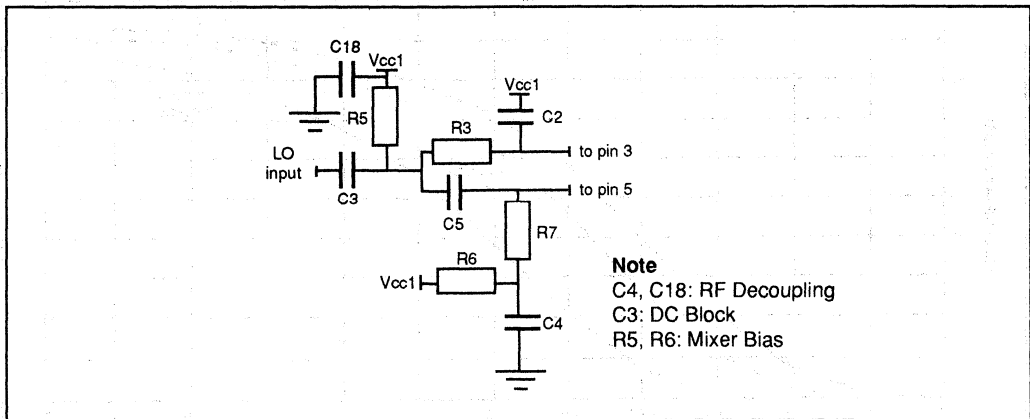


Fig.5 LO Network

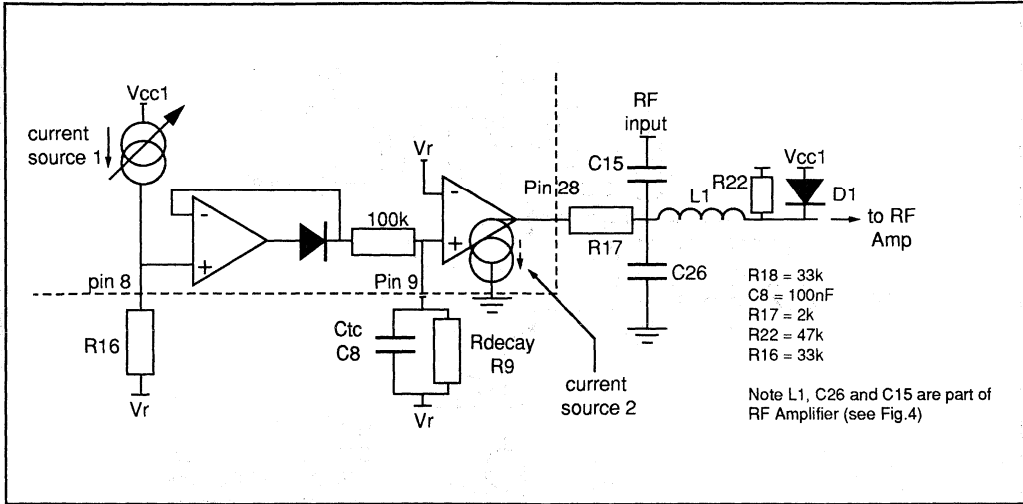


Fig.6 AGC Schematic

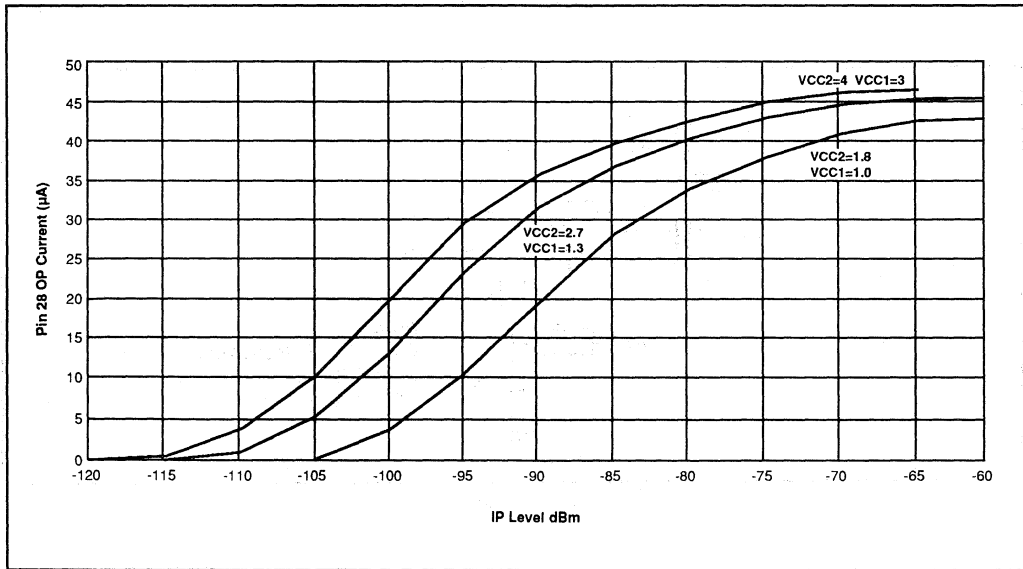


Fig.7 Audio AGC current vs. IP power at 25°C

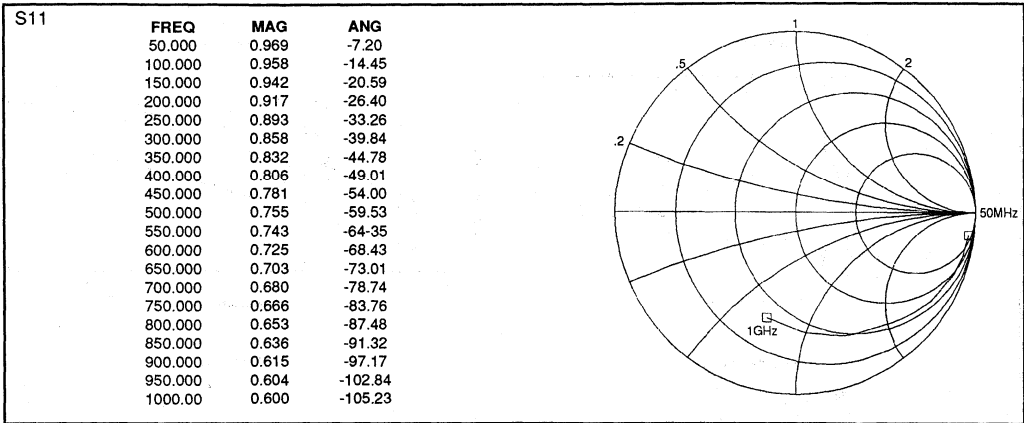


Fig.8a SL6609 Mixer A input S-Parameters

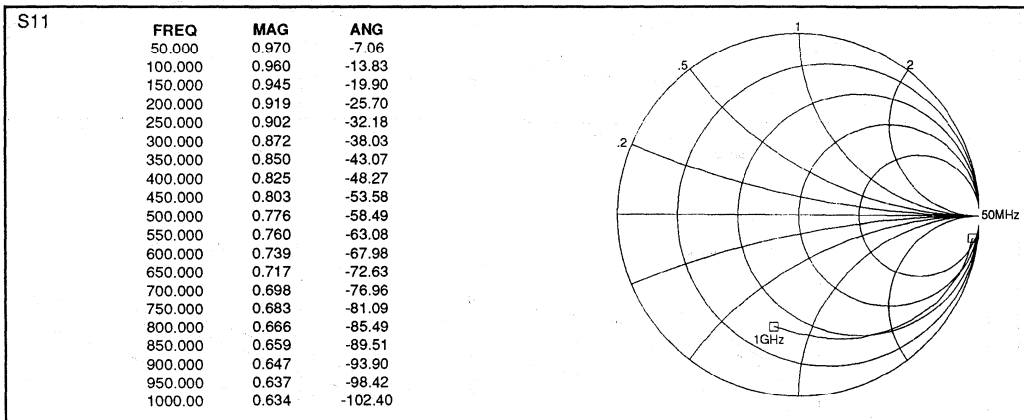


Fig.8b SL6609 Mixer B input S-Parameters

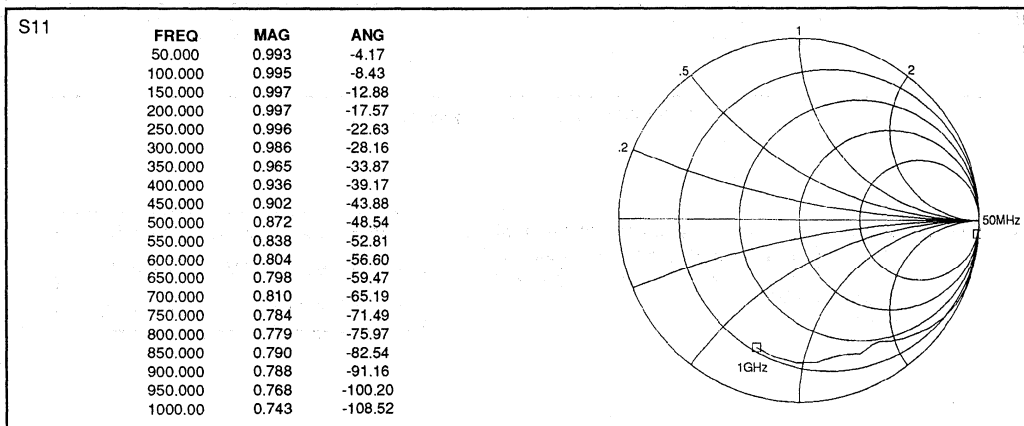


Fig.9 SL6609 LO X,Y inputs S-Parameters

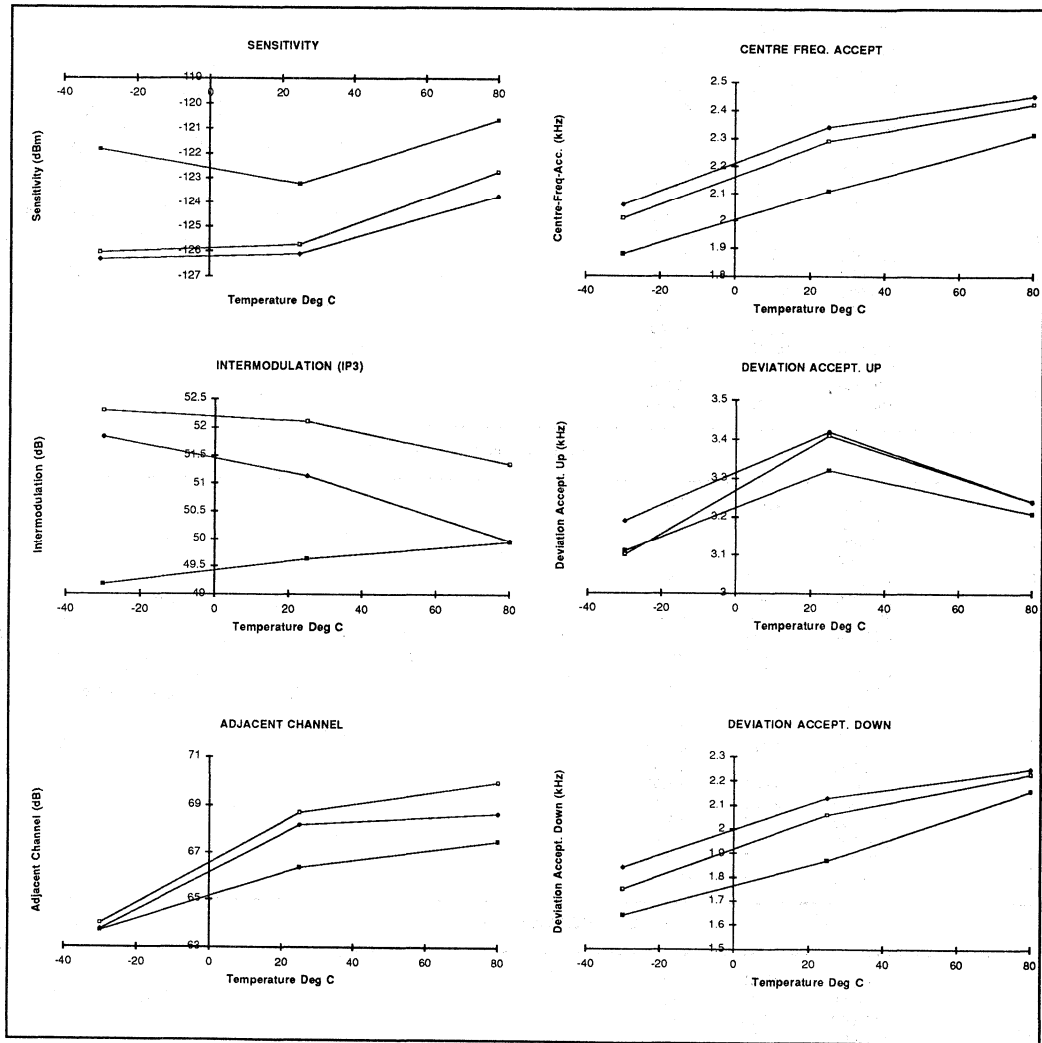
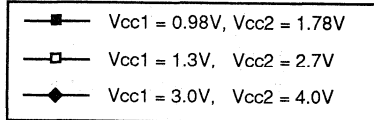


Fig.10 AC parameters vs. supply and temperature

Conditions:- 282MHz GPS demonstration board i.e. 18dB LNA, 2dB noise figure, carrier frequency 282MHz, 1200bps baud rate, 4kHz deviation frequency BER 1 in 30.





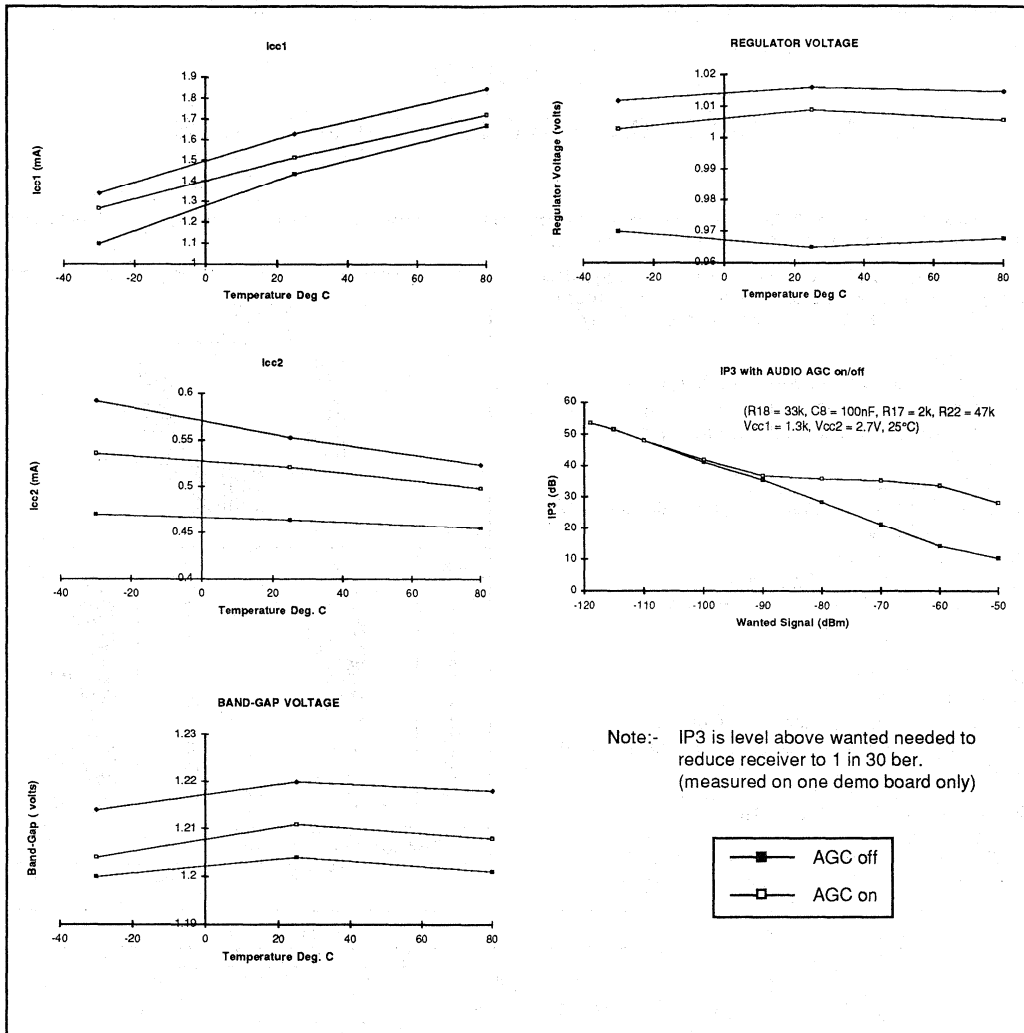


Fig.11 DC parameters vs. supply and temperature  
(IP3 vs audio AGC both on and off)

Conditions:- ICC1 includes 500µA LNA current but does not include the regulator supply (audio AGC inactive). ICC2 measured with BATT FLAG and DATA O/P HIGH, Fc = 282MHz.

■	Vcc1 = 0.98V, Vcc2 = 1.78V
□	Vcc1 = 1.3V, Vcc2 = 2.7V
◆	Vcc1 = 3.0V, Vcc2 = 4.0V

# SL6619

## UHF DIRECT CONVERSION FSK DATA RECEIVER

This is a **TARGET SPECIFICATION** of an active development program. No guarantee of production availability of this product can be given. Please contact your local sales office for further details.

The SL6619 is a Direct Conversion Receiver designed for use up to 450MHz. It integrates all the facilities required for the conversion of an RF FSK signal to a binary data stream.

### FEATURES

- Very low power operation – typ 3.1mW
- Single cell operation for most of the device, remaining functional blocks operating via an inverter
- Superior sensitivity
- Operation at wide range of paging data rates 512, 1200, 2400 baud
- On-chip 1Volt regulator
- 1mm thick small package offering
- Automatic frequency control function

### APPLICATIONS

- Credit card pagers
- Watch pagers
- Small form factor pagers i.e. PCMCIA
- Low data rate data receivers i.e. Security/remote control

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	5.5V
Storage temperature	-55°C to +150°C
Operating temperature	-20°C to +70°C

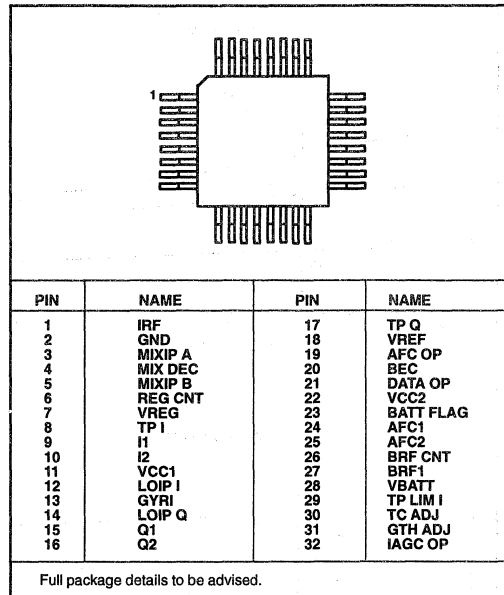


Fig. 1 Pin connections

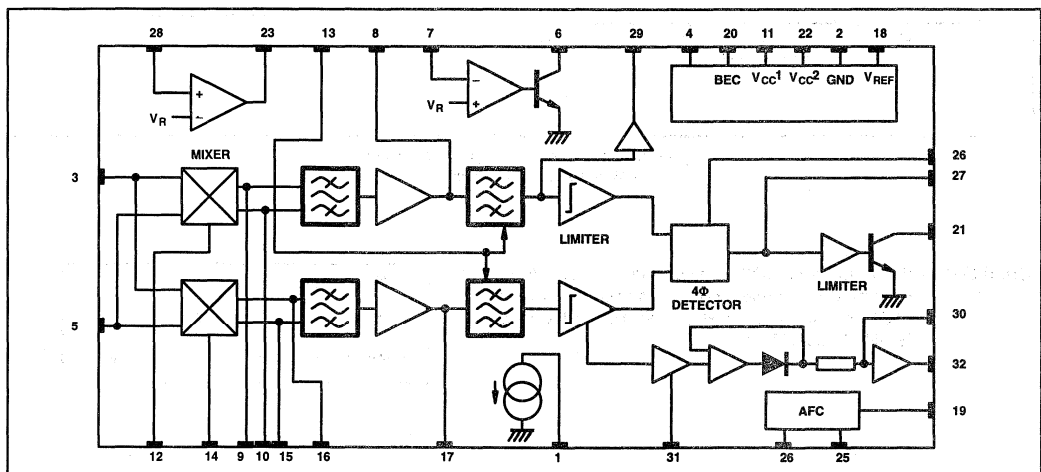


Fig. 2 Block diagram of SL6619

# SL6649-1

## 200MHz DIRECT CONVERSION FSK DATA RECEIVER

(Supersedes edition in May 1992 Personal Communications IC Handbook)

The SL6649-1 is a low power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capability of 'power down' for battery conservation.

The device also includes a low battery flag indicator.

### FEATURES

- Very Low Power Operation - typ. 3.7mW.
- Single Cell Operation with External Inverter
- Complete Radio Receiver in one Package.
- Operation up to 200MHz.
- 100nV Typical Sensitivity.
- Operates up to 1200 BPS.
- On Chip Tunable Active Filters.
- Minimum External Component Count
- Low Power Down Current Typical 5µA.

### APPLICATIONS

- Low Power Radio Data Receiver.
- Wristwatch Credit Card Pager.
- Radio Paging.
- Ultrasonic Direction Indication.
- Security Systems.
- Remote Control Systems

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Storage Temperature	-55°C to +150°C
Operating Temperature	-20°C to +70°C

### ORDERING INFORMATION

- SL6649-1/KG/LCAS - Ceramic chip (LC28) carrier in tubes
- SL6649-1/KG/MPES - Small outline (MP28) supplied in tubes
- SL6649-1/KG/MPEF - Small outline (MP28) supplied in tape & reel
- SL6649-1/KG/LCAG - Ceramic chip (LC28) carrier in tape & reel

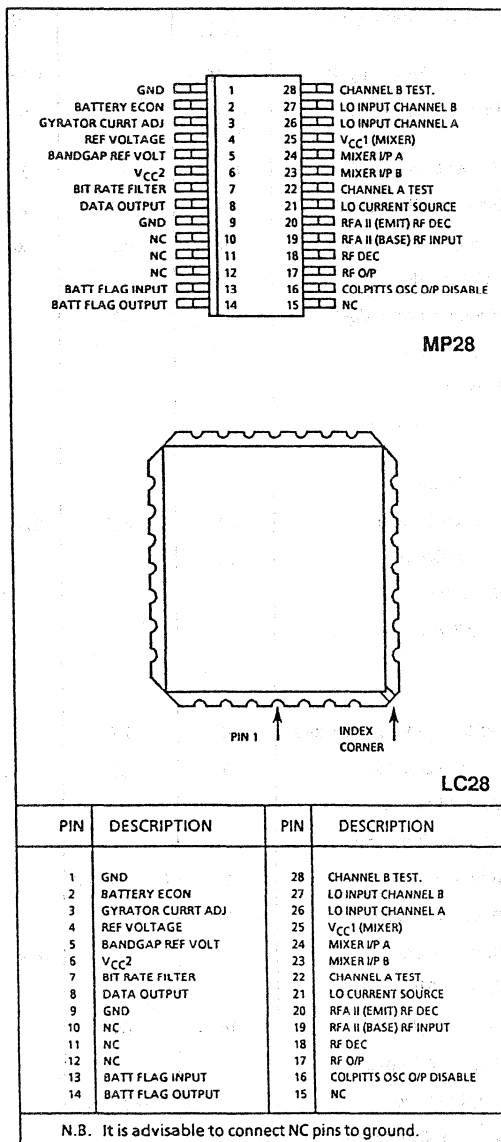


Fig.1 Pin connections - Top view

**ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed over the following conditions unless otherwise stated.

$$T_{amb} = 25^{\circ}\text{C}, V_{CC1} = 2.5\text{V}, V_{CC2} = 3.5\text{V}$$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage $V_{CC1}$	25	$V_R$	1.3	2.8	V	$V_{CC1} \leq (V_{CC2}) - 0.7$
Supply Voltage $V_{CC2}$	6,16	1.8	2.3	3.5	V	
Supply Current $I_{CC1}$	17, 25 26,27		1.6	2.0	mA	( $I_{RF}$ ) Included
Supply Current $I_{CC2}$	6,16		0.65	0.80	mA	
Power Down $I_{CC1}$	17,21,25, 26,27		5	12	$\mu\text{A}$	Batt Econ Low
Power Down $I_{CC2}$	6,16		3	12	$\mu\text{A}$	Batt Econ Low
Bandgap Reference	5	1.15	1.22	1.35	V	
Voltage Reference	4	0.93	1.0	1.13	V	
<b>RF Amplifier</b>						
Supply Current ( $I_{RF}$ )	17	460		640	$\mu\text{A}$	
Power Down	17				$\mu\text{A}$	Included in Power Down $I_{CC1}$
<b>Mixers</b>						
Gain to "IF Test"		32		38	dB	L.O. inputs driven in parallel with 50mV RMS @ 50MHz. IF = 2KHz
<b>Oscillator</b>						
Current Source	21	230	270	330	$\mu\text{A}$	
Power Down	21				$\mu\text{A}$	Included in Power Down $I_{CC1}$
<b>Decoder</b>						
Sensitivity				40	$\mu\text{Vrms}$	Signal injected at "IF TEST" B.E.R. $\leq 1$ in 30 5KHz deviation @ 500 bits/sec BRF capacitor = 1nF
Output Mark Space Ratio	8	7:9		9:7		
Output Logic High	8	85			$\%V_{CC2}$	
Output Logic Low				15	$\%V_{CC2}$	
<b>Battery Economy</b>						
Input Logic High	2	( $V_{CC2}$ ) -0.3			V	Powered Up
Input Logic Low	2			0.3	V	Powered Down
Input Current			0.05	1	$\mu\text{A}$	
<b>Battery Flag</b>						
Output High Level	14	85			$\%V_{CC2}$	Battery Low $R_L > 1\text{M}\Omega$
Output Low Level	14			15	$\%V_{CC2}$	Battery High $R_L > 1\text{M}\Omega$
Flag trig Level	13	$V_R - 25\text{mV}$		$V_R + 25\text{mV}$	V	Voltage Reference ( $V_R$ ) pin 4
<b>Colpitts Oscillator</b>						
Frequency		15		15	kHz kHz	R = 90K, pin 3 to GND R = 360K, pin 3 to GND

**TYPICAL ELECTRICAL CHARACTERISTICS**

These characteristics are guaranteed by design

 $T_{amb} = 25^{\circ}\text{C}$ ,  $V_{CC1} = 2.5\text{V}$ ,  $V_{CC2} = 3.5\text{V}$ 

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
<b>RF Amplifier</b>						
Noise Figure			5.5		dB	$R_S = 50\Omega$
Power Gain			14		dB	
Input Impedance	19					See Fig. 8
<b>Mixer</b>						
RF Input Impedance	23, 24					See Fig 9 (a) and (b)
LO Input Impedance	26, 27					See Fig 10
LO DC Bias Voltage	26, 27				V	Equal to pin 25.
<b>Detector</b>						
Output Current	7		$\pm 4$		$\mu\text{A}$	
<b>Colpitts Oscillator</b>						
Frequency	16		15		kHz	$R = 270\text{K}$ , Pin 3 to GND
Output Voltage	16		20		mVp-p	$R_L \gg 1\text{M}\Omega$ N.B. Refer to Channel Filter Fig. 4.

**RECEIVER CHARACTERISTICS (GPS Demonstration Board)**

**Measurement conditions (unless otherwise stated):** Applications circuit diagram Fig.6;  $V_{CC1} = 1.3\text{V}$ ;  $V_{CC2} = 2.3\text{V}$ ;  $T_{amb} = 25^{\circ}\text{C}$ ; ; Colpitts oscillator resistor = 270k $\Omega$ ; mixer input A and B phase balance = 180 $^{\circ}$ ; local oscillator input A and B phase balance = 90 $^{\circ}$ . Measurement methods as described by CEPT Res 2 specification.  $F_{IN} = 153\text{MHz}$  (512 baud)

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Terminal Sensitivity Tone only 4/5 call reception			-127	-124	dBm	$\Delta f = 4.5\text{kHz}$ , $R_S = 50\Omega$
Deviation Acceptance			$\pm 2.5$		kHz	3dB De-Sensitisation. $F_{IN} = F_{LO}$
Centre Frequency Acceptance		$\pm 2.0$	$\pm 2.5$		kHz	$\Delta f = 4.5\text{kHz}$
Adjacent Channel Rejection		65	70		dB	$\Delta f = 4.5\text{kHz}$ Channel Spacing 25KHz
Adjacent +1 Channel Rejection		65	70		dB	External capacitors on test
Third Order Intermod adj-1 + adj-2		52	53		dB	pins A and B.

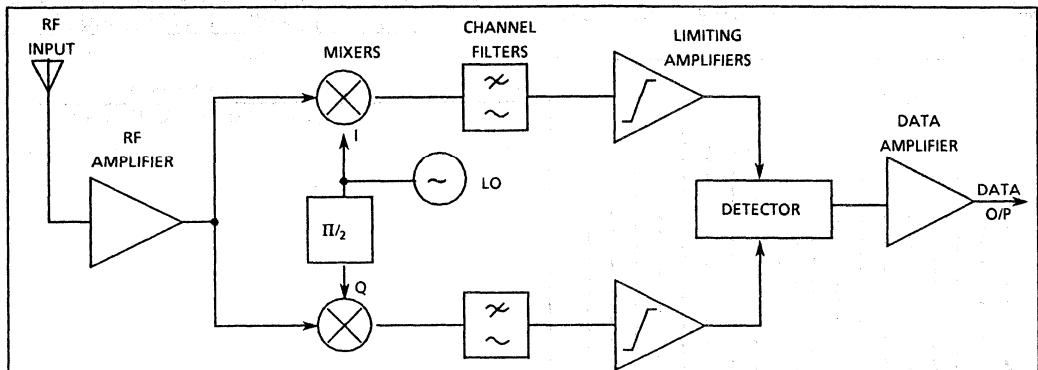


Fig.2 Block Diagram of SL6649-1 Direct Conversion Receiver

**PRINCIPLE OF OPERATION**

The incoming signal is split into two parts and frequency converted to baseband. The two paths are produced in phase quadrature (see Fig 2) and detected in a phase detector which provides a digital output. The quadrature network must be in the local oscillator path.

At a data rate of 512 baud and a deviation frequency of 4.5kHz, the input to the system has a demodulation index of 18. This gives a spectrum as in Fig 3.  $f_1$  and  $f_0$  represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig 3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate;  $f_c$  is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between  $f_0$  and  $f_c$  or  $f_1$  and  $f_c$ . If the LO is precisely at  $f_c$ , then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states. By applying the amplified outputs of the mixers to a phase discriminator, the digital data is reproduced.

**TUNING THE CHANNEL FILTERS**

The adjacent channel rejection performance of the SL6649-1 receiver is determined by the channel filters. To obtain optimum adjacent channel rejection, the channel filters' cut off frequency should be set to 8KHz. The process tolerances are such that the cut off frequency can not be accurately defined, hence the channel filters must be tuned. However the receiver characteristics on page 3 can be achieved with a fixed 270kΩ resistor between pin 3 and GND.

Tuning is performed by adjusting the current in the gyrator circuits. This changes the values of the gyrator's equivalent inductance. The cut off frequency is tuned to 8KHz. To accurately define the cut off of the channel filters, a gyrator based Colpitts oscillator circuit has been included on the SL6649-1. The Colpitts oscillator and channel filters use the same type of architecture, hence there is a direct correlation between oscillator frequency and cut off frequency. By knowing the Colpitts oscillator frequency the channel filter cut off frequency can be estimated from Figure 4.

Once the channel filters have been tuned it may be necessary to disable the Colpitts oscillator. The Colpitts oscillator is disabled by connecting the Colpitts oscillator output/disable pin (pin # 16) to  $V_{CC}$  2. This is needed since the Colpitts oscillator may impair the performance of the receiver.

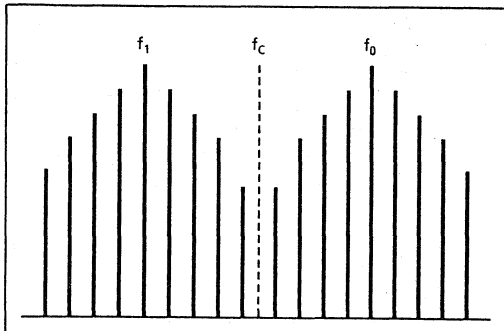


Fig. 3. Spectrum Diagram

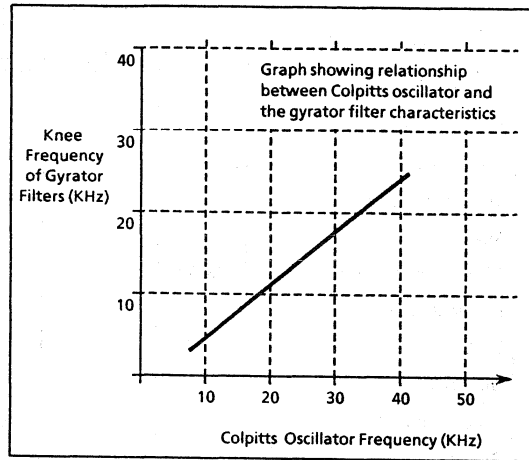


Fig. 4

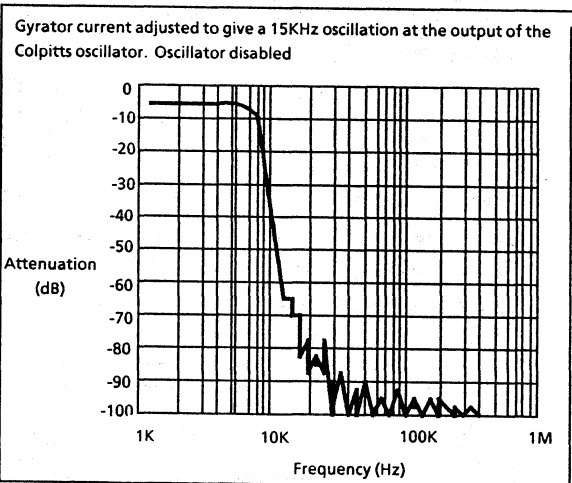


Fig. 5 Channel Filter Response

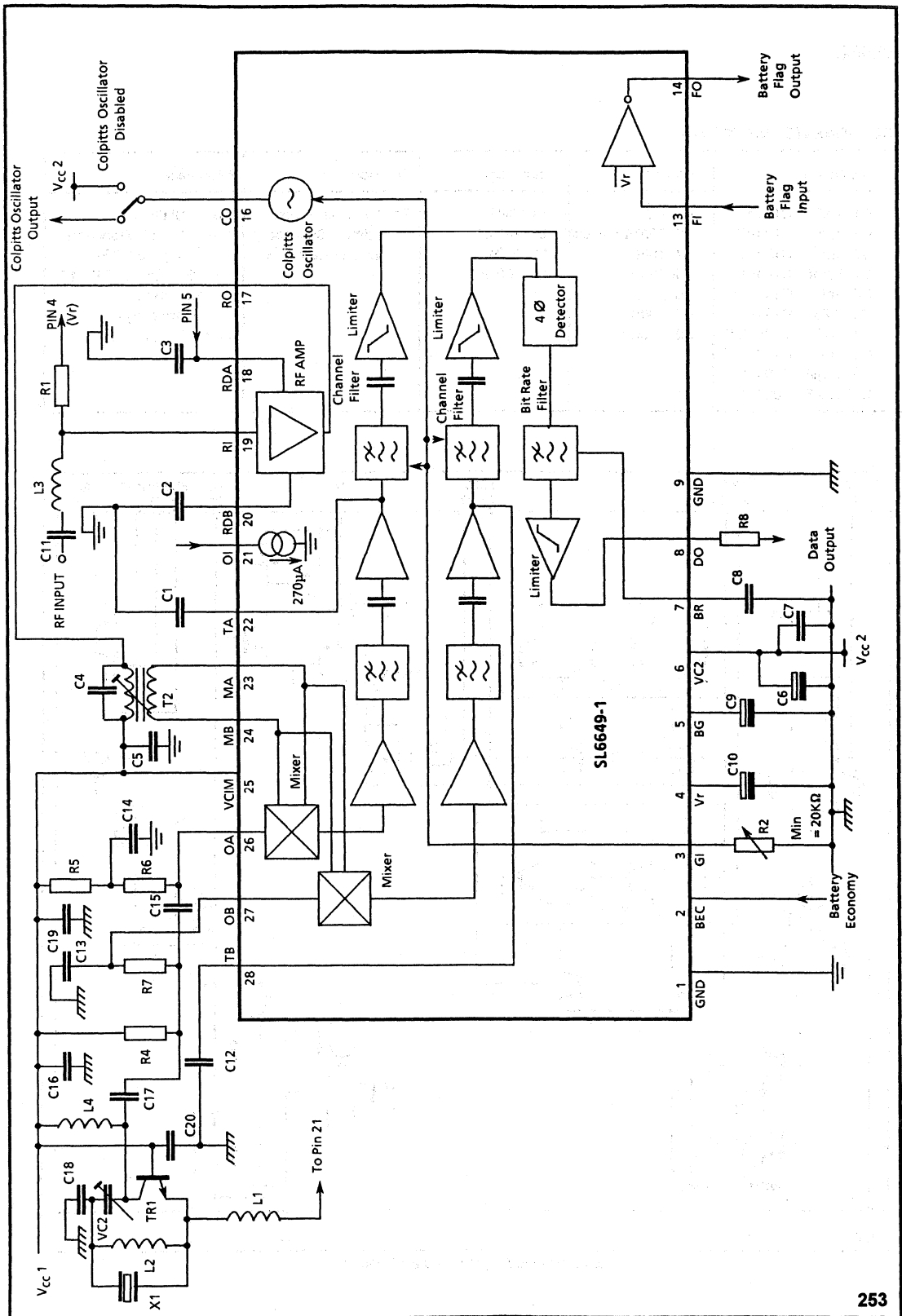


Fig. 6 Block Diagram and Applications Circuit (for component values see page 6)

COMPONENTS LIST FOR FIG.6

Capacitors	Resistors	Inductors	Transformers	Miscellaneous
C1 1nF C11 1nF	R1 2.2kΩ	L1 10μH	T1 1:1 Transformer Primary/Secondary Inductance = 200nH	IC1 SL6649-1 TR1 SOT-23 Transistor with $f_t \geq 1.3\text{GHz}$ (EG. ZETEX BFS 17) X1 153MHz 7th overtone crystal VC2 1.5-10pF
C2 1nF C12 1nF	R2 500kΩ Variable	L2 220nH		
C3 1nF C13 10pF	R4 100Ω	L3 150nH		
C4 5.6pF C14 1nF	R5 100Ω	L4 100nH		
C5 1nF C15 10pF	R6 100Ω			
C6 2.2μF C16 1nF	R7 100Ω			
C7 1nF C17 5.6pF	R8 100kΩ			
C8 1nF C18 4.7pF				
C9 2.2μF C19 1nF				
C10 2.2μF C20 1nF				

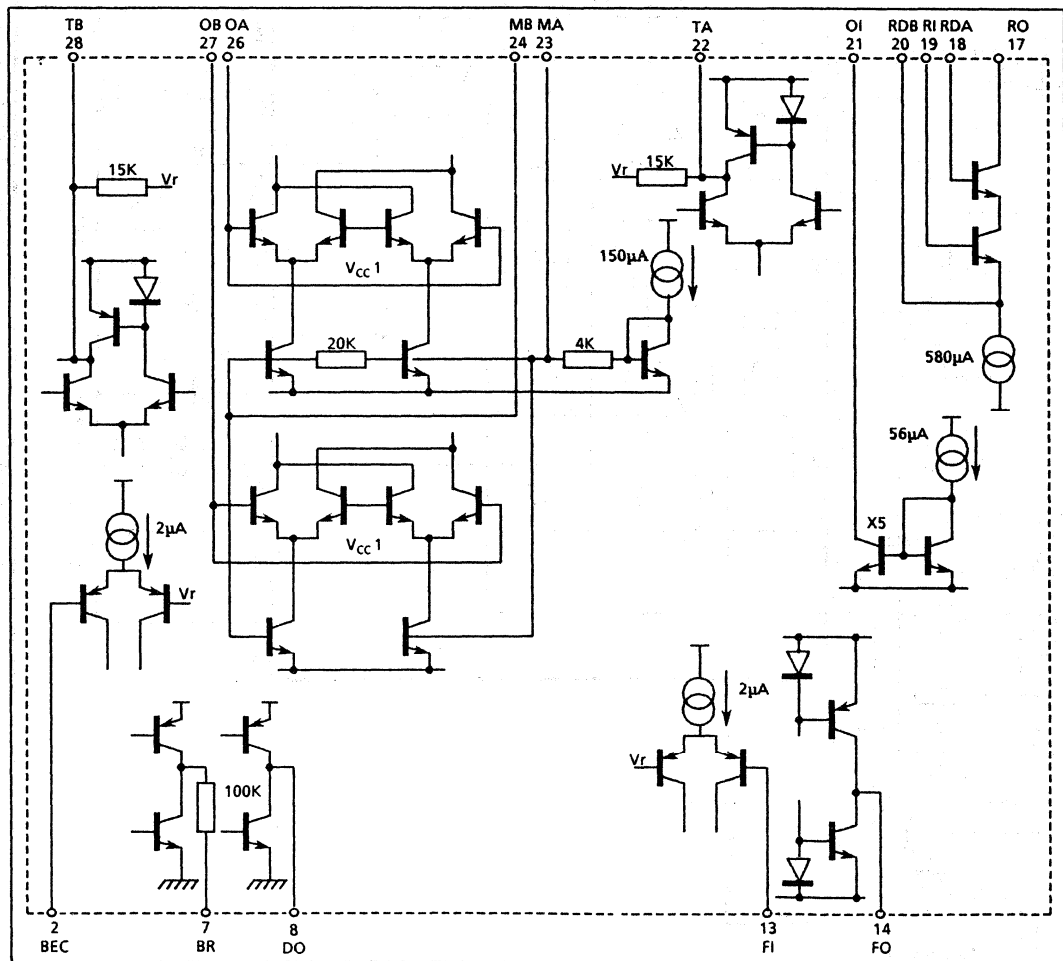


Fig. 7 Pinning Diagram of the SL6649-1



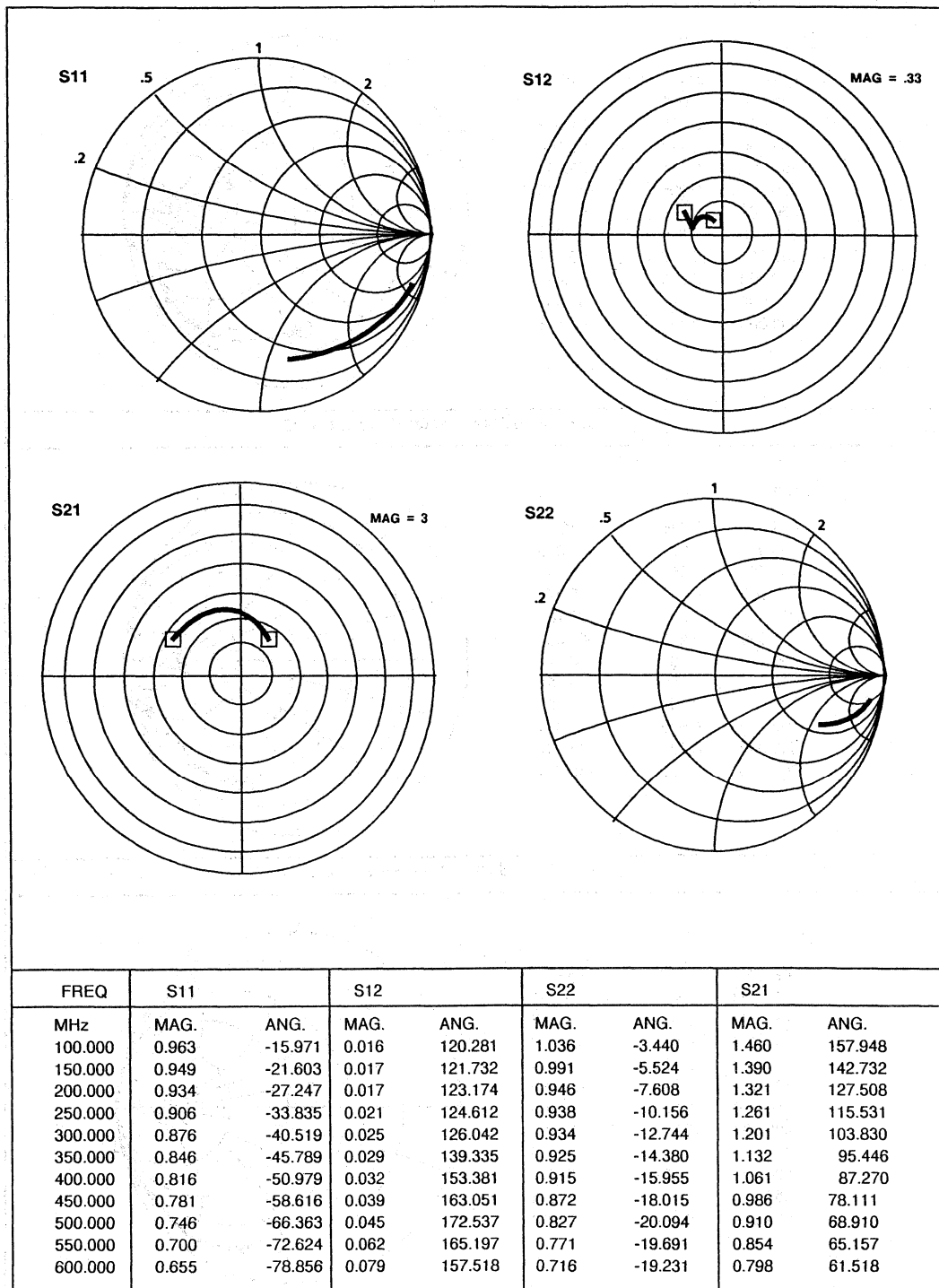


Fig. 8 RF Amplifier

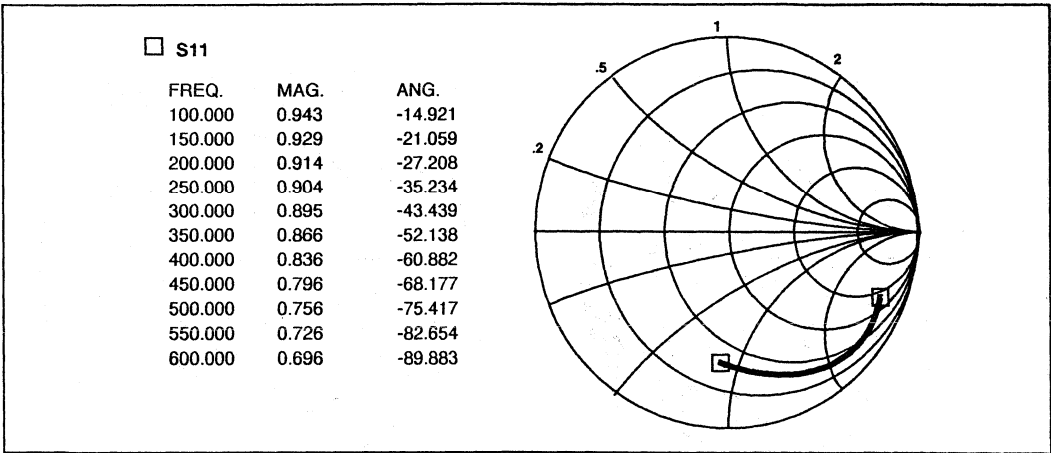


Fig. 9a SL6649-1 Mixer RF input pin. 23

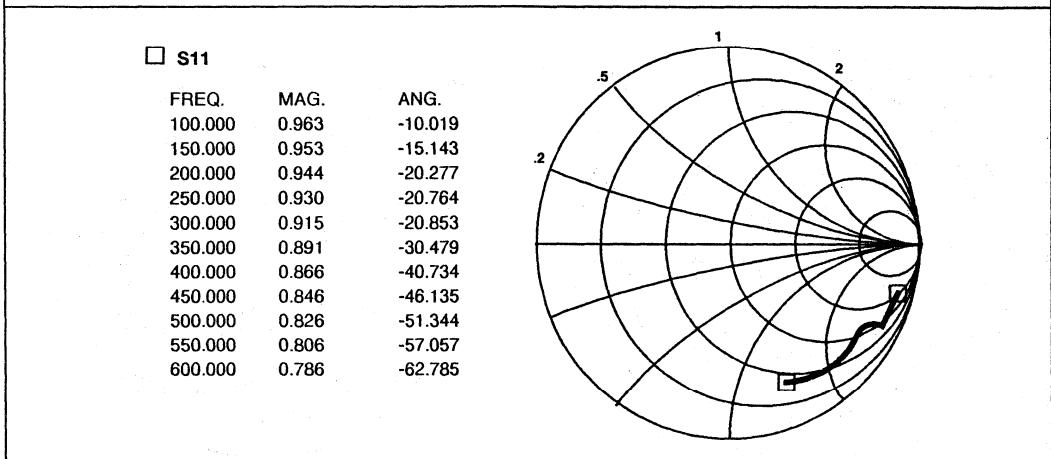


Fig. 9b SL6649-1 Mixer RF input pin. 24

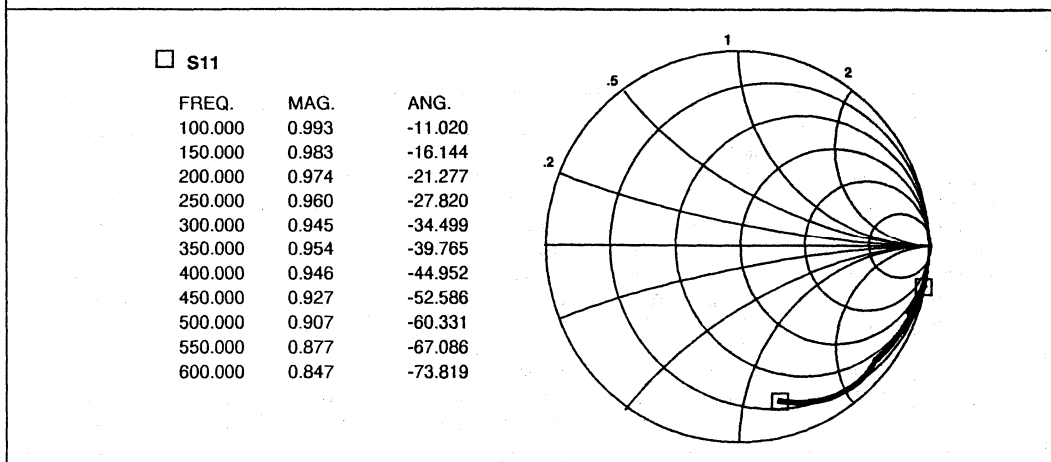


Fig. 10 SL6649-1 Mixer LO input pins 26 and 27.

## METHOD FOR THE MEASUREMENT OF SENSITIVITY ON THE SL6649-1 RECEIVER

The method used by GEC Plessey Semiconductors in the measurement of terminal sensitivity is essentially the same as that described in the Cept. Res2 Specification.

This method requires the following equipment:

1. A signal generator e.g. HP8640
2. A pocsag encoder
3. A pocsag decoder e.g. MV6639
4. An SL6649-1 Demo Board.
5. An interference free low impedance P.S.U. (Vcc1 and Vcc2 must be separate supplies and there must be at least 0.7V difference between them). Recommended supply configurations are shown in Fig. 13.

The test equipment and D.U.T. are set up as shown in Fig. 11.

The R.F. frequency is set to the nominal L.O. frequency of the receiver and the peak deviation is set to 4.5KHz. Care must be taken to avoid long power supply leads and any ground loops. Any interference from the decoder will be reduced by the insertion of a high value resistor R1 (100K $\Omega$ ) between the receiver data output and the decoder input.

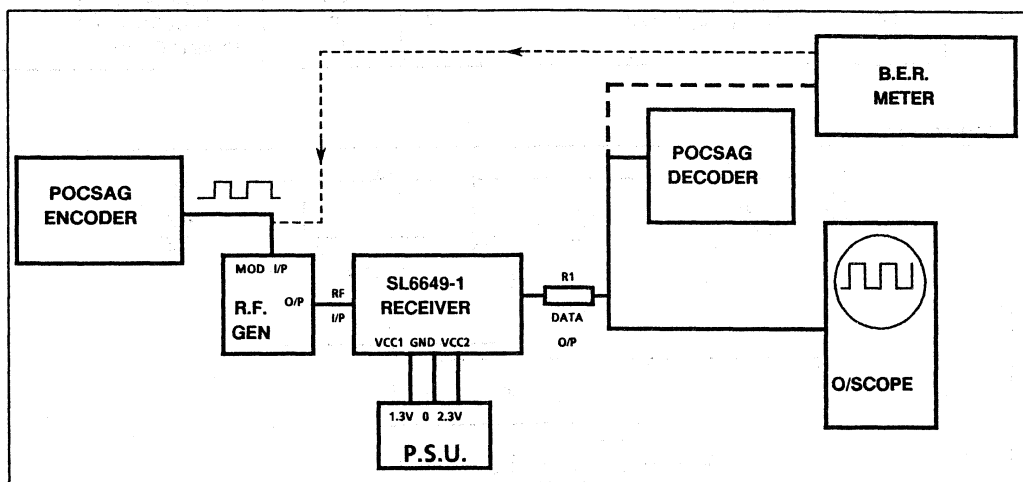


Fig. 11 Test System

The generator output level is reduced successively until the decoder responds just 4 out of 5 times to the encoder signal. This output level is then recorded as the sensitivity threshold of the receiver.

We find that this threshold correlates to a bit error rate of 1 in 30. The data output waveforms for an input level which produces a B.E.R. of 1 in 30 and for input levels 2dB above and below this level, are shown below (square wave input). It can be seen that the edge jitter increases dramatically at signal levels below the sensitivity threshold of -127dBm. Typical waveforms that can be seen on an oscilloscope around the sensitivity threshold level are shown in Fig. 12.

NB. In performing the sensitivity measurement great care should be taken in preventing coupling between test leads.

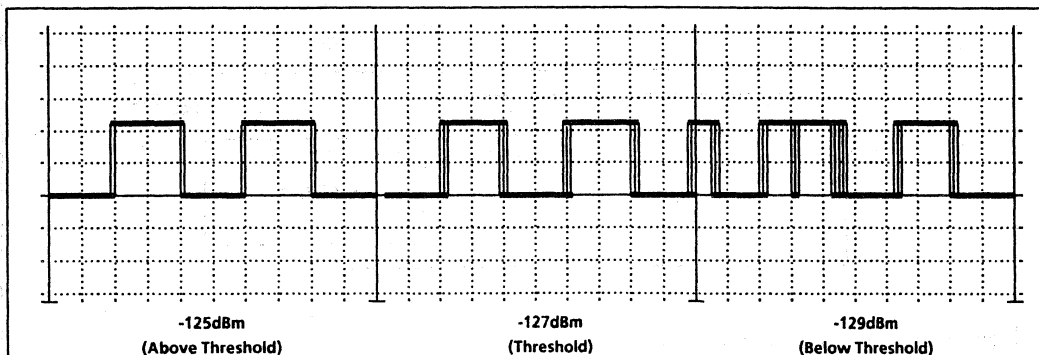


Fig. 12. Waveform at Data O/P

PIN	MNEMONIC	FUNCTION
1	GND	Ground
2	BEC	Battery Economy
3	GI	Gyrator Current Adjust
4	Vr	Reference Voltage
5	BG	Bandgap Reference Voltage
6	V <sub>cc2</sub>	V <sub>cc2</sub>
7	BR	Bit rate Filter
8	DO	Data Output
9	GND	Ground
10	UNC	UNC
11	UNC	UNC
12	UNC	UNC
13	FI	Battery Flag Input
14	FO	Battery Flag Output

PIN	MNEMONIC	FUNCTION
15	UNC	UNC
16	CO	Colpitts Oscillator Output/Disable
17	RO	RFA I (collector) RF Output
18	RDA	RFA I (base) RF Decouple
19	RI	RFA II (base) RF Input
20	RDB	RFAII (emitter) RF Decouple
21	OI	LO Current Source
22	TA	Channel A Test
23	MA	Mixer I/P B
24	MB	Mixer I/P A
25	VCIM	V <sub>cc1</sub> (mixer)
26	OA	LO Input Channel A
27	OB	LO Input Channel B
28	TB	Channel B Test

**Power Supplies**

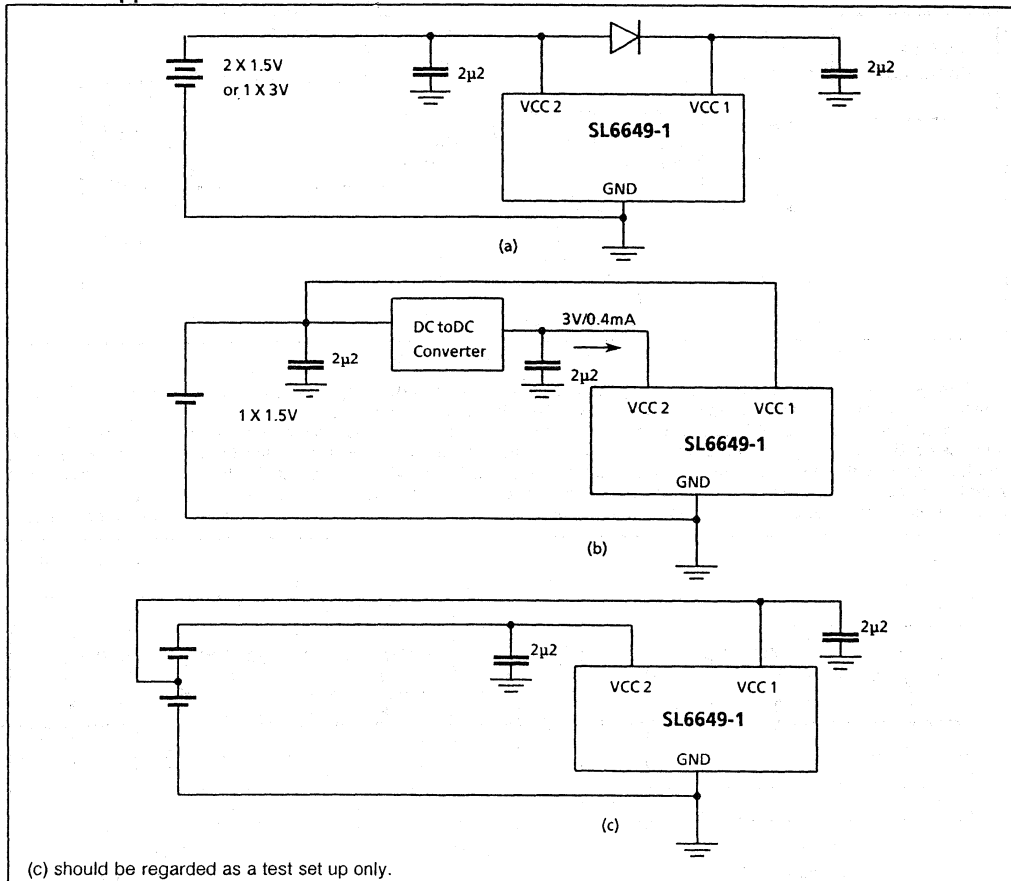


Fig. 13 (a) SL6649-1 Power Supply Options

### PAGER APPLICATION EXAMPLE

A typical 1 volt pager system suitable as a wrist watch application is shown in Fig. 13 (b). Only 3 integrated circuits are required to perform all the functions of a tone only pager. These are SL6649-1 direct conversion radio receiver and the MV6639 POCSAG decoder plus a 1 volt E2PROM (eg Seiko Epson SPM28C51).

The SL6649-1 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The MV6639 performs all the function required for a POCSAG decoder for tone only and/or pager messaging at 512 or 1200 baud. A 32KHz watch crystal is used as the reference frequency for the decoder.

The decoder voltage doubler output  $V_{CC2}$  is available to power not only the receiver, but an alternative higher voltage E2PROM and microprocessor/LCD driver for a full tone and message pager.

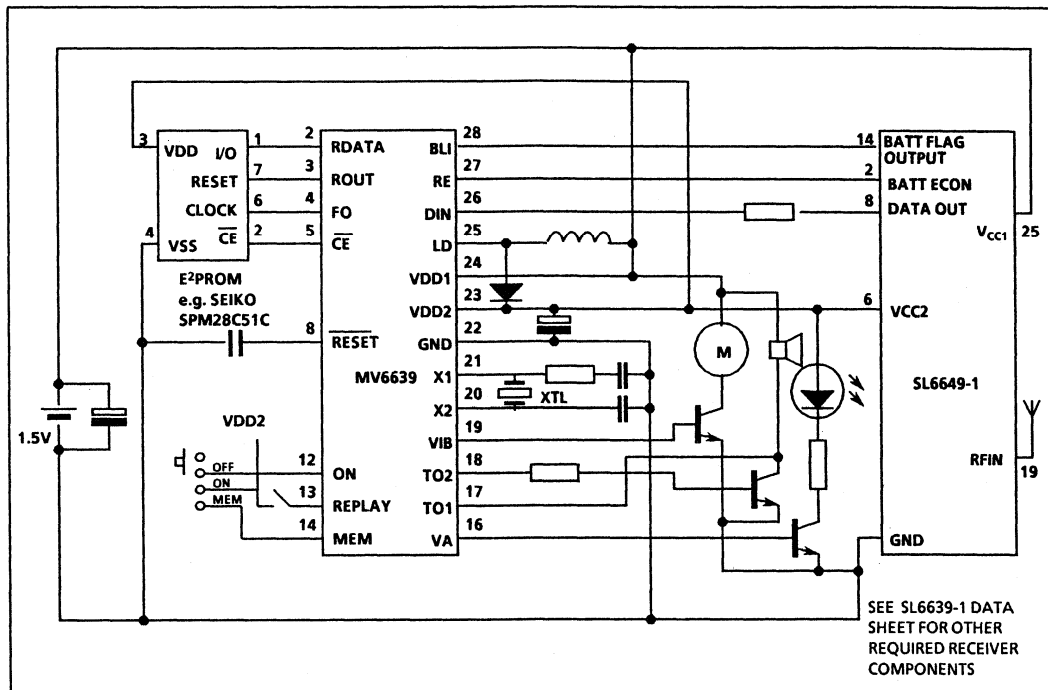


Fig. 13 (b) Tone Pager applications example showing interface with SL6649-1 receiver

### OPERATION AT OTHER FREQUENCIES AND DATA RATES

The values given in the components list on page 6 are appropriate for frequencies nominally around 153MHz. In order to use the receiver at other frequencies it is necessary to change the capacitor C4 which is resonant with the transformer T1, and L2 and L4 in the oscillator circuit.

It is also necessary to change the values of capacitors C13 and C15 such that the reactance of these is equal to 100Ω at the required frequency.

It is of course necessary to use a crystal of the required frequency and stability. In order to use the receiver at higher data rates it is only necessary to reduce the value of C8, for example, at 1200bps,  $C8 = 470\text{pf}$ .

A demonstration board has been designed specifically to demonstrate terminal sensitivity. It is possible to connect an antenna to the board with suitable matching but no guarantee can be given regarding field strength sensitivity. However, with a suitably designed combination of PCB and antenna, a sensitivity of  $5\mu\text{V/M}$  should be attainable.

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# Section 8

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## THE NJ88C24 PHASE DETECTORS

This application note deals with the theoretical and practical behaviour of Sample and Hold type Phase Locked Loop Synthesiser ICs. The implementation uses an NJ88C24 device and concentrates on the analysis of its phase detectors, the functionality of the digital phase detector and its analog post processing unit (which uses a ramp generator to increase the gain of the digital phase detector) and a sample and hold delay filter. Having characterised the phase detectors, consideration is given to modelling a complete loop using the NJ88C24 and comparing those predictions with the practical result. Some previously unpublished information is presented, which should make this note of interest to both new and old users of this type of PLL Synthesiser.

### INTRODUCTION

The initial goal is to derive a model of the NJ88C24's phase detectors which can be used to solve the external component values around the loop filter for a particular set of loop parameters: the loop natural frequency ( $\omega_0$ ), the loop damping factor ( $\zeta$ ) and the division ratio between the VCO output and the phase comparator input (N). The component values are calculated using general network analysis techniques. Note that the transfer function of the phase detector gain has not been generally available from previous application notes; the following discussion is intended to redress this omission. The form of the loop will

be examined in its most basic form, from which the need to analyse both the digital and analog phase detectors will emerge. The complete schematic of the input buffers, the dividers, the phase comparator, the digital phase detector output, the analog phase detector output and its control logic will be discussed first. A description of their function follows, with a detailed examination of both detectors' functions, testing and measured results. An analysis of the phase detectors' gains is carried out and the equations for the loop components are written. A comparison is made between the result of the expression which mathematically models the behaviour of a loop and its practical implementation in an evaluation card.

# AN-94

## USING THE NJ88C33 PLL SYNTHESISER

### Abstract:

A tutorial intended to assist with the understanding of the basic parameters of a single-loop, phase-feedback frequency locked oscillator. Since the uses of phase-locked loops are many and varied, only a sample of their uses and design equations have been given here. Some mathematical ability is necessary to deal with the ideas expressed. To assist, all working has been shown for the derivation of the formulae. The aim of this note is to encourage manipulation of the variables and build confidence with phase-locked loop parameters in general. It is recommended that all formulae derivations are followed through with pencil and paper to gain a full understanding of their function. The NJ88C33 has been used as the particular example.

### Introduction

The NJ88C33 is a single chip solution for VHF PLL Synthesis, capable of lower levels of phase-noise than earlier PLL ICs since it uses current source outputs from the phase detector to charge pump a passive loop filter, rather than the active types favoured previously. The simplest type of practical loop using this phase detector is of "the third order, type two". An analysis of these loops is not generally available from control theory books, prompting the generation of this Tutorial Note.

In Part A we introduce the NJ88C33. The implementation of a third order charge pumped phase-locked loop is examined in Part B where the loop equations are developed using standard control theory to predict the time and frequency responses for the basic loop. Part C is devoted to bench measurements of the parameters involved to prove the equations of Part B and explains the use of the evaluation card and a simple programming board to gain an insight into how the device works with its programming sequences. This section also covers a discussion of commonly encountered problems when designing circuits using synthesiser ICs, along with an examination of the sensitive areas of the NJ88C33. Last, but not least, is a series of Appendices which deal with the derivation of the basic concepts behind the formulae used in the loop analysis.

Please contact your local GPS Customer Service Centre for copies of both these Application Notes.



# AN151

## MV3100 CODEC EVALUATION PACKAGE

### SUMMARY

This Application Note describes the evaluation package for the MV3100, 3 Volt Codec for Digital Mobile Telephones. The package contains hardware and supporting software for use with IBM PCs or compatibles.

The Hardware of the evaluation package consists of a printed circuit board containing two MV3100 codecs with full access to the analog and PCM ports. The control data ports are buffered to allow control from a PC working at TTL voltage levels. The board also contains circuitry to supply the necessary clock signals to the codecs so that the board can be used without additional hardware. The software of the evaluation package allows the control of the programmable features of each codec independently.

The evaluation package allows users to try out the range of options offered by the codecs but it is not suitable for the verification of all specified parameters.

### HARDWARE DESCRIPTION

The hardware of the evaluation package consists of a PCB and a cable with which to attach it to the parallel port of a PC. The PCB contains two codecs each with an interface to the PC controller. This allows a full duplex link to be made or two parallel circuits, with differing set-ups, to be compared.

The two codec circuits are completely separated apart from the common power supply. The applied voltage (VCC on the circuit diagram) should be 2.7V to 3.6V with respect to AGND.

The board also contains a clock generating circuit that can generate the clocks required for back to back operation. The clocks operate from a separate power supply to the codecs and VDD should be 5V  $\pm 10\%$  with respect to DGND.

N.B. AGND and DGND should be connected at a single point, at the board power connector if not connected elsewhere in the system. VDD should be connected even if the clocks are not required.

The cable consists of a ribbon cable with a 25 way D type plug on one end and a 24 pin DIL header on the other. The D type should be connected to the parallel (printer) connector of a PC, the DIL should be connected to SK9 on the PCB so that wire 1 (brown) is at the end of the socket with pin 1.

### Codecs

Each codec has four separate interfaces:-

The PM connector has all the signals for the PCM interface and timing. FIN is the master 32kHz clock from which the codec PLL derives the internal clocks. The BCLK signal is used to clock data in (RXIN) or out (TXOUT) of the PCM interface, it may consist of a continuous clock or a train of pulses as defined in the data sheet. The frame sync, pulse FS should be high for one clock cycle of BCLK every 125 $\mu$ s.

The balanced inputs to the microphone amplifier MIC1 and MIC2 are on the MIC connector and also on a pair of BNCs, each has a DC blocking capacitor. An audio signal at -35 dBV with the input gain set to nominal will produce a 0 dBm0 PCM output signal. The connector also has AGND and VCC for biasing the microphone if this is required. The auxiliary audio input and output are also on this connector.

The output from the summing amplifier LSC2 is taken to the LS connector where it should be connected to the input to the Loudspeaker amplifier LSC1 either directly or via an external filter if that is required. The balanced outputs from the Loudspeaker amplifier LSOPP and LSOPN are then taken to the same connector and to a pair of BNCs.

The control interface to both codecs comes through the parallel data cable from the PC. The four control inputs to each codec are driven from the data port via open collector buffers. Other signals are routed through the PCs Control and Status registers on the same connector. N.B. if two or more parallel ports are detected the lowest number port will be used.

As the interfaces take significant current the codec power consumption cannot be measured with this board.

### Clock Circuits

The on board clock generator circuitry needs to be powered by a separate 5 V  $\pm 10\%$  supply (VDD). A crystal oscillator provides a 16.384MHz clock from which all the on board timing signals are derived. These signals are then passed through open collector buffers to convert the signals to 3V logic levels. The signals produced are, BCLK\_OUT (a 1 MHz square wave), FIN\_OUT (32kHz square wave) and FS\_OUT (a pulse every 125 $\mu$ s).

## AN151

The clocks can be controlled by an option on the opening menu. They should be switched off if external timing signals are being supplied to the codecs.

### SOFTWARE DESCRIPTION

The Software allows complete control of the internal registers of both MV3100 codecs on the demonstration board. It is designed to run on any IBM PC or compatible with DOS 2.11 or later, a screen that will display 80 x 25 text and a parallel port. It will also run as a DOS application under Windows or OS/2.

The software requires ansi.sys to be loaded. If the Control Menu (see below) appears with a jumble of numbers and square brackets at the bottom of the screen ansi.sys is not loaded. Quit the programme and use a text editor to add a line such as "device = c:\dos\ansi.sys." to the config.sys file and reboot the computer. The Program should now run correctly.

The opening screen offers a choice of the two codecs to program or a short screen of instructions. Choosing 1 or 2 will display the control menu of the appropriate codec. This shows the status of all the programmable settings of the device. Option 3 will display a short list of instructions. Option 4 allows the on board clock to be switched on or off. Option 5, Q or Esc will exit to the operating system.

### Control Screen

Each codec has a separate control screen. On initial entry the program displays the codec status at power up.

The Control screen with the codec set for normal use will look similar to that below.

```
GEC - Plessey Semiconductors : MV3100 CODEC number 2 : Control Software

                                MENU

Digital circuitry                Active
PLL and Voltage reference        Active
Microphone amplifier            Active
Loudspeaker amplifier           Active
Auxiliary amplifier             Active
Base Station mode               Off
Sidetone path                   On
PLL clock enable                On
Auxiliary input                 Off
Transmit mute                   Normal
Receive mute                    Normal
P.C.M. Mode                     Linear
Transmit Main Path Gain         +34.8dBm0/dBv
Transmit Auxiliary Path Gain    +19.9dB
Receive Main Path Gain         -6.1dBv/dBm0
Receive Auxiliary Path Gain     +13.4dB
Sidetone Gain                   +25.7dB

1. View Registers      2. Disk Interface    3. Update Registers    4. Quit
```

To change any setting move the cursor to the relevant line using the arrow keys. Use the + and - keys to change the value. Functions with only two options will toggle between them. The P. C. M. mode will cycle between Linear, A-Law and u-Law. Gain settings will increase (+) or decrease (-) until their limit is reached and then stop at that value. Note that gain changes can be made whether the amplifiers are in standby or active modes and that powering down the amplifier has no effect on the gain settings. As the main and auxiliary gains are set in an amplifier common to both paths changing one value also changes the other.

If any value is changed on screen new data is immediately sent to the codec register. If the program returns to the control menu from the disc interface menu with altered values, all registers and screen values are updated accordingly.

Other Control Screen options are:-

1. View Registers will display all the register contents in Hexadecimal and Binary.
2. Disk Interface will Select the Disc Interface Menu, see below.
3. Update Registers will program all six registers with the current settings.
4. Quit will return to the opening screen.

**As the program cannot detect if power is present on the board it is recommended that option 3 is used if either power supply to the board or the serial interface is interrupted. This will ensure that the status displayed will match that in the codec. Note that each codec will need to be updated separately each from it's own Control Screen.**

## Disc Interface Screen

On entry the screen will show the disc interface menu and the current register settings as hexadecimal numbers. These will change if new register settings are loaded.

The Disc Interface Menu allows the following actions:-

1. Load a set of register values from disk, the file must be ASCII text with the registers in order and their contents in hex separated from an equals sign by a space. Extra text notes are ignored. The file should have type extension .gps.
  2. Save a set of register values to disk as an ASCII text file. Do not specify an extension, .gps will be used.
  3. Register values to be set "Nominal " ie. all circuits switched on (apart from the Auxiliary input and Base station mode) and gain settings at the specified nominal levels (see data sheet).
  4. Register values to be set at the same status as when a codec has been reset or after power up.
  5. Return to the Control Menu with the modified register values and program the device with them.
- Q. Return to the Control Menu without changing the device or program registers.

### EXAMPLE SET UP

Connect the Evaluation board to a PC using the lead in the kit.

Connect AGND and DGND to the 0V of a power supply, 3V to VCC and 5V to VDD.

Connect FS\_OUT to FS\_1 and FS\_2; FIN\_OUT to FIN\_1 and FIN\_2; BCLK\_OUT to BCLK\_1 and BCLK\_2.

Connect TXOUT\_1 to RXIN\_2 and TXOUT\_2 to RXIN\_1.

Connect LSC1\_1 to LSC2\_1 and LSC1\_2 to LSC2\_2.

Connect a microphone (eg Panasonic WM-034) to each pair of MICIN inputs using suitable biasing.

Connect loudspeakers (eg Panasonic WM-70S) between each LSOPP and LSOPN.

Place the floppy disc supplied in the drive of the PC and run the program MV3100.EXE.

Select 1 from the opening menu followed by, 2 to get the disc interface menu, 3 to get the "nominal " register settings and 5 to load these settings to codec no 1. Now press 4 to return to initial menu and repeat the process for codec 2.

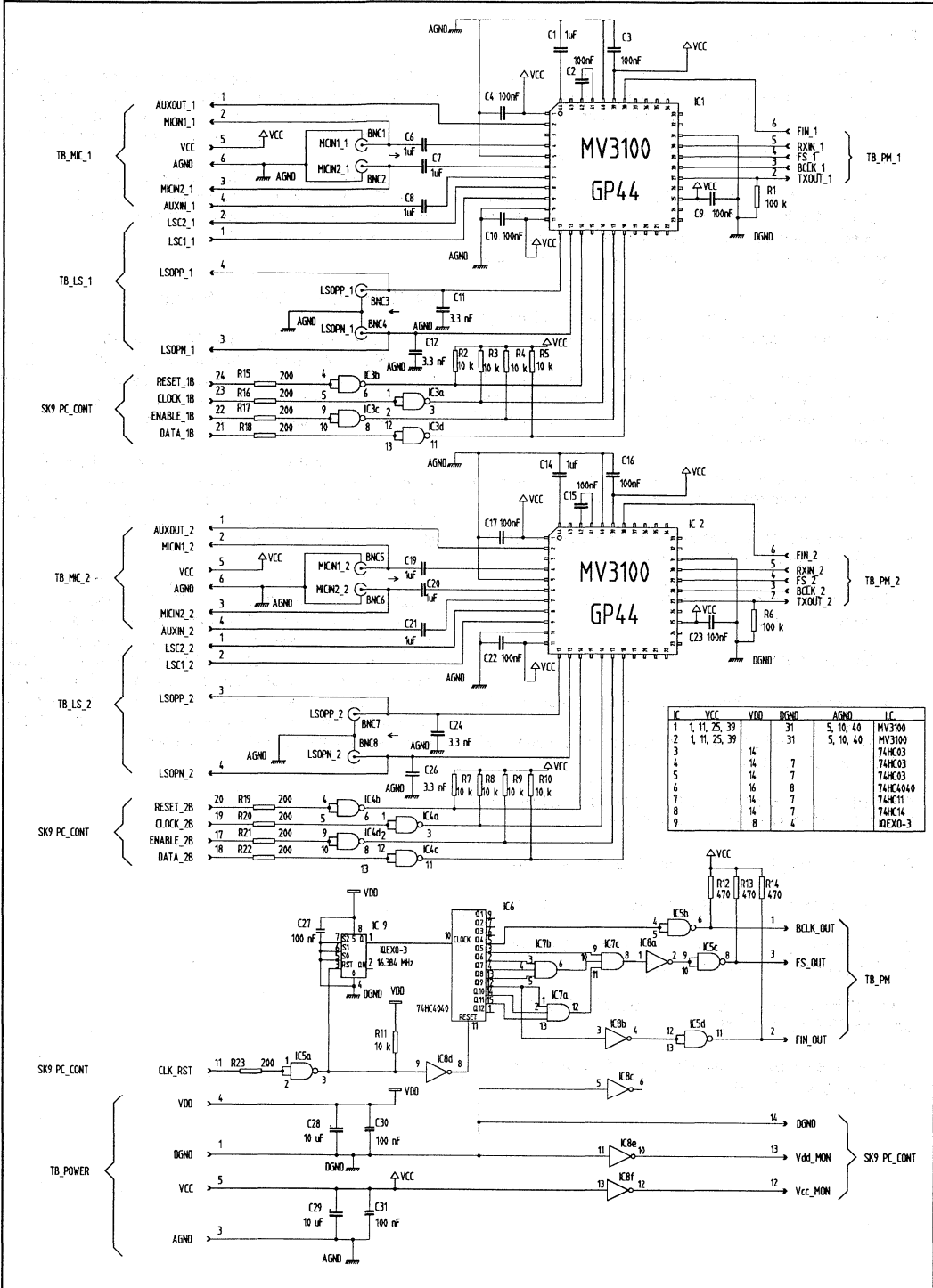
You should now have a full duplex link established using linear PCM. If you want to try companded speech, either A-Law or u-Law remember to set both codecs to the same mode otherwise it will sound awful!

### LAYOUT AROUND THE MV3100

The four ground pins, GNDTX (5), GNDRX (10), GNDD (31), GNDPL (40) must all be connected together preferably to a ground plane. If it is wished to separate the digital ground to reduce noise in the audio circuits, the two should meet at a single position, preferably close to the codec.

The four power pins  $V_{DD}TX$  (1),  $V_{DD}RX$  (11),  $V_{DD}D$  (25),  $V_{DD}PL$ (39) should all be connected to the same power rail. To reduce digital noise breakthrough into the analog they should be separately decoupled to the ground plane. Track lengths should be kept to a minimum.

The PLL capacitor should be close to the codec and track lengths to the pins CD0 (41), CD1(42) kept as short as possible. As far as possible noisy signals should be routed away from these tracks. The capacitor should be a low leakage type. In ceramic types X7R ( or NPO ) would be better than Y5V or Z5U, though of course more expensive. Better still would be certain types of plastic film capacitor but these tend to be larger and may not be available in surface mount form. A possibility is the Wima MKS01 series.



## A USER FRIENDLY GUIDE TO PLL SYNTHESISER DESIGN

An excellent and comprehensive treatment of PLL theory and design compromises for optimum performance is presented in the two application notes. It is however felt that a much simplified procedure for designing the loop filter used with the GPS NJ88XX series of synthesiser IC's was needed.

This simpler description is presented for those who do not require the ultimate performance from their PLL designs and should enable an adequate and reliable synthesiser to be designed.

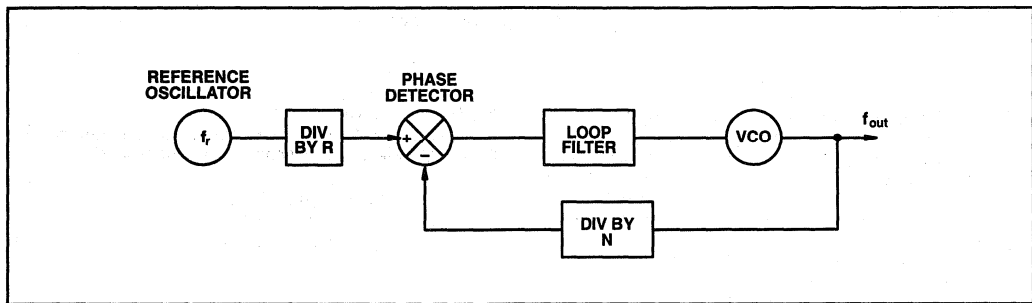


Fig.1 Basic phase locked loop

The basic PLL architecture shown in Fig. 1 will be used as the basis for this design procedure and we can calculate certain fundamental loop filter parameters common to all PLL synthesiser loops. Having obtained these we may then consider the implementation of different PLL filter configurations to suit different synthesiser types.

To begin we must consider the following parameters which arise out of the specification of the synthesiser application.

a). The comparison frequency ( $f_{comp}$ ) which is derived from the reference oscillator ( $f_r$ ) divided by R, (the reference divider ratio).  $f_{comp}$  is usually in the range 10KHz to 200KHz.

b). The output frequency ( $f_{out}$ ). This will determine the type of VCO used, e.g. a varactor controlled tuned circuit at VHF or a dielectric resonator for very low phase noise at SHF.

c). The total division ratio (N) which is the product of the internal divider ratio (M) and the external prescaler ratio (P) if one is used. The output frequency ( $f_{out}$ ) is  $N \times f_{comp}$ . so  $N = f_{out}/f_{comp}$ .

d). The frequency step size ( $f_{step}$ ) this may be equal to, or some multiple of the comparison frequency.

e). The settle time ( $t_s$ ) which for a given step size is the time taken for the output frequency to change and reach a given offset frequency ( $f_{os}$ ) from the required new output frequency.

f). The modulation frequency range. This will depend on whether speech or data is to be transmitted and is usually in the range 300Hz to 200KHz but may be in excess of 1.0MHz.

From the above criteria we can decide on suitable values for our basic loop parameters which are the filter's natural loop frequency ( $\omega$ ) and damping factor ( $\zeta$ ). In this simplified

treatment we will make  $\zeta=0.707$  which will give a loop that is critically damped (i.e. no overshoot). This is an assumption often made in PLL design.

The value of  $\omega$  must be less than half the minimum modulation frequency. If modulation is not used then it is desirable to make  $\omega$  as high as possible to give lowest "close-in" phase noise at the output. The choice of  $\omega$  will also affect the reference frequency sideband attenuation which is poor for a high  $\omega$ .

We may choose a fairly optimum value for  $\omega$  by using equation 1.

$$\omega = \frac{\ln E}{t_s f_{step}^2} \quad (\text{rad/sec}) \quad (1)$$

where  $E = \frac{f_{os}}{f_{step}}$

We are now in a position to consider some actual PLL circuits and determine the external component values required.

### Active loop filter topology

The first circuit topology is illustrated in Fig. 2 and is the one most commonly used with the NJ88C2X series of synthesisers. This circuit uses a low noise operational amplifier configured as an active filter followed by a passive RC filter.

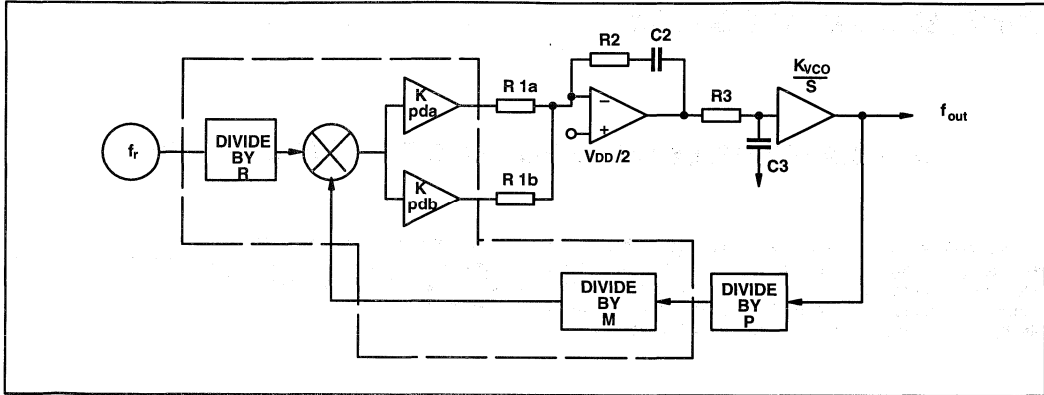


Fig.2 PLL circuit topology using active filter

The VCO gain ( $K_V$ ) is in general fixed for any given VCO and a VCO is chosen with sufficient gain ( $\text{rad/s/V}$ ) to give the required maximum frequency step size within the constraints of the op-amp output voltage swing. If the non-inverting input to the op-amp is biased at  $\frac{1}{2}V_{DD}$ , then the magnitude of the maximum output voltage step will be approximately  $(V_{DD}-1)-(\frac{1}{2}V_{DD})$ .

We now need to choose a value for the phase detector gain ( $K_{pd}$ ). In the NJ88C2X series of synthesisers we have effectively two phase detector outputs with gains  $K_{pda}$  and  $K_{pdb}$  respectively. The value of  $K_{pda}$  is controlled by the values of an external resistor RB and external capacitor CAP. Refer to the relevant data sheet on how to select these values. The value of  $K_{pdb}$  is  $V_{DD}/4\pi$  and is fixed by the supply voltage. The choice of  $K_{pda}$  will depend on factors such as the phase noise requirement of the synthesiser or the frequency aperture over which it operates. A typical value of  $K_{pda}$  would be  $200\text{V/rad}$ .

The next step is to select values for  $R_2$  and  $R_3$ . If we assume that the tuning range of the VCO 1V less than either extreme of the op-amp's linear range then the maximum voltage step range ( $V_{step}$ ) is 1V. This sets the minimum value for the  $R_2, R_3$  parallel combination. If we set  $R_2=R_3$  then;

$$R_2 = R_3 = 2 \left( \frac{V_{step}}{I_{max}} \right)$$

Where  $I_{max}$  is the op-amp's maximum output current.

We find the value of  $R_{1a}$  from equation 2.

$$R_{1a} = \frac{K_{pda}K_V R_2 (R + 2\zeta)}{N\omega(1 + 2\zeta R)} \quad (2)$$

The value of R in this equation is defined in the text of AN112 and is typically in the range 3 to 20.

It will depend on how we wish to compromise between comparison frequency sideband rejection and the possibility of loop instability. A fairly safe assumption is to make  $R=10$ .

To determine the value of  $R_{1B}$  we use equation 3.

$$R_{1b} = (dV_{pdb}/dV_{out})R_2 \quad (3)$$

Where  $dV_{pdb}=V_{DD}/2$  and  $dV_{out}$ = the maximum incremental voltage that can be permitted at the op-amp output, which is

the 1V found above.

All that now remains is to calculate values for the capacitors  $C_2$  and  $C_3$ . We use equations 4 and 5 respectively.

$$C_2 = \frac{K_V K_{pda} (2\zeta + R)}{N R R_{1a} \omega^2} \quad (4)$$

$$C_3 = 1/[\omega(2\zeta + R)R_3] \quad (5)$$

### Design example

As an example let us design a loop to meet the following specifications:-

- $f_{out} = 1\text{GHz}$
- $f_{comp} = 50\text{KHz}$  (hence  $N=20,000$ )
- $f_{step} = 100\text{KHz}$
- $f_{os} = 1\text{KHz}$
- $t_s = 1\text{ms}$
- modulation = none
- $V_{DD} = 5\text{V}$
- $I_{max} = 1\text{mA}$
- $V_{step} = 1\text{V}$
- $K_V = 189\text{Mrad/s/V}$
- $K_{pda} = 200\text{V/rad}$

$$\begin{aligned} \omega &= \frac{-\ln E}{t_s \zeta} \\ &= \frac{-\ln 0.01}{0.001 \times 0.707} \\ &= 6513 \text{ rad/s (1.04KHz)} \end{aligned}$$

$$\begin{aligned} R_2 = R_3 &= \frac{2V_{step}}{I_{max}} \\ &= 2\text{K}\Omega \text{ (use } 2.2\text{K}\Omega) \end{aligned}$$

$$\begin{aligned} R_{1a} &= \frac{K_{pda}K_V R_2 (R + 2\zeta)}{N\omega(1 + 2\zeta R)} \\ &= \frac{200 \times 189 \times 10^6 \times 2 \times 10^3 (10 + 1.414)}{2 \times 10^4 \times 6513 \times 15.14} \\ &= 437.5\text{K}\Omega \text{ (use } 430\text{K}\Omega) \end{aligned}$$

$$R_{fb} = \left( \frac{dV_{pdr}}{dV_{out}} \right) R_2 = \left( \frac{2.5}{1} \right) 2 \times 10^3 = 116nF \text{ (use } 120nF)$$

$$= 5K\Omega \text{ (use } 4.7K\Omega)$$

$$C_3 = \frac{1}{\omega (2\xi + R) R_3} = \frac{1}{6513 \times 11.414 \times 2 \times 10^3} = 6.7nF \text{ (use } 6.8nF)$$

$$C_2 = \frac{K_V K_{pdr} (2\xi + 1)}{NR R_{fb} \omega^2} = \frac{189 \times 10^6 \times 200 \times 11.414}{20 \times 10^3 \times 10 \times 437.5 \times 10^3 \times 42.4 \times 10^6} = 95nF \text{ (use } 100nF)$$

**Passive loop filter topology**

The other circuit topology to be considered is shown in Fig.3 and is used with the NJ88C33 synthesiser. Unlike the

previous example there is only one phase detector output and the loop filter is passive.

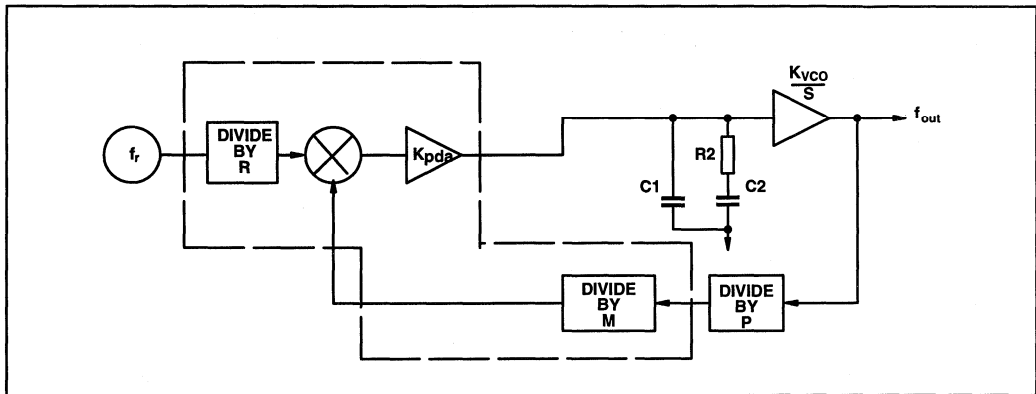


Fig.3 PLL circuit topology using passive filter

We obtain values for  $\omega$  and  $\xi$  in the same manner as we did for the previous loop filter type. In this example the value of  $R$  is set equal to 6. The VCO gain (specified in MHz/V) is again fixed, as is the phase detector gain in this type of synthesiser (specified in amps/Hz).

$$K_V = 5\text{MHz/V}$$

$$K_{pd} = 2.5 \times 10^{-3} \text{A/Hz}$$

We now calculate the value of  $C_1$  from equation 6.

$$C_1 = \frac{K_V K_{pd}}{N\omega^2(1 + 2\xi R)} \tag{6}$$

$$\omega = \frac{-\ln E}{t_s^2} = \frac{-\ln 1 \times 10^{-4}}{4.14 \times 10^{-3} \times 0.707} = 3.139 \times 10^3 \text{ rad/s (500Hz)}$$

In order to find the values of the remaining two components  $C_2$  and  $R_2$  we use equation 7 to determine  $T_2 (= R_2 C_2)$  and equation 8 to find the value of  $C_2$ .

$$T_2 = \frac{(2\xi R + 1)}{\omega R} \tag{7}$$

$$C_1 = \frac{K_V K_{pd}}{N\omega^2(1 + 2\xi R)} = \frac{5 \times 10^6 \times 2.5 \times 10^{-3}}{1400 \times (3.139 \times 10^3)^2 \cdot (1 + 2 \times 0.707 \times 6)} = 95nF \text{ (use } 100nF)$$

$$C_2 = C_1 [\omega T_2 (2\xi + R) - 1] \tag{8}$$

$$T_2 = \frac{2\xi R + 1}{\omega R}$$

**Design example**

As an example we will design a loop to meet the following specifications:-

- $f_{out} = 70\text{MHz}$
- $f_{comp} = 50\text{KHz}$  (hence  $N=1400$ )
- $f_{step} = 1\text{MHz}$
- $f_{os} = 100\text{Hz}$
- $t_s = 4.15\text{ms}$
- modulation = none

$$= \frac{2x \cdot 707x6 + 1}{3 \cdot 139x10^3x6}$$

$$= 504\mu s$$

$$C_2 = C_1[\omega T_2(2\xi + R) - 1]$$

$$= 95x10^{-9}[504x10^{-6}x3 \cdot 139x10^3(1 \cdot 414 + 6) - 1]$$

$$= 1 \cdot 02\mu F \text{ (use } 1\mu F)$$

$$R_2 = \frac{T_2}{C_2} = \frac{504x10^{-6}}{1 \cdot 02x10^{-6}}$$

$$= 494\Omega \text{ (use } 470\Omega)$$

### Conclusion

The two examples given above should enable someone with little or no experience of PLL design to make an adequate synthesiser loop filter. It is not expected that this simple approach will achieve the best possible performance in terms of settle time or phase noise. For more exacting applications refer to application notes AN112 and AN94.



# Multimodulus Division

This Application Note compares the various techniques currently employed in phase locked loop (PLL) frequency synthesiser designs with the technique of multimodulus division embodied in the GPS NJ882X series of synthesiser controllers when combined with the SP87XX series of two-modulus prescalers.

## DIRECT DIVISION

Phase Locked Loop Frequency Synthesisers of the form shown in Fig. 1 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolescent, guaranteed operation above about 50MHz still requires relatively high power.

## FIXED PRESCALING

Fixed prescaling, as in Fig. 2, is widely used, but for a division ratio of  $P$  in the prescaler, the phase comparison frequency of Fig. 1 has been reduced by a factor of  $1/P$ . This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock-up time.

## MIXING IN THE LOOP

One alternative to fixed division is mixing, as in Fig. 3. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, it is certainly complicated in terms of its physical realisation, requirements for 'adjust on test' parts, and in its susceptibility to layout problems.

## MULTIMODULUS DIVISION

The multimodulus divider system, shown in Fig. 4, is significantly less complicated. It is built up from a number of blocks.

1. A two-modulus prescaler which will divide by one of two numbers  $P$  or  $P + 1$  (e.g., 10/11, 64/65 etc.).
2. A programmable 'A' counter, the output of which controls the modulus of the prescaler.
3. A programmable 'M' counter which is clocked in parallel with the 'A' counter. In most of the NJ882X series, the output of the 'M' counter resets both itself and the 'A' counter (see Fig. 4).
4. A programmable Reference Frequency counter, 'R', the division ratio of which is determined by the reference frequency  $f_{osc}$  and the desired channel spacing (see below).

### Principle of Operation

The 'A' counter is programmed to a smaller number than the 'M' counter, and assuming the counters to be empty, the system starts with the prescaler ( $P/P + 1$ ) dividing by  $P + 1$ . This continues until the 'M' counter is full. As the 'M' counter has received  $A$  pulses, this counter overflows after  $(M - A)$  pulses, corresponding to  $P(M - A)$  input pulses to the divider. Thus the total division ratio  $N$  is given by:

$$N = (P + 1)A + P(M - A) = PM + A$$

Obviously,  $A$  must be equal to or less than  $M$  for the system to work, while for every possible channel to be available, the minimum total divide ratio is  $P(P - 1)$  while the maximum total division ratio is  $M(P + 1)$ .  $A_{max}$  should be  $\geq P$ .

Although simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the  $(P + 1)$ th pulse appears at the two-modulus prescaler input. After some time  $t_{p1}$  the output produces a pulse, which clocks the A and 'M' counters. Assume that the 'A' counter is filled by the pulse,

and so after a time  $t_{p2}$  (determined by the propagation delay of the 'A' counter), an output is produced to set the two-modulus prescaler ratio to  $P$ . After a set time  $t_s$ , the dual modulus divider will divide by  $P$ . But if  $t_{p1} + t_{p2} + t_s$  is greater than  $P$  cycles of input frequency, the divider will not be set to divide by  $P$  until after  $P$  pulses have appeared, and the system will fail.

$$\text{Thus, } \frac{P}{f_{VCO}} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances MUST be used if the reproducibility of the design under temperature and voltage extremes is not to be compromised.

The value of  $P$  must also be large enough that the output frequency from the prescaler does not exceed the maximum input frequency of the following circuitry. In single-chip MOS controllers this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the 'A' and 'M' counters trigger. If the edges are opposite then the loop delay may be increased by a large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of  $P$  is therefore settled by these constraints, but the actual choice of  $P$  may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency (channel spacing)  $f_{comp}$ , using a  $\div 40/41$  prescaler.

At 156MHz:

$$N = 156/0.025 = 6240$$

therefore  $PM + A = 6240$

$$40M + 0 = 6240 \quad (A = 0 \text{ for the lowest channel})$$

$$M = 156$$

In general, where

$$f_{VCO} P = 1 \text{ or } 10 \text{ or } 100$$

$$M = f_{VCO} / f_{comp} \div 10, f_{VCO} \div 100 \text{ etc.}$$

and similarly for the binary division ratios.

The choice of prescaler is therefore determined by:

1. VCO frequency
2. Total loop delay.
3. Prescaler output frequency must be within the controller input frequency band.
4. Programming ease.

## REFERENCE FREQUENCY DIVISION RATIO ( $R$ )

The value of  $R$  is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal sizes. Normally a frequency between 4 and 15 MHz is used, especially as in double conversion equipments commonality of oscillators may be possible. For example, with a 5kHz comparison frequency and 10-240MHz 2nd local oscillator frequency,

$$R = \frac{(10 \cdot 240 \times 10^3)}{(5 \times 10^3)} = 2048$$

Note that, for the NJ882X series, the reference counter division ratio is twice the programmed value and is therefore always even (see AN133 and individual data).

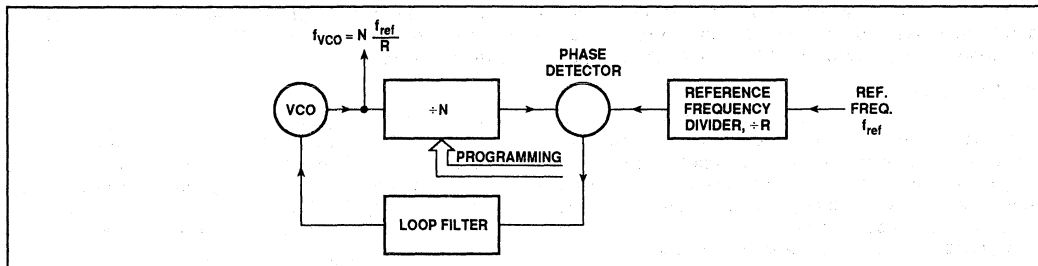


Fig. 1 Direct division

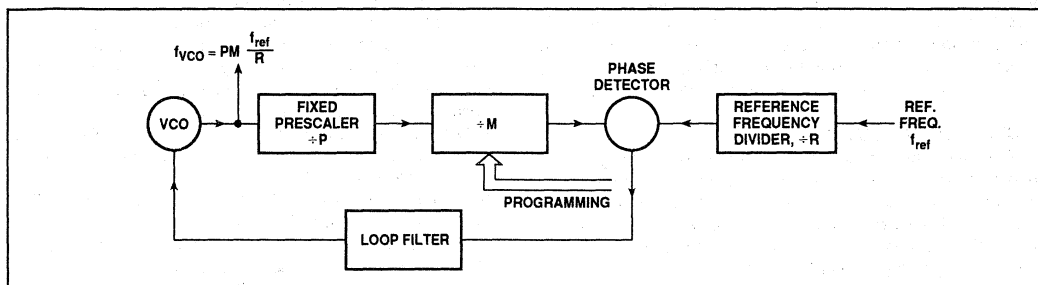


Fig. 2 Fixed prescaling

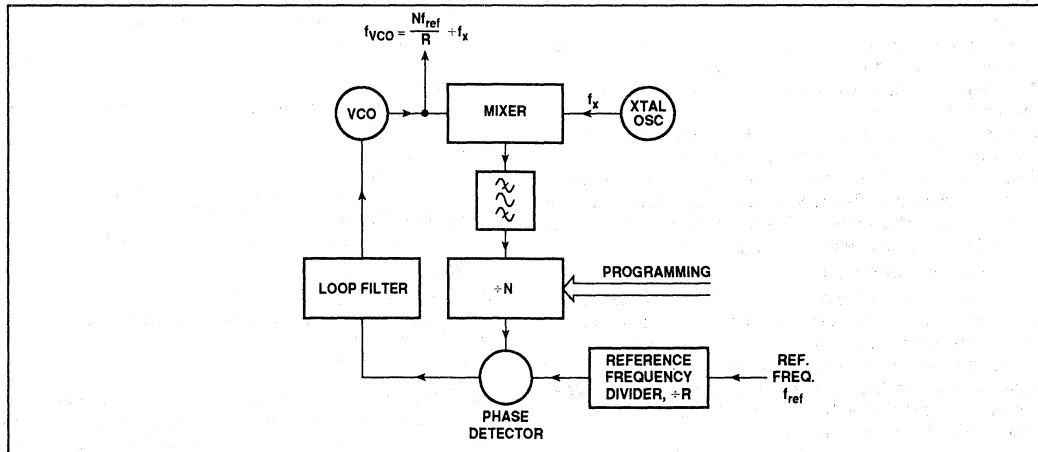


Fig. 3 Mixing in the loop

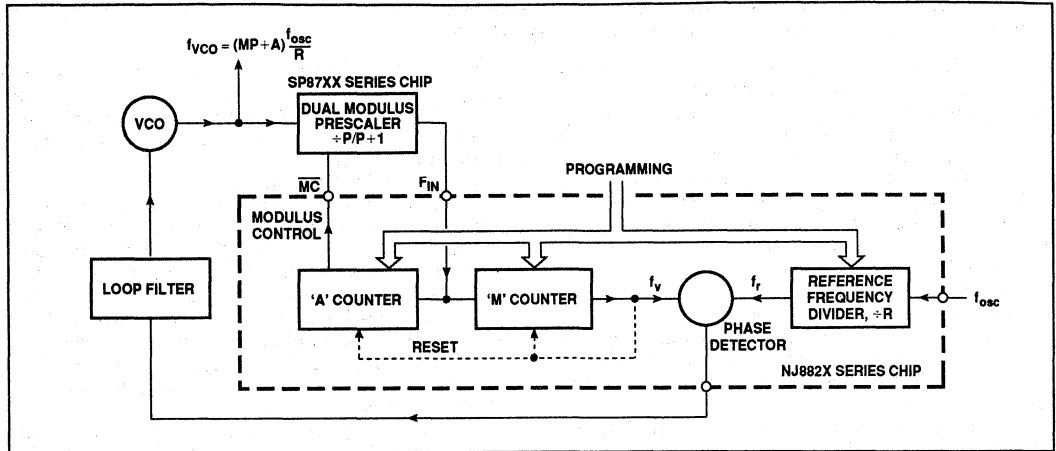


Fig. 4 Multi-modulus division. The NJ8823, NJ88C24 and NJ88C28 have non-resettable counters for faster loop lock-up times; see individual data.

# Programming the NJ8820 and NJ8821/23

AN133

The NJ8820, NJ8821 and NJ8823 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices are in hardware programming methods.

The basic system of a single loop frequency synthesiser is shown in Fig. 1, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1/3 is programmed by 8 4-bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the 'A' counter (7 bits), the 'M' counter (10 bits) and the reference or 'R' counter (11 bits).

## ADDRESSING

Addressing is by one of three modes. These are:

### A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a Data Read cycle commences every  $1024/f_{osc}$  seconds.

In this Data Read cycle the Memory Enable pin ( $\overline{ME}$ , NJ8820 only) is pulled low, and the Data Select outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the data on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edges of the Data Select pulses (see Fig. 2).

Note that the Program Clock is internally derived and is at a frequency of  $f_{osc}/64$ . The PE (Program Enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, however, as noise from the digital data may be picked up by the phase locked loop.

### B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input which initiates a data read cycle as outlined above; on the NJ8820, the  $\overline{ME}$  pin goes high at the end of the cycle, thus minimising power consumption. 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

### C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one to be entered.

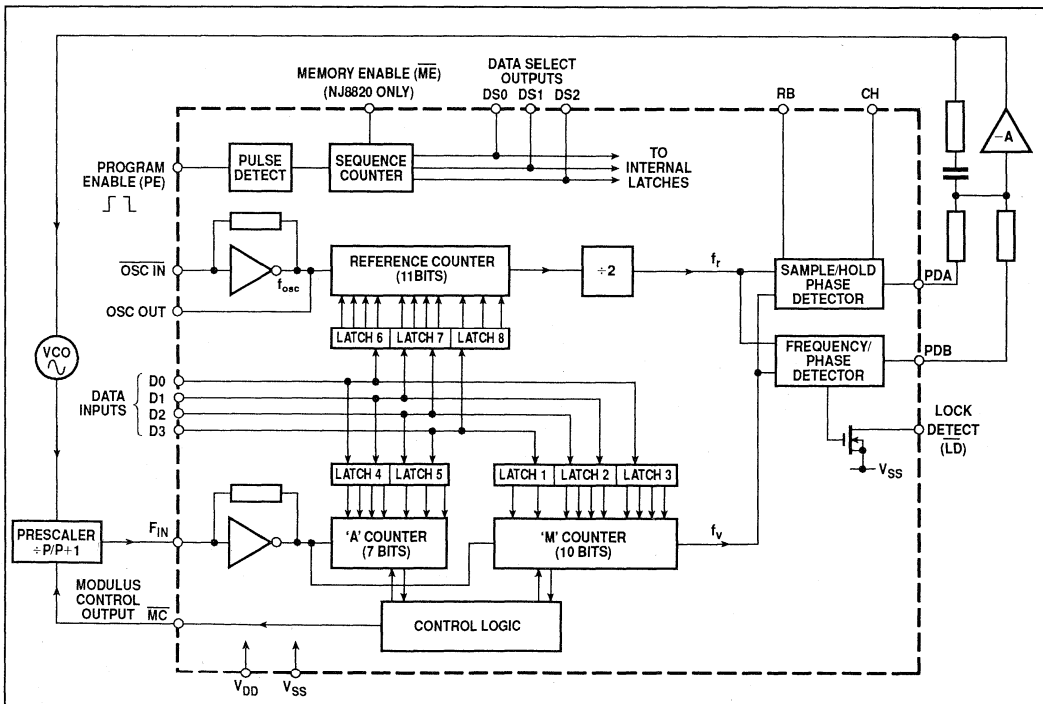


Fig. 1 The phase locked loop

**WORD VALUES**

For any particular set of conditions — namely operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator — a unique set of programming words exists.

**Reference Divider**

This divider produces the comparison frequency required by the synthesiser. The division ratio is programmable from 6 to 4094 in steps of 2, the programmed number being half the division ratio. Therefore, if for example a 10MHz crystal is used, and a 12.5kHz comparison frequency is required, this counter would be programmed to give a ratio of  $100000 \div 12.5 = 800$ . The actual programmed number would thus be 400, entered in binary according to the data map, Table 1.

Word	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 1 Data map

**'A' and 'M' Counters**

The 'A' counter is a 7-bit counter and the 'M' counter is a 10-bit counter. The programming calculations are as follows:

1. The 'A' counter should contain  $x$  bits such that  $2^x = M$ .
2. If more bits are included in the 'A' counter, these should be programmed to zero.

e.g.  $M = 64 = 6$  bits  
 $A = 10$  bits  
 then the 4 MSB are programmed to zero.

3. The 'M' and 'A' counters are treated as being combined so that the MSB of the 'M' counter is the MSB of the total and the LSB of the 'A' counter is the LSB of the total.

For example, a synthesiser operating from 430 to 440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.

$$N = f/f_c \text{ where } f_c = \text{channel spacing} = 25\text{kHz}$$

$$N_{min} = 430/0.025 = 17200$$

$$N_{max} = 440/0.025 = 17600$$

Minimum possible division ratio is  $P^2 - P = 4032$  where  $P$  is the two modulus prescaler ratio.

Maximum allowable loop delay =  $64/(440 \times 10^6) = 145\text{ns}$ .

Total division ratio,  $N$ , is given by

$$N = PM + A$$

$P = 64$ , as a 64/65 prescaler is used

$$N_{min} \text{ from above is } 17200$$

Therefore  $17200 = 64M + A$

and  $M \geq A$ .

Let  $A = 0$  then  $M_{min} = 17200 \div 64 = 268.75 = 268$

and  $M_{max} = 17600 \div 64 = 275.0$

Thus the 'M' counter must be programmable from 268 to 275 as required: the 'M' counter must have at least 9 bits.

For a frequency of 433.975MHz

$$N = 433.97 \div 0.025 = 17359$$

therefore  $M = 17359 \div 64 = 271.2343$

The 'A' counter is programmed for the remainder i.e.  $0.2343 \times 64 = 15$

From this, the 'A' counter is programmed to 15 and the 'M' counter to 271. The output frequency can now be checked.

$$N = PM + A$$

$$= 271 \times 64 + 15 = 17359$$

and this is the required frequency divider ratio.

Repeated calculations for memory programming may be easily evaluated using a programmable calculator.

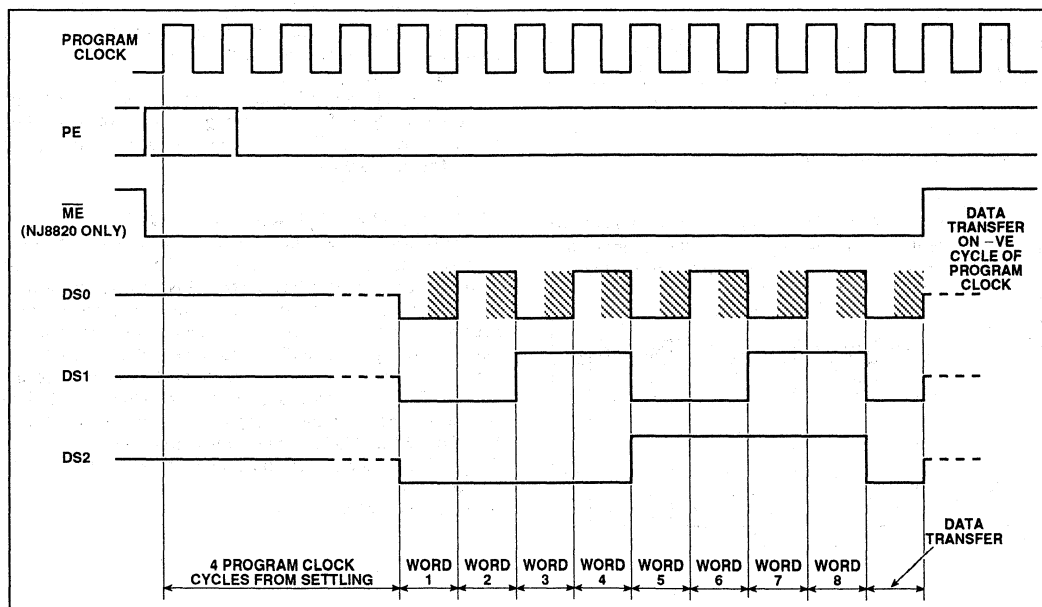


Fig. 2 Data selection

**SYNTHESISER DESIGN EXAMPLE**

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** (see AN132 for criteria)  
The SP8718 is one choice. Since it divides by 64/65 then  $P = 64$ .
- **Choose the comparison frequency,  $f_r$**   
25kHz is the required channel spacing and is the best choice in this case.
- **Calculate the crystal frequency**  
2.5MHz is one possibility. The value of  $R$  can now be calculated.  
Crystal frequency = comparison frequency  $\times R \times 2$  so  $R = 50$ .
- **Calculate the division ratio.** (The ratio between the VCO output frequency and comparison frequency.)  
This is 17200 to 17600 in steps of one.
- **Calculate values for A and M.**  
The division ratio  $PM + A$  is 17200 to 17600.  
So for the minimum frequency:  $64M + A = 17200$   
If  $A = 0$ ,  $M = 268.75$   
This is not possible (it must be an integer) so this must be decreased to make  $M_{min} = 268$ .
- **Draw up a table** for the required values of A and M.  
Division ratio  $N = PM + A$

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430.000
...	49	17201	430.025
...	50	17202	430.050
...	...	...	...
...	...	...	...
268	63	17215	430.375
269	0	17216	430.400
...	...	...	...
...	...	...	...
...	...	...	...
...	...	...	...
...	...	...	...
274	63	17599	439.975
275	0	17600	440.000

Table 2. Decimal values of A and M.

$= 64M + A$ .

These figures are acceptable:

$P \geq A$   
 $N > P^2 - P$

The values of M, A and R must be fed into the NJ8820/1 for each value of the frequency required. (In this example the value of R is constant.) The values must first be converted into

M (decimal)	M (10-bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
269	0	1	0	0	0	0	1	1	0	1
...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 3a. Binary values for M.

A (decimal)	A (7-bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 3b. Binary values for A.

R (decimal)	R (11-bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0

Table 3c. Binary values for R.

binary format as shown in Table 3.

In each case the LSB is identified by the heading M0, A0 or R0.

The NJ8820 and NJ8821/3 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ2280 — data obtained from a PROM.

NJ8821/3 — data obtained from a microprocessor.

**USING THE NJ8820.**

The NJ8820 operates with an external 4-bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the PE pin is activated. A 1024-bit PROM (256  $\times$  4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256  $\times$  4 PROM has 8 address lines (A0 to A7) of which the NJ2280 can address three (A0 to A2, connected to DS0 to DS2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case) as shown in Table 4, so for each channel number there are 8 words, each of four bits. The composition of these words is as shown in Table 5. 'X' indicates that this is not read; normally the 8-bit value is 0.

The value of the bits D3, M1 etc. can be either 0 or 1, and can be found from Tables 1 through 4. For example, when  $M = 268$  then (from Table 3a)  $M1 = 0$ ,  $M0 = 0$  and (from Table 4) word 1 is 0000.

**USING THE NJ8821/3 IN A PARALLEL MODE.**

The NJ8821/3 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the 'M' counter, 4 and 5 the 'A' counter, 6 to 8 the 'R' counter. It is not necessary to transfer all the words every time: WORD 1 indicates to the NJ2281/3 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and the NJ8821/3:

- DS0, DS1 and DS2 to select the correct word.
- D0, D1, D2 and D3 are the input data for 'A', 'M' and 'R' counters.
- PE is the strobe.

To enter channel information follow the sequence listed below:

1. Ensure the PE (strobe) is 0.
2. Select any word (except WORD 1) ... (DS0 to DS2) and the relevant input data (D0 to D3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to ).
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for WORD 1.

The composition of the data words is the same as for the NJ2280.

#### Using The NJ8821/3 In A Serial Mode.

When used in a serial mode (using a single external shift register) the NJ2281/3 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the 'A', 'M' and 'R' counters, but only 5 words (35 bits) subsequently to reprogram the 'A' and 'M' counters. Thus there are only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig. 3. The composition and entry sequence of the data words is identical to that of the NJ2280 except that the data is transferred serially.

Once again there is no need to transfer all the words every time provided that WORD 1 is sent last.

		Address Lines								
		A7	A6	A5	A4	A3	A2	A1	A0	
Channel Number 0						0	0	0	0	Word 1
						0	0	0	1	Word 2
						0	0	1	0	Word 3
						0	0	1	1	Word 4
						0	1	0	0	Word 5
						0	1	0	1	Word 6
						0	1	1	0	Word 7
						0	1	1	1	Word 8
Channel Number 0	0	0	0	0	1	0	0	0	Word 1	
					1	0	0	1	Word 2	
					1	0	1	0	Word 3	
					1	0	1	1	Word 4	
					1	1	0	0	Word 5	
					1	1	0	1	Word 6	
					1	1	1	0	Word 7	
					1	1	1	1	Word 8	

Table 4 Channel Identification

Word	Address Lines			Address Lines			
	A2	A1	A0	D3	D2	D1	D0
1	0	0	0	M1	M0	X	X
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	X	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	X	R10	R9	R8

Table 5 Channel number composition

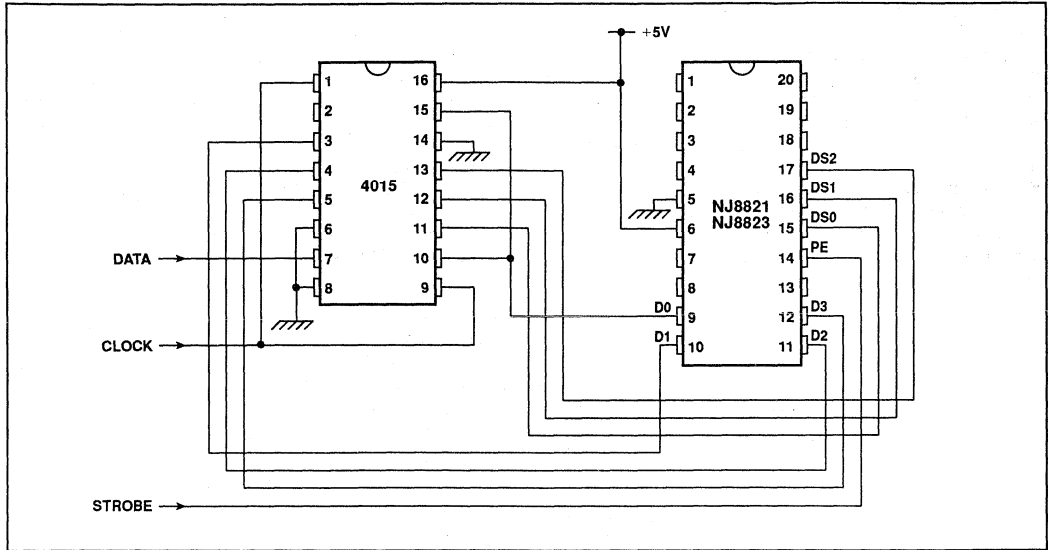


Fig. 3 NJ8821/NJ8823 serial mode connections

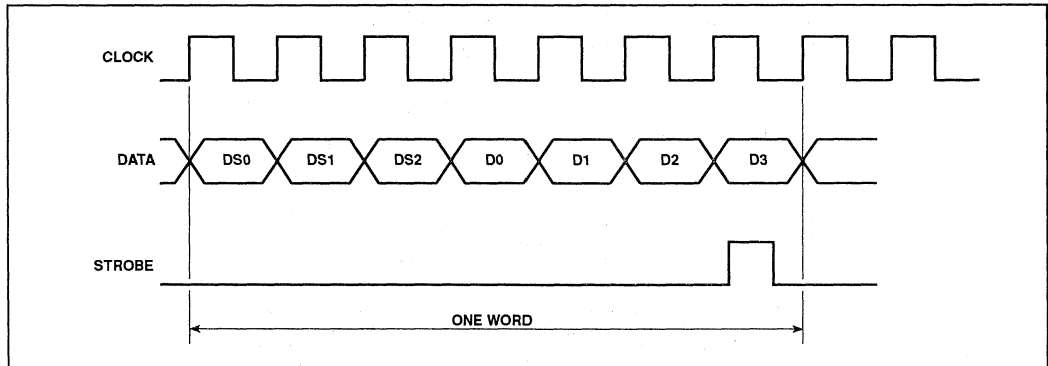


Fig. 4 Serial data timing



# Tuned Amplifier Application for the SL6140

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends upon the Q factor of the tuned/matching circuits used.

Fig. 1 shows a single ended amplifier with tuned input and output networks.

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), the other input being decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high impedance of the device (see Smith chart, Fig.3). The tuned frequency is given by the following equation:

$$f = \frac{1}{2\pi \frac{\sqrt{L \times C \times C1}}{\sqrt{C + C1}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector outputs of the device to V<sub>CC</sub>. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised, but if too high an impedance is seen by the input or output of the device

the circuit may oscillate. L1 and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth, so for maximum gain the matching network should be designed to provide the minimum bandwidth necessary for the particular application.

An alternative method of tuning the output of the device is to transformer-couple to the 50Ω load as shown in Fig. 2. The primary winding is connected across the outputs (a centre tap providing V<sub>CC</sub>) and resonated at the required frequency with a capacitor. This circuit has a 6dB improvement of gain over the previous circuit as both outputs are used.

## PCB LAYOUT

For best performance a ground plane should be used with 50Ω source and load. Also the matching network and decoupling capacitors should be placed as close to the device as possible.

If a very high gain, low bandwidth amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

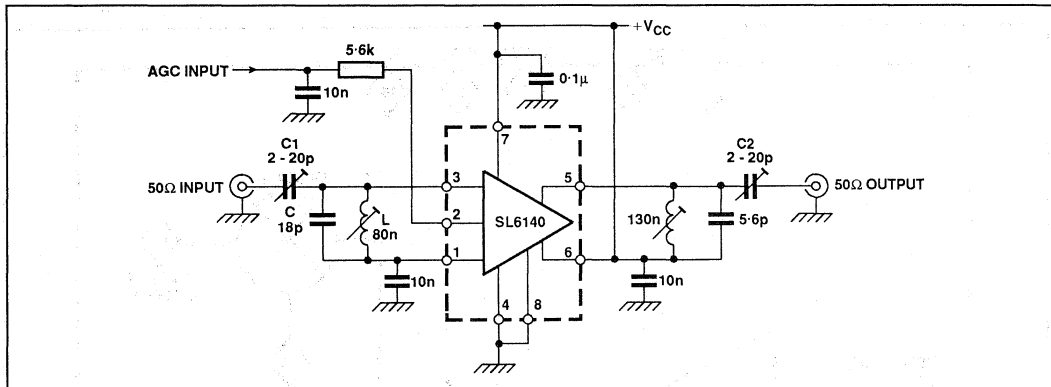


Fig. 1 A 100MHz tuned amplifier application with 35dB power gain (CM pinout)

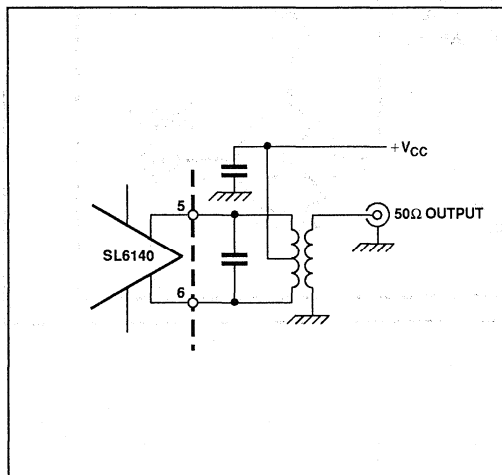


Fig. 2 Differential tuned output

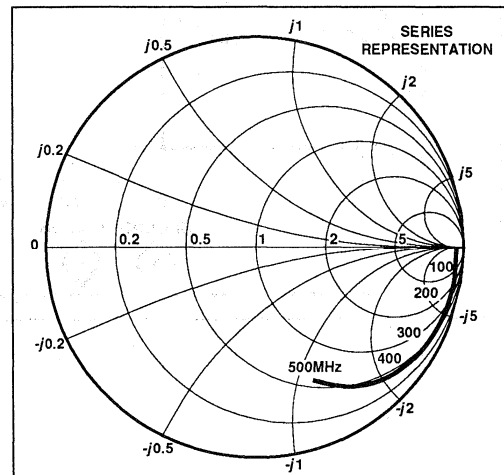


Fig. 3 Input impedance of SL6140 (50Ω normalised)

# SL6442

## APPLICATION CIRCUIT FOR USE AT 950MHz

This Application Note describes a circuit configuration which demonstrates the functions and performance of the SL6442 which is a 1GHz amplifier/mixer receiver front end.

A functional block diagram is shown in Fig. 1 and illustrates the main circuit elements.

Fig. 2 is a schematic diagram which illustrates the arrangement of the ancillary components required for optimum performance at 950MHz. Approximate starting values for these components were obtained using a Smith chart and data derived from s-parameter analysis of the SL6442.

The SL6442 contains a low noise amplifier which may be gain controlled by a D.C. signal, and two identical mixers suitable for either direct conversion I & Q receivers or image cancelling superhet receivers. There is also a battery economy facility. The device operates from a nominal 5V supply and draws about 4mA when powered up.

The actual component values were determined by using a linear circuit simulator such as Touchstone™. In this case the circuit is optimised for maximum gain and minimum input reflection coefficient at the required frequency.

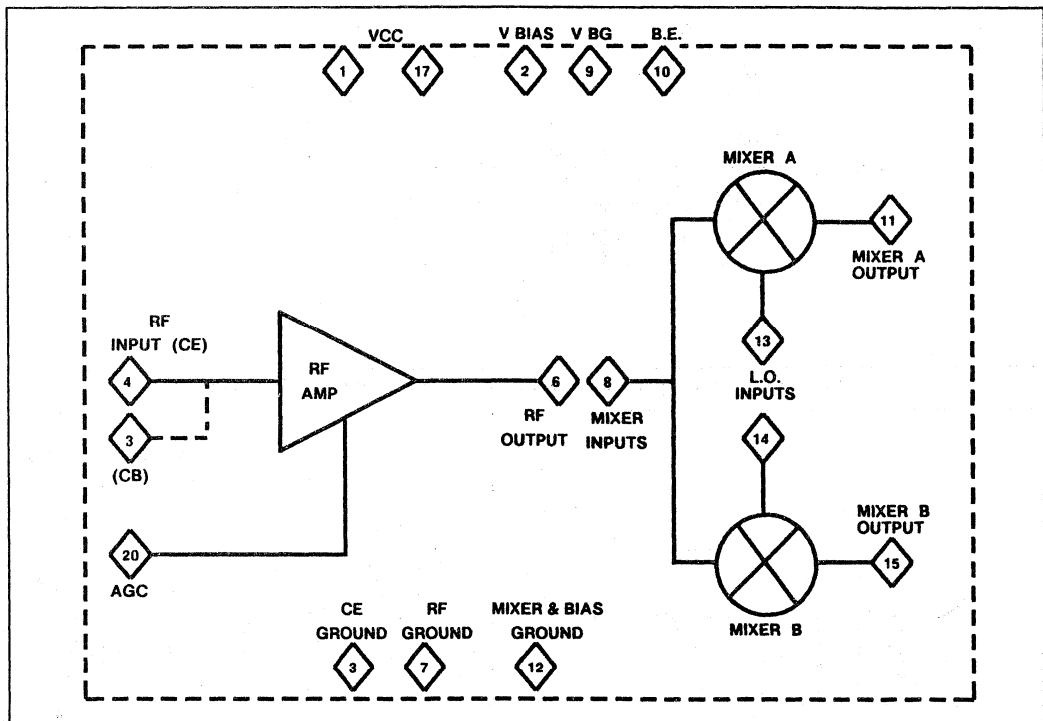


Fig.1

The input match is achieved by using a stripline shorted stub network. The LNA output to mixer input match is accomplished by using a series inductor and the mixer output to 50ohm match consists of a tunable LC network.

To prevent possible RF instability, pin2 (V bias) is decoupled with a series RC network as well as a 2.2 $\mu$ F capacitor. The quadrature phase shift network consists of phase lead and phase lag RC 'L' networks, which are capacitor coupled to the L.O. input pins. Inductor L3 serves to resonate out the parasitic capacitance between the two ports.

The exact values of the phase shift components have been determined empirically and the ones shown in the circuit diagram achieve an amplitude and phase imbalance of about 1dB and 4 degrees respectively.

The variable capacitors VC1 and VC2 are tuned for a maximum output level at an I.F. of 20MHz. Other I.F frequencies may require changing the values of the trimmers and/or L4 and L5. At zero I.F as in direct conversion receivers the output matching network is transparent.

If the AGC facility is not required it is necessary to connect pin 20 to pin 9 (VBG). The battery economy pin may be connected directly to ground if power down is not used.

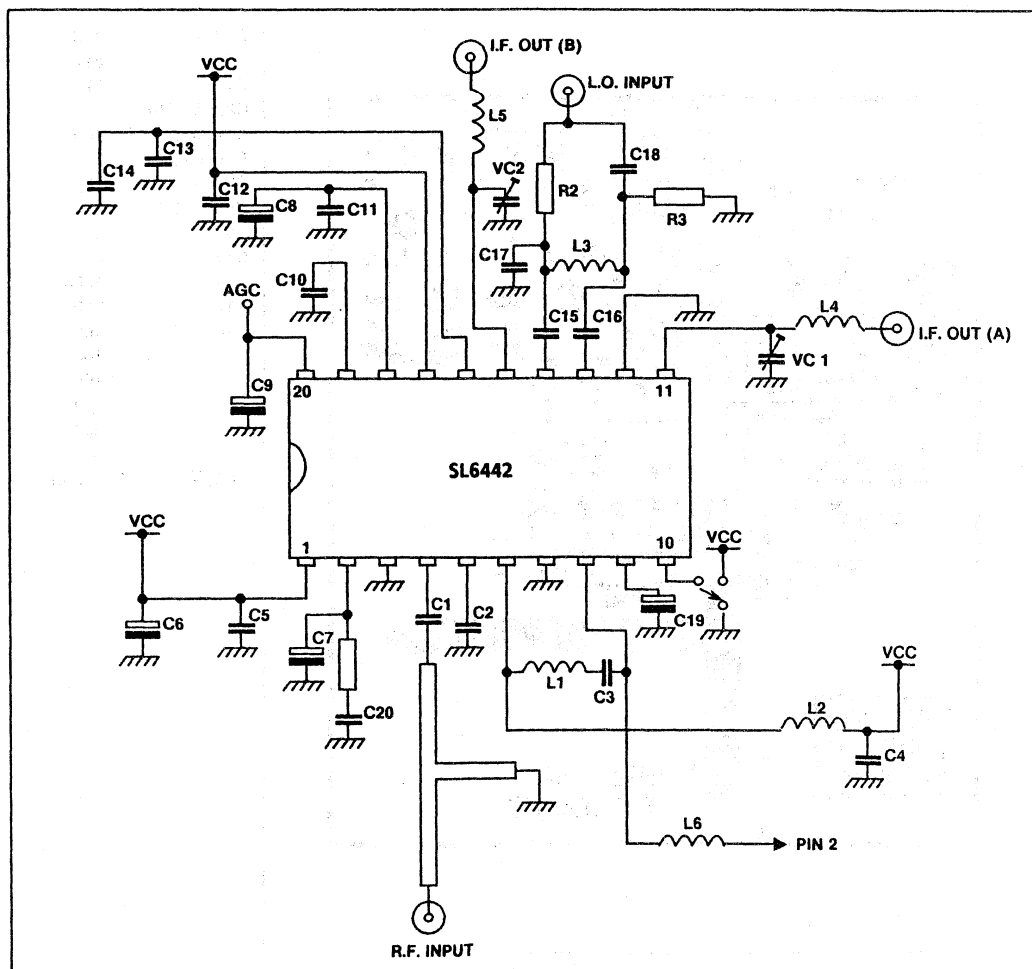


Fig. 2 Circuit diagram

**PERFORMANCE CHARACTERISTICS**

MEASUREMENT CONDITIONS:

- VCC = 5.0V. V<sub>gdc</sub> = 1.20V.
- Input/Output terminations = 50ohm
- L.O. drive level (into phase shift network) = -5dBm
- Temperature = 25°C

RESULTS

- Overall power gain (20MHz I.F.) 7dB
- Overall voltage gain (baseband) 33dB (Z<sub>L</sub> > 100k)
- 3rd. order input intercept (20MHz I.F.) -22dBm
- Overall DSB noise figure (20MHz I.F.) 8.2dB

The actual pcb layout and component values are shown in Fig. 3.

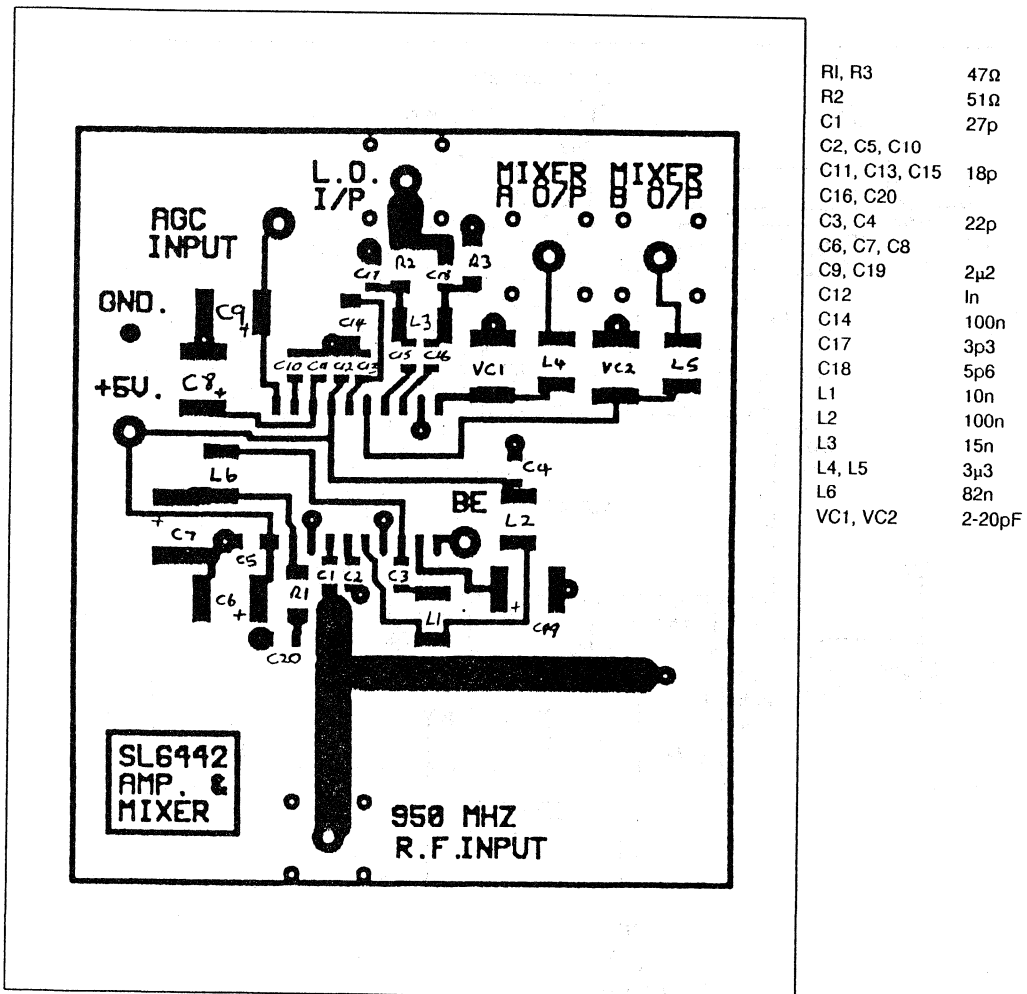


Fig. 3

# USING THE SL6444

## INTRODUCTION

The SL6444 is an RF amplifier and mixer combined integrated circuit for superhet receiver front end applications. It has been designed for low noise operation at frequencies up to 1GHz with low power consumption. The device includes a bandgap voltage reference and circuits necessary to bias the RF amplifier and mixer. A local oscillator buffer circuit is also provided for the mixer. This device is designed to meet requirements of RF front end circuits in CT2 cordless handsets but can be used in cellular radios, pagers and similar low power receiver applications. A block diagram of the device is shown in Fig. 1. Eight different application circuits are included in this applications note and the frequency of operation in each case is centred at 915MHz. Circuit diagram, PCB mask and performance results are provided in each application.

## RF AMPLIFIER

The SL6444 RF amplifier block is a simple unmatched cascode transistor arrangement. An internal schematic of the amplifier is shown in Fig. 2. The amplifier is intended for common emitter operation. The base of the upper transistor is biased from the  $V_{CC}$  supply line and decoupled by integrated capacitors. Additional external decoupling is possible via pin 5 (VCCDEC). Quiescent current in the amplifier transistors is established by connecting the base of the lower transistor pin 3 (RFIN) to pin 2 bias supply through a suitable inductor. The bias supply voltage is temperature compensated in which the gain of the amplifier is maintained over the temperature range. Because of its simplicity, the RF amplifier is versatile and can be adapted and optimised for a wide range of applications by the user. In most applications external impedance transformers which typically consist of inductors and capacitors are required at the input and output. Measured S parameters of the RF amplifier are shown in Fig. 3.

## MIXER

The SL6444 mixer circuit is a Gilbert multiplier cell with open collector outputs and single ended input. The complementary input being decoupled by an integrated capacitor. An internal schematic of the mixer is shown in Fig. 4 and input  $s$ -parameter in Fig. 5. The total mixer current is split into two equal parts which flows in either branch of the mixer. The mixer may be used in either single or double balanced configurations. In the single balanced configuration the matching of the input and output is relatively straight forward. The double balanced configuration requires an output transformer to provide balun action. The performance of the mixer then depends very much on the design of this transformer.

## APPLICATION CIRCUITS

The SL6444 amplifier and mixer can be configured into a variety of circuits for applications up to 1GHz. This ranging from RF receiver front ends to frequency up converters. Eight different applications circuits are included. Their nominal frequencies of operation are: RF at 915MHz and IF at 150

MHz. The RF input matching is a broadband design and the IF output circuitry is a selective tuned circuit.

## LOW NOISE AMPLIFIER

The amplifier requires DC bias at the input and output ports. The bias to the input port comes from the on-chip temperature compensated bias circuit through external inductors L1 and L2 as shown in Fig. 6. Transmission line T1, inductor L3 and trimmer capacitor VC2 perform RF matching to the amplifier input. Minimum noise performance can also be achieved using this input matching circuitry. The amplifier output port is matched to a 50ohm load impedance by the transmission lines T2, T4, short circuit stub T3 and trimmer VC3. Maximum amplifier gain and minimum noise figure can be achieved with this circuit configuration. The unused mixer ports are either terminated or decoupled to ground. Fig. 7 shows the measured input match characteristic centred at 915 MHz. Fig. 8 shows the gain of the low noise amplifier vs frequency. Typical measured noise figure is 2.9dB and third order intercept point at the input is  $-12\text{dBm}$ .

## RF AMPLIFIER

This RF amplifier circuit is similar to the low noise configuration except that the overall gain is reduced to about 11dB. This is achieved by having a gain dumping resistor between the amplifier output and a RF ground. In situations where high gain is a disadvantage, this circuit will reduce the overall gain and at the same time improves the third order intercept point. The measured noise figure is 3.4dB which is slightly higher than the minimum. Fig. 9 shows the RF amplifier circuit configuration. Fig. 10 shows the overall gain profile. The IP3 at the input is typically  $-4\text{dBm}$ .

## FEEDBACK AMPLIFIER

The feedback amplifier circuit shown in Fig. 11 is most suitable for broadband applications. The input and output matching circuits are designed for 50ohm operation. Lumped circuit elements are used through out, hence board space can be kept to a minimum. The unused pins of the mixer are decoupled to ground. The gain profile of the amplifier is illustrated in Fig. 12. Typical noise figure and IP3 are 4.5dB and  $-5\text{dBm}$  at the input respectively.

## SINGLE BALANCED MIXER

Fig. 13 shows the SL6444 configured as a single balanced mixer. The output of the mixer can be taken either from pin 10 or 11, in this case pin 11 is used and pin 10 is returned to  $V_{CC}$ . The input matching is done mainly by using lumped elements and only short transmission line is required. The RF input is matched to 50ohm at 915MHz. The LO input requires only AC coupling as the impedance at the mixer LO input pin is nominally 50ohm. The IF output is matched to 50ohm by a single tuned circuit which is formed by L1 and VC2. The IF frequency is chosen to be 150MHz and the bandwidth is relatively narrow due to the nature of the tuned circuit. However, other IF frequencies can be achieved by using different values for L1 and VC2. Conversion gain of 9.5dB can

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be obtained and the overall noise figure, is 9.5dB. LO–RF isolation is measured to be 26dB and the IP3 is approximately –10dBm at the input. The amplifier section of the integrated circuit is decoupled to avoid possible interference and also to reduce power consumption.

## MIXER

This circuit configuration is similar to the single balanced mixer except that the IF output matching is modified to give higher IP3. The mixer circuit is shown in Fig. 14. R1 acts as a gain dumping resistor which reduces the overall gain to 1.7dB. The IP3 however is improved to +1.9dBm.

## LOW NOISE FRONT END

The Low Noise Amplifier and the Single Balanced Mixer circuits are combined to form this low noise and high gain front end which is shown in Fig. 15. The interstage matching is carried out at a higher impedance level than 50ohm by VC2 and short circuit stub T2. This circuit is relatively broadband. The matching arrangement at the amplifier input is essentially the same as in the Low Noise Amplifier circuit. The IF output matching stage is formed by the tuned circuit VC3 and L5. The IF frequency is 150MHz which comes from a LO=765MHz and a RF=915MHz. The IF output return loss is shown in Fig. 16. The total gain is 27dB and the overall noise figure is 3.3dB. The IP3 is measured to be –30dBm at the input.

## RF FRONT END

This RF Front End circuit consists of the RF Amplifier and the Mixer in combination. Fig. 17 shows the circuit configuration. The interstage network is similar to that in the Low Noise Front End. The main feature of this circuit is the increased IP3 which in certain applications is more important. The total gain is measured to be 12dB and IP3 is –1 dBm. The overall noise figure is 4.4dB.

## UP CONVERTER

Fig. 18 shows the mixer section of the SL6444 configured as an up converter. Low frequency modulating signal (150MHz) is applied to the RF input of the mixer and the up converted signal at 915MHz (LO=765MHz) emerges at the IF port of the mixer. The short circuit stub T2 provides the output matching which is relatively narrow band. When a different IF centre frequency is required, the length of T2 i.e. position of C8 can be altered to give optimum results. This up converter circuit provides a gain of 3dB and LO–RF isolation of 42dB.

## SUMMARY

The SL6444 is a versatile RF integrated circuit. Eight different circuit configurations have been presented with which various RF front end functions can be obtained. The circuits described so far have been optimised to operate at 915MHz for RF, 765MHz for LO and 150MHz for IF. The table below summarises the main features of the application circuits for easy reference. The measurement set ups for gain, noise figure and IP3 are shown in the Appendix.

APPLICATION CIRCUIT	GAIN (dB)	NOISE FIGURE (dB)	IP3	FEATURES
LOW NOISE AMPLIFIER	18	2.9	–12	HIGH GAIN, LOW NOISE
RF AMPLIFIER	11	3.4	–3.4	HIGH IP3
FEEDBACK AMPLIFIER	12	4.5	–5	BROADBAND, HIGH IP3
SINGLE BALANCED MIXER	9.5	9.5	–10	GOOD CONVERSION GAIN
MIXER	1.7	–	+1.9	HIGH IP3 WITH CONVERSION GAIN
LOW NOISE FRONT END	27	3.3	–30	HIGH FRONT END GAIN, LOW NOISE
RF FRONT END	11.5	4.4	–13	GOOD IP3 AND GAIN
UP CONVERTER	3	(LO rejection 42dB)		UP CONVERSION WITH GAIN

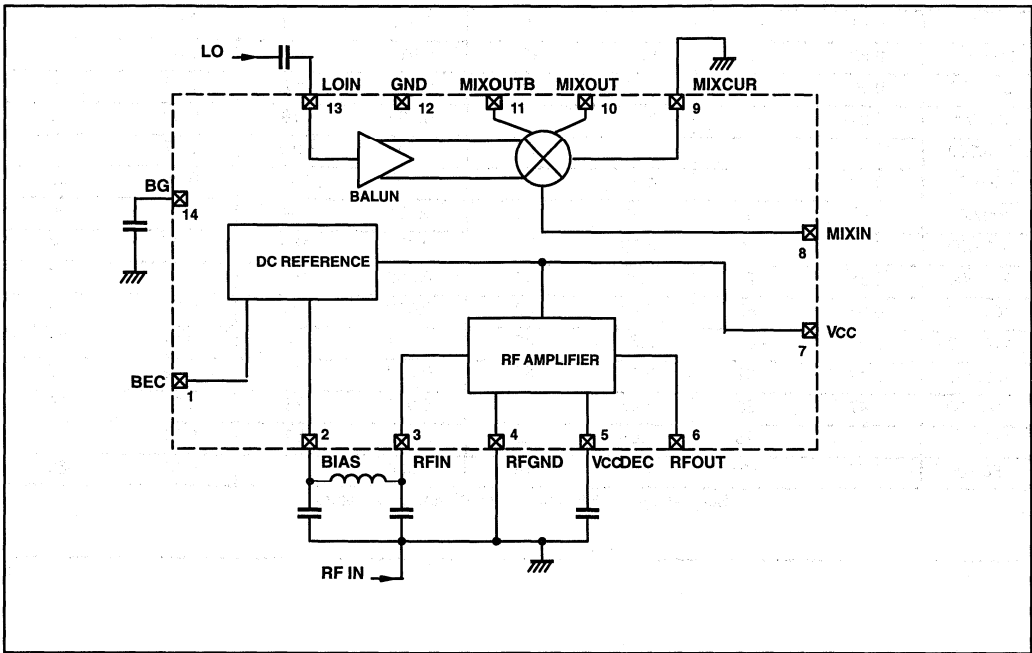


Fig. 1 Block diagram

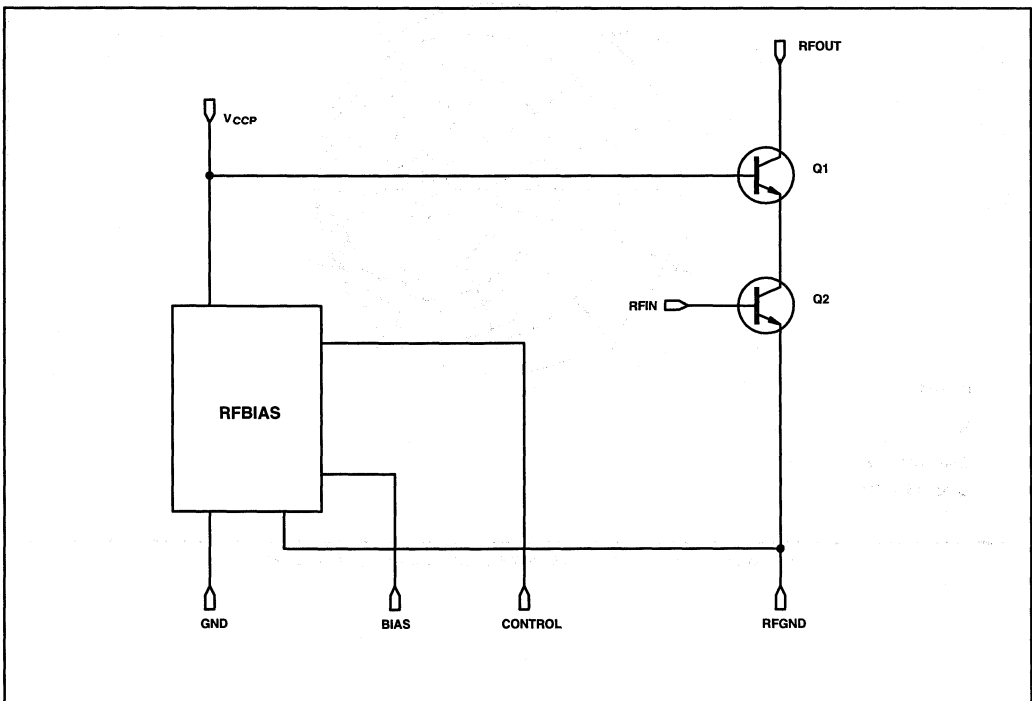


Fig. 2 Internal schematic of the RF Amplifier

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**V<sub>CC</sub>=5V Amplifier current 2.2mA**

FREQ MHZ	MAG [S11]	ANG [S11]	MAG [S21]	ANG [S21]	MAG [S12]	ANG [S12]	MAG [22]	ANG [S22]
100.000	0.91	-10	5.89	167	0.016	158	0.99	-5
200.000	0.89	-21	5.86	151	0.010	-75	0.99	-11
300.000	0.86	-30	5.60	136	0.004	55	0.99	-16
400.000	0.81	-39	5.19	121	0.003	118	0.98	-21
500.000	0.77	-47	4.86	108	0.004	-102	0.97	-25
600.000	0.72	-55	4.48	95	0.005	154	0.98	-32
700.000	0.67	-63	4.11	84	0.004	134	0.97	-38
800.000	0.62	-70	3.73	73	0.008	165	0.97	-44
900.000	0.58	-77	3.35	61	0.008	150	0.94	-52
1000.00	0.55	-83	2.97	52	0.010	117	0.91	-59
1100.00	0.52	-87	2.64	43	0.014	97	0.87	-66
1200.00	0.49	-92	2.32	34	0.013	82	0.82	-73
1300.00	0.47	-95	2.06	28	0.010	78	0.76	-79
1400.00	0.45	-98	1.85	22	0.009	59	0.71	-85
1500.00	0.45	-101	1.71	16	0.004	80	0.67	-89

SL6444 Typical RF Amplifier scattering parameters

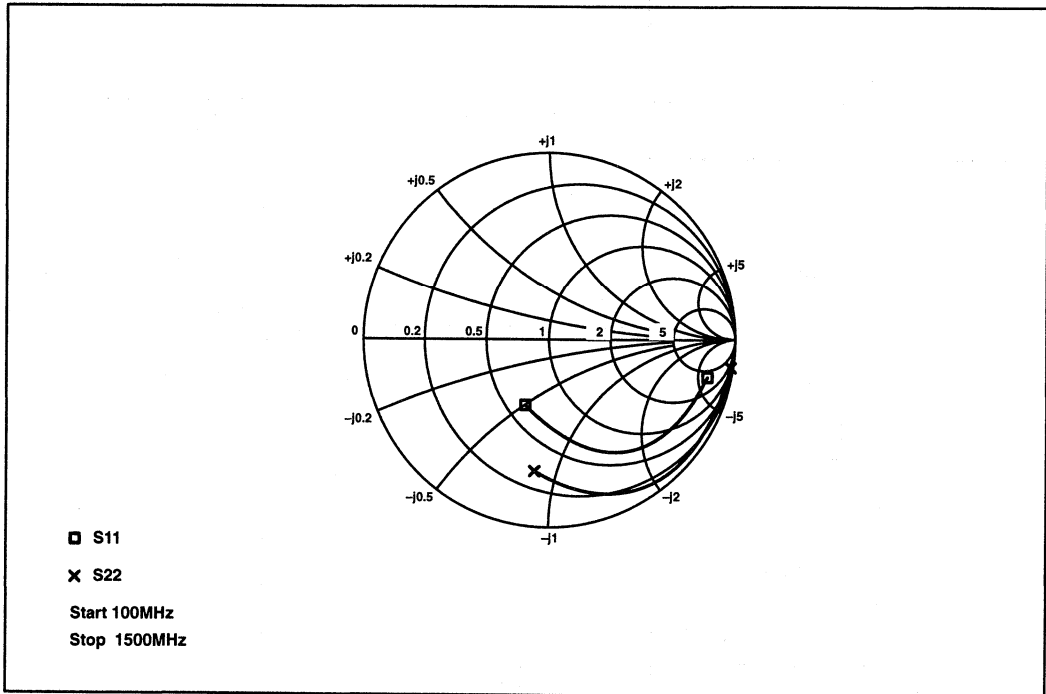


Fig. 3 Typical RF Amplifier S parameter and input/output impedance



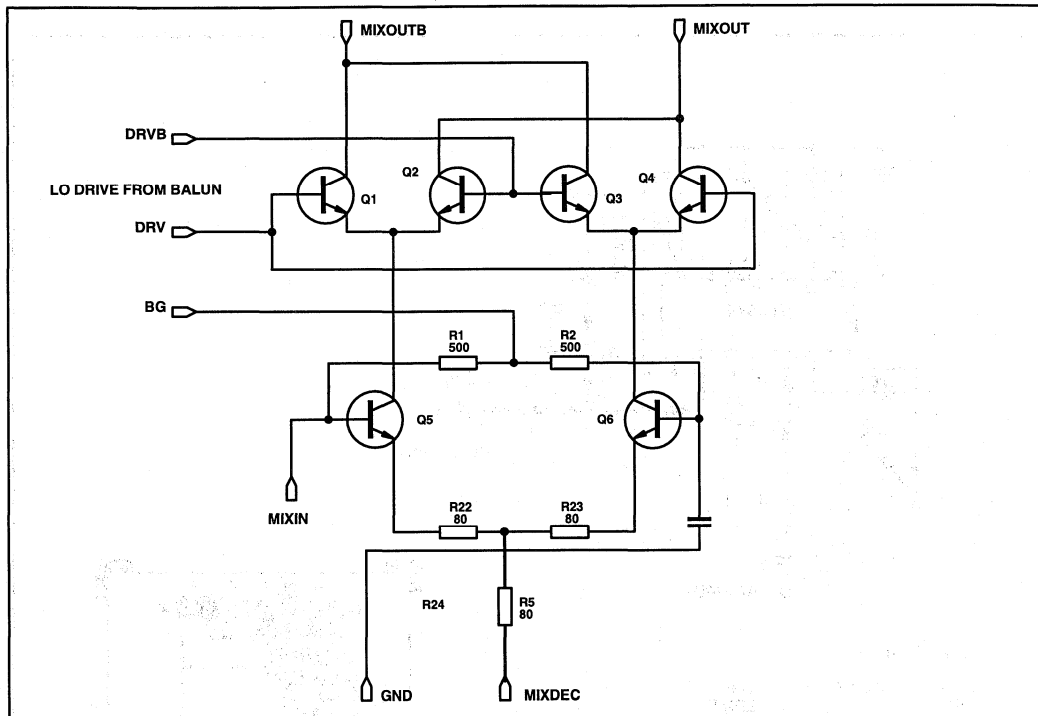


Fig. 4 Internal schematic of the mixer

$V_{CC}=5V$  Mixer current 4.4mA S22 is measured at either MIXOUT or MIXOUTB S11 is measured at MIXIN

FREQ— MHz	MAG [S11]	ANG [S11]	MAG [S22]	ANG [S22]
100.00	0.79	-6	1.00	-6
200.000	0.78	-13	0.99	-12
300.000	0.77	-20	0.99	-16
400.000	0.76	-28	0.97	-22
500.000	0.77	-34	0.96	-28
600.000	0.78	-41	0.97	-35
700.000	0.73	-50	0.94	-40
800.000	0.70	-58	0.91	-47
900.000	0.68	-67	0.88	-54
1000.00	0.64	-76	0.86	-60
1100.00	0.61	-86	0.83	-67
1200.00	0.58	-95	0.79	-74
1300.00	0.55	-105	0.75	-82
1400.00	0.51	-117	0.71	-89
1500.00	0.49	-129	0.68	-96

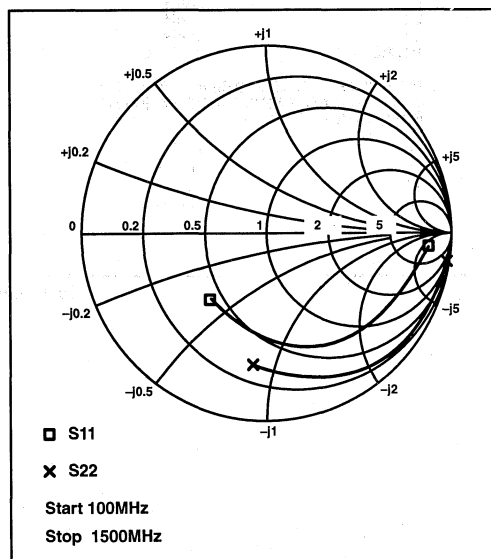


Fig. 5 Typical input and output impedance of SL6444 mixer (normalised to 50Ω)

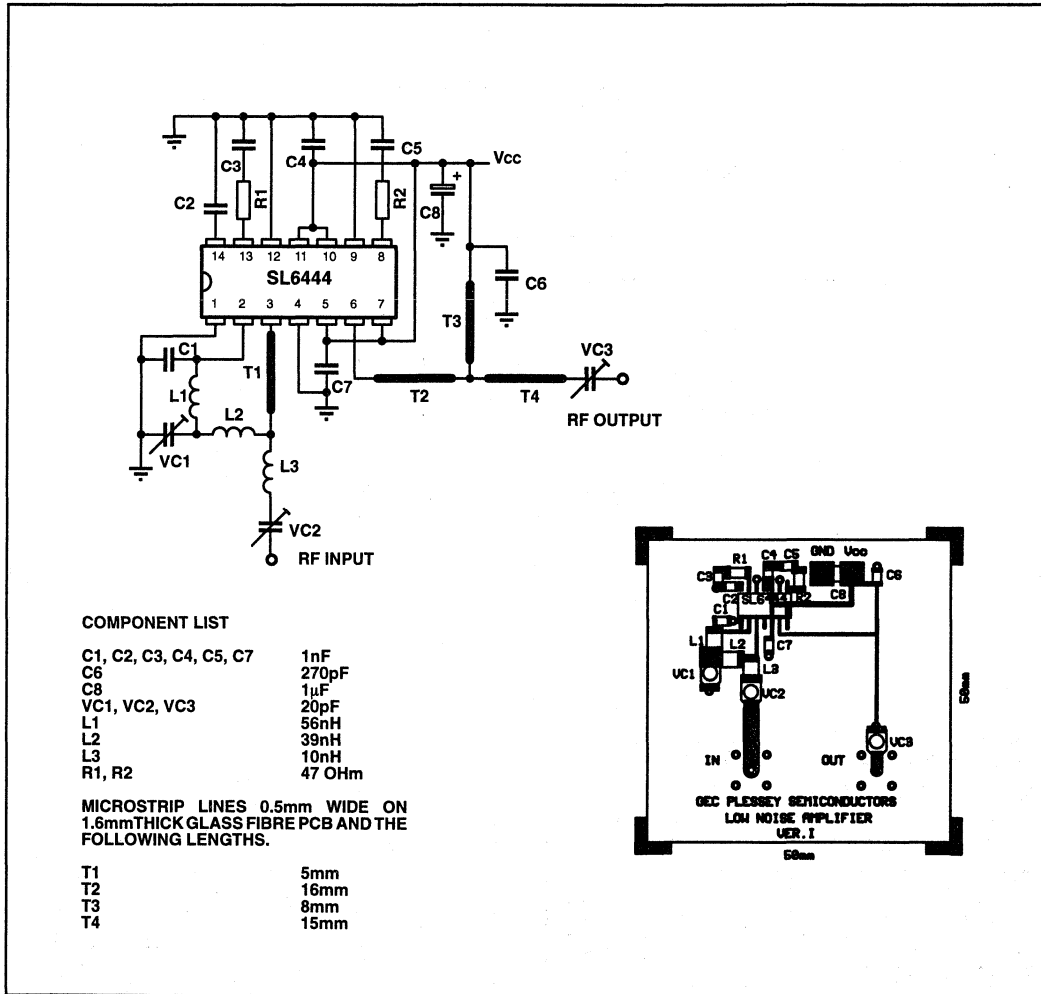


Fig. 6 Low noise amplifier

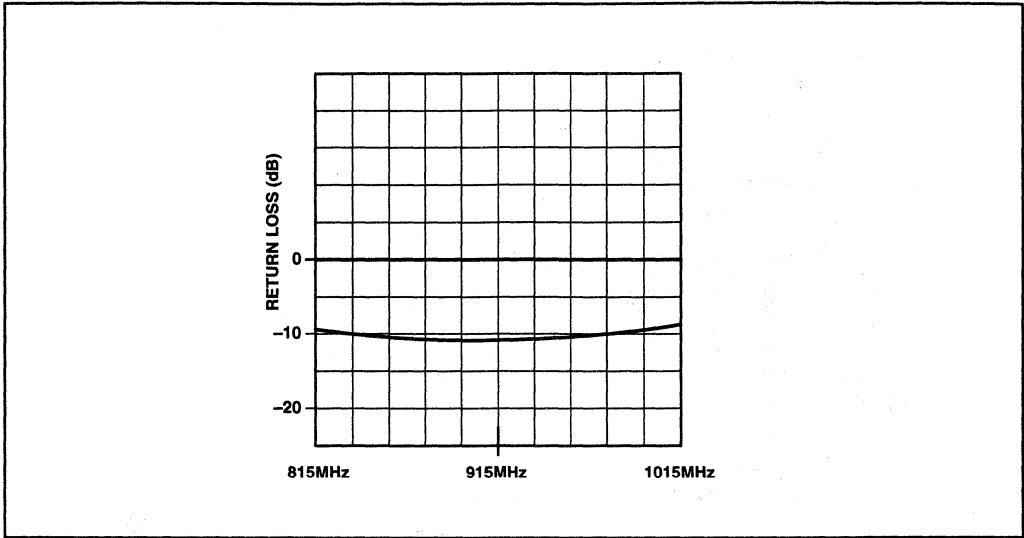


Fig. 7 Low noise amplifier input return loss

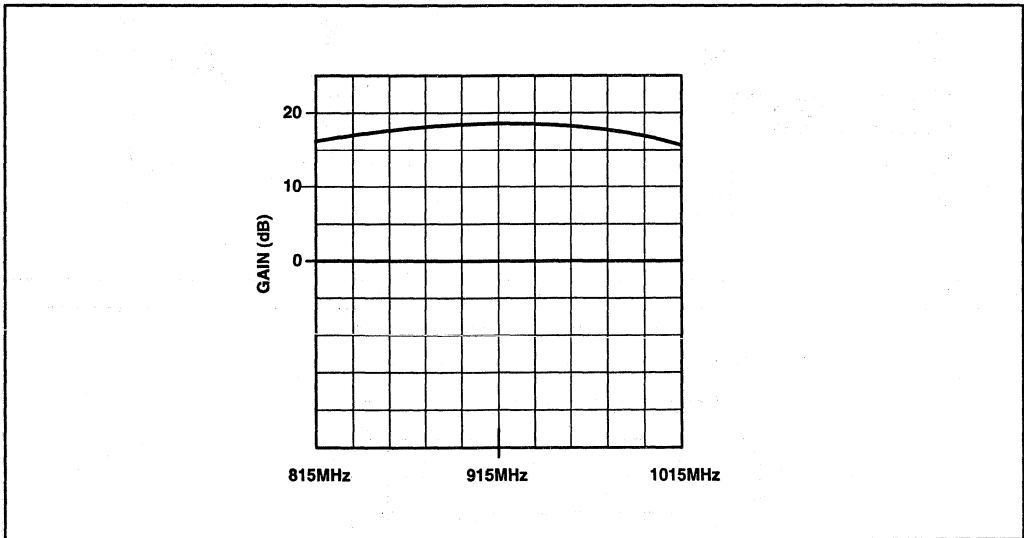


Fig. 8 Low noise amplifier gain profile

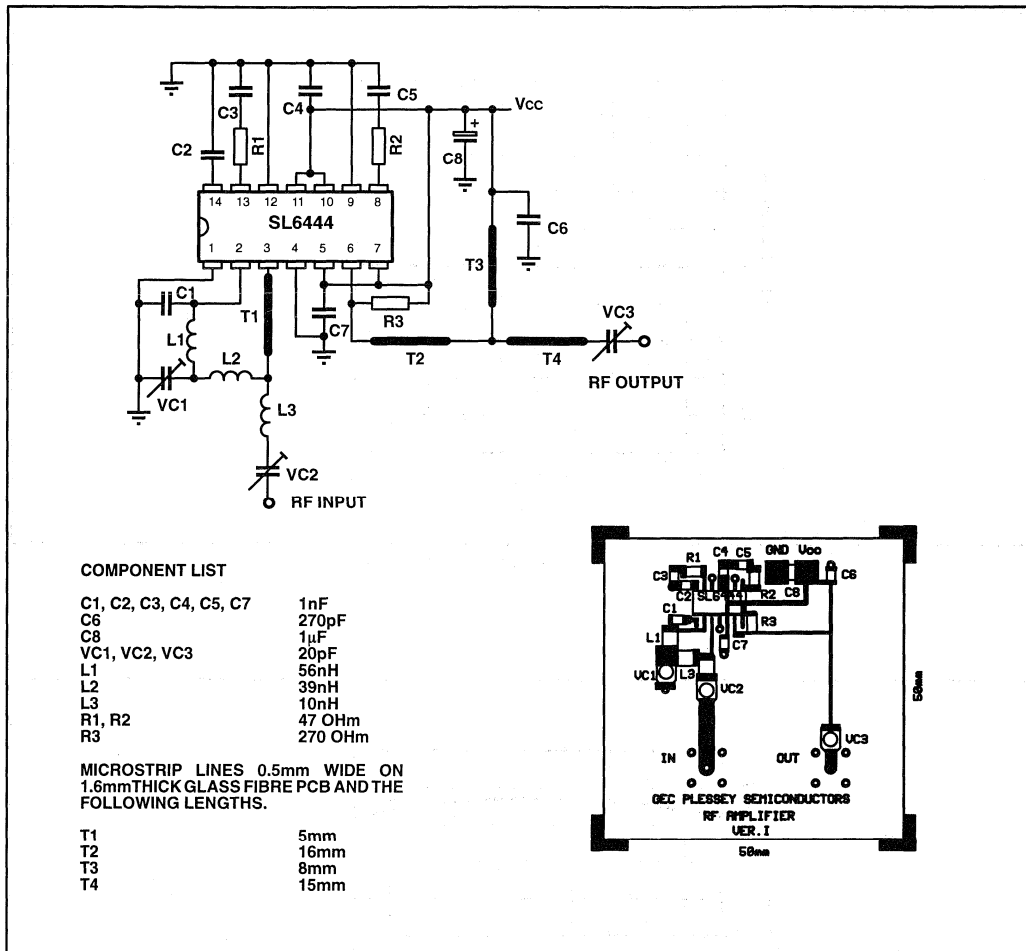


Fig. 9 R.F. amplifier

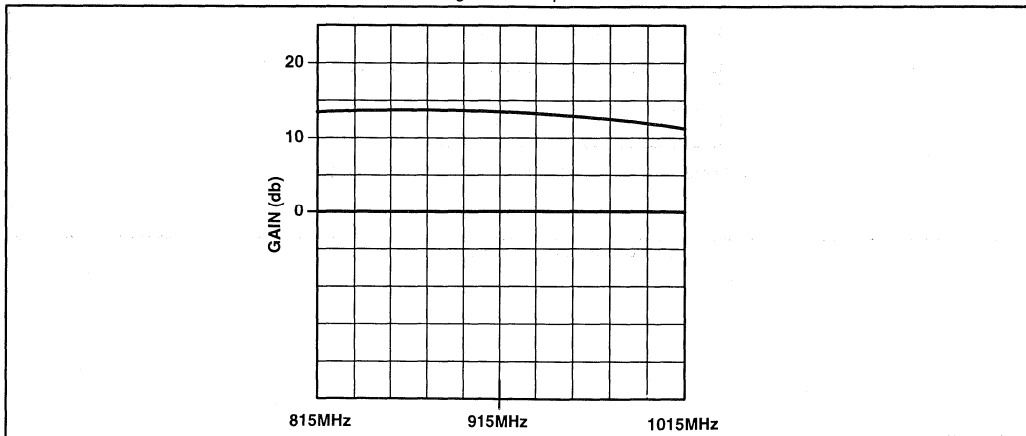


Fig. 10 Gain profile of the RF amplifier

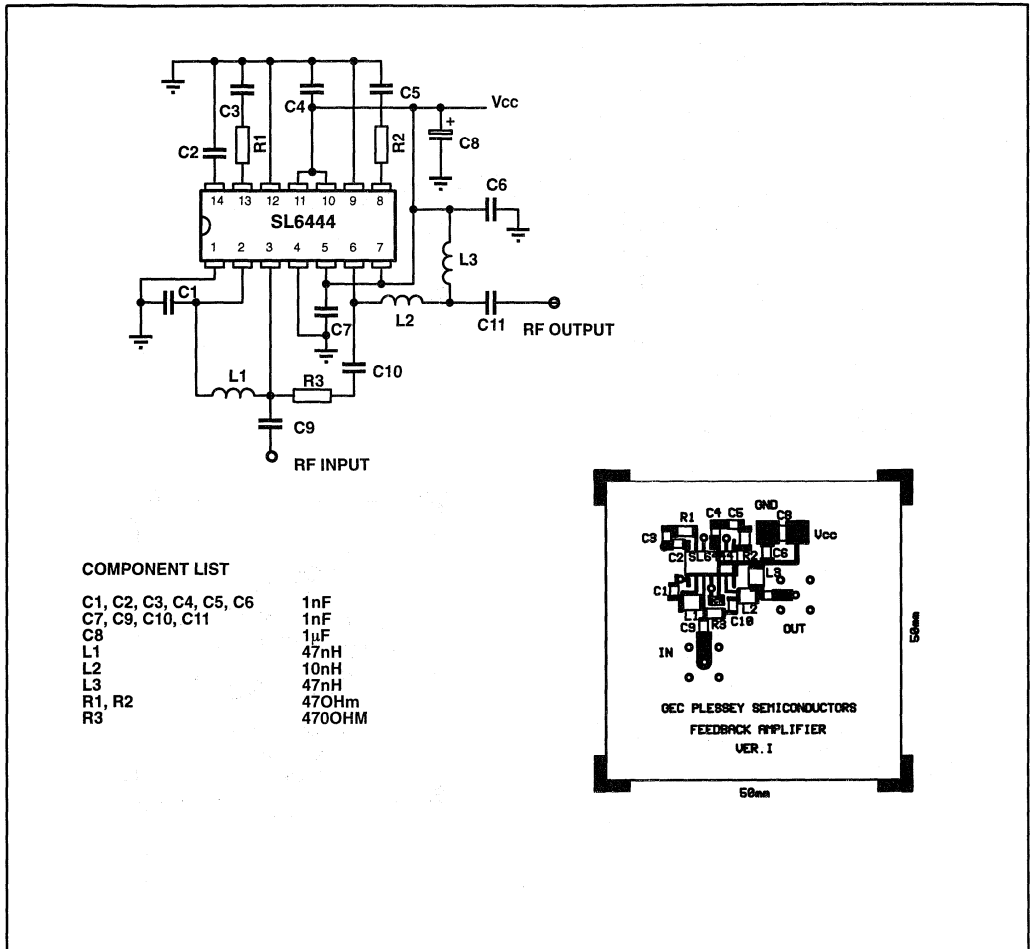


Fig. 11 Feedback amplifier

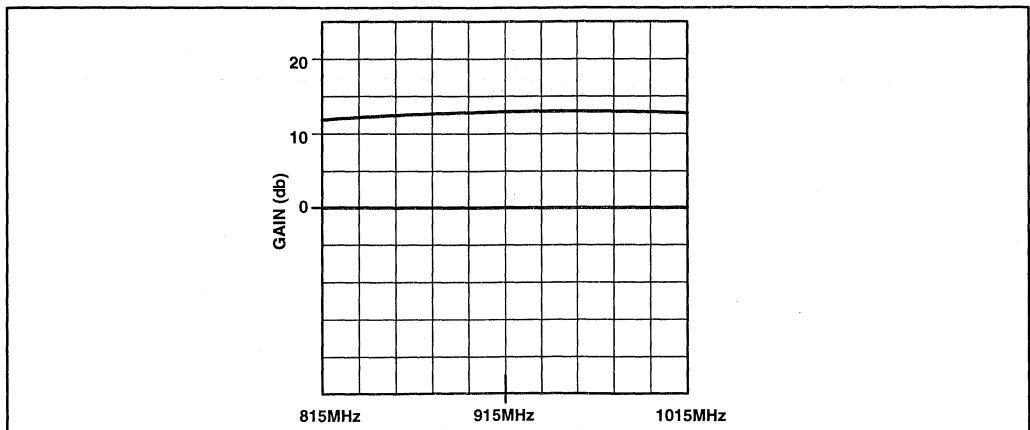


Fig. 12 Gain profile of the feedback amplifier

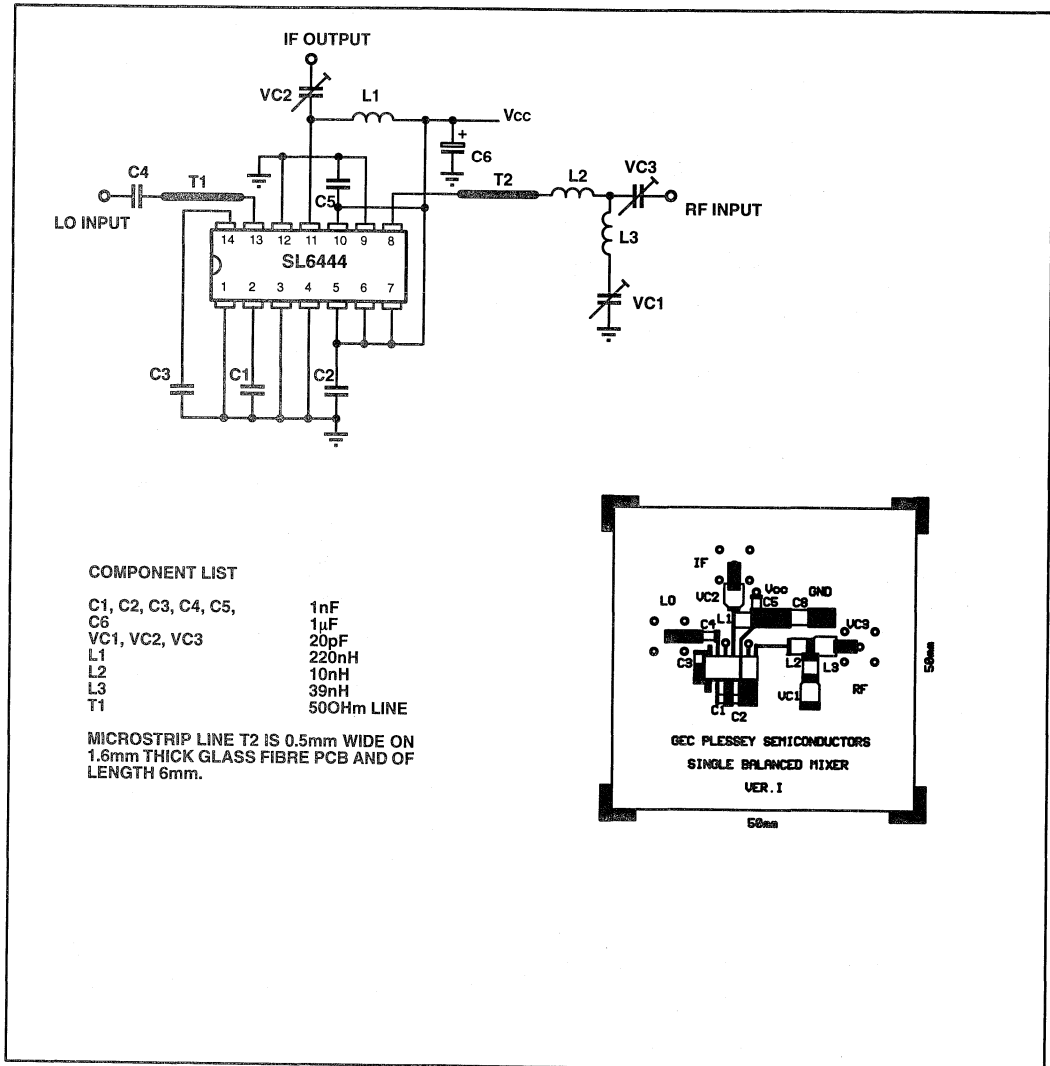


Fig. 13 Single balanced mixer

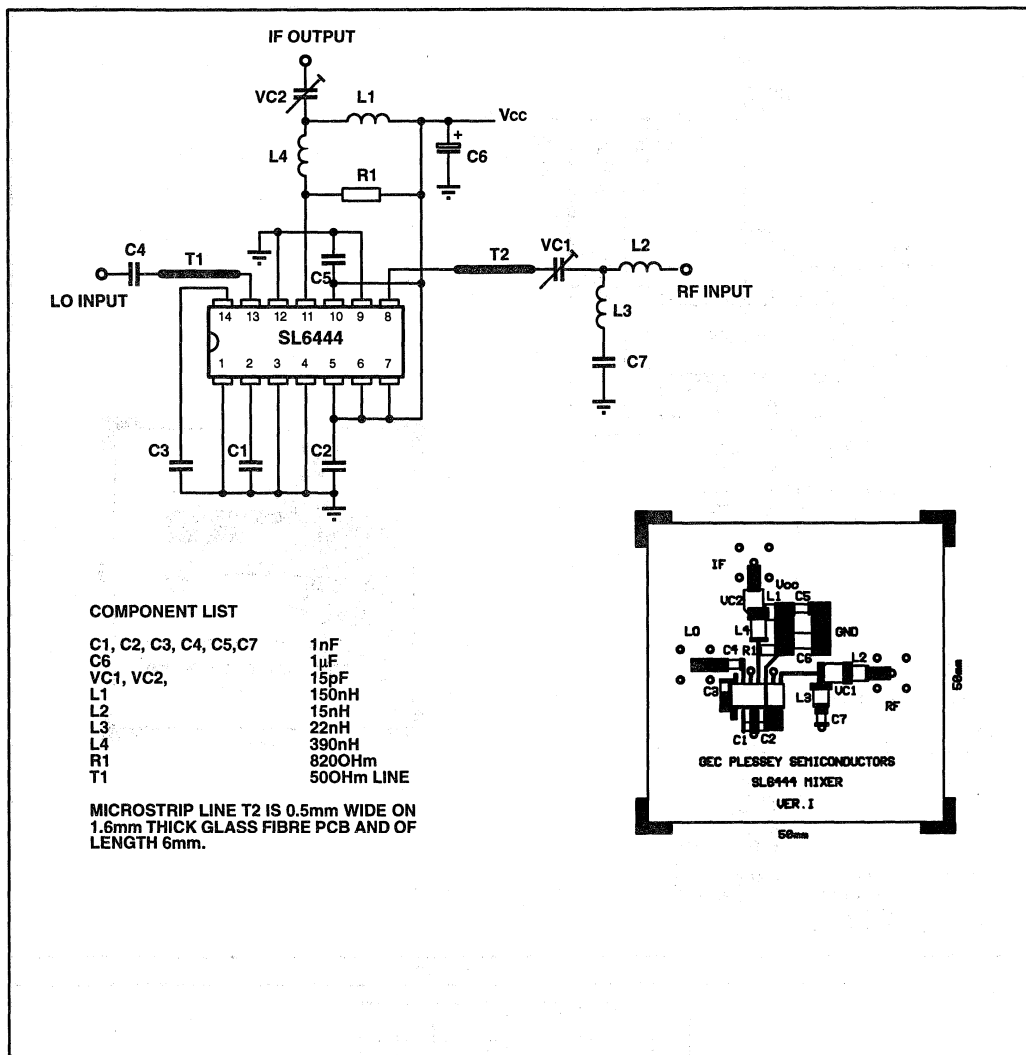


Fig. 14 Mixer

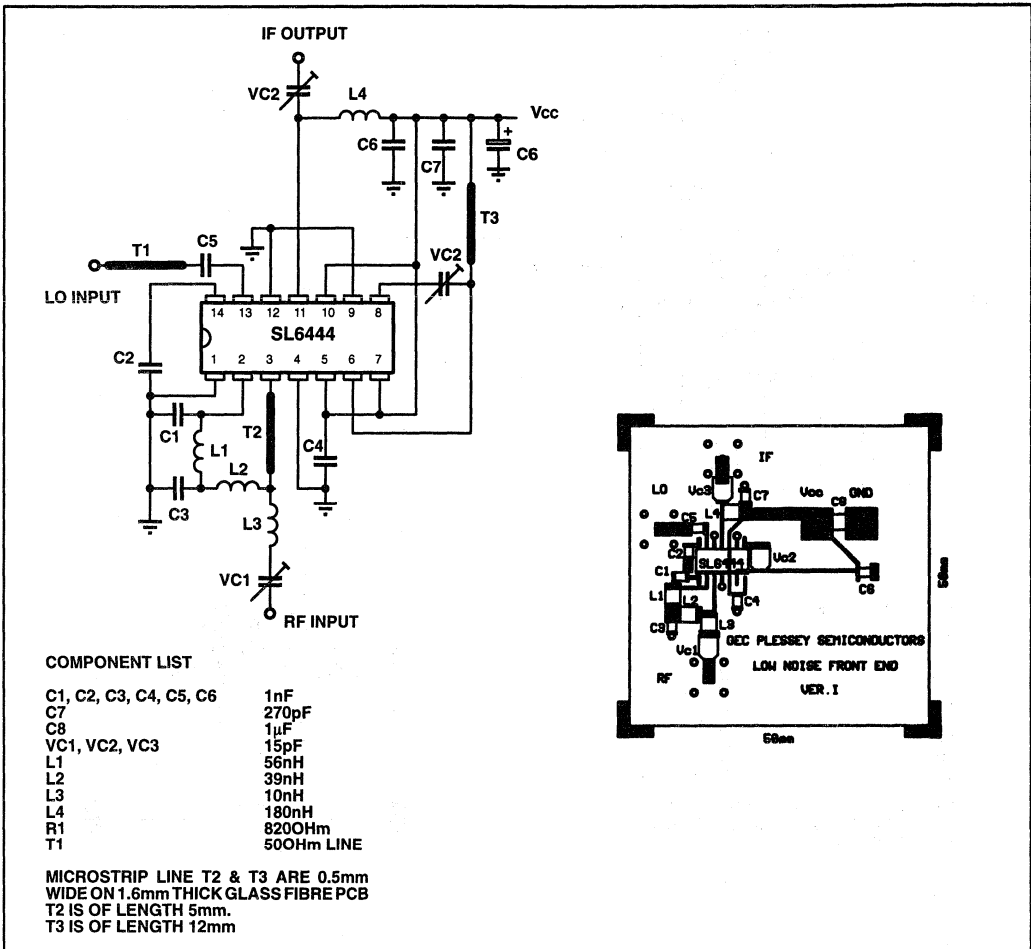


Fig. 15 Low noise front end.

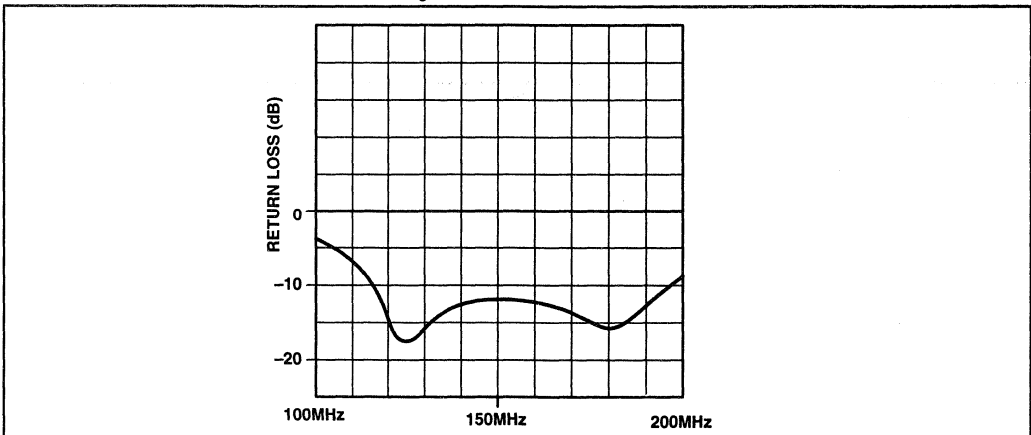


Fig. 16 I.F. output return loss.



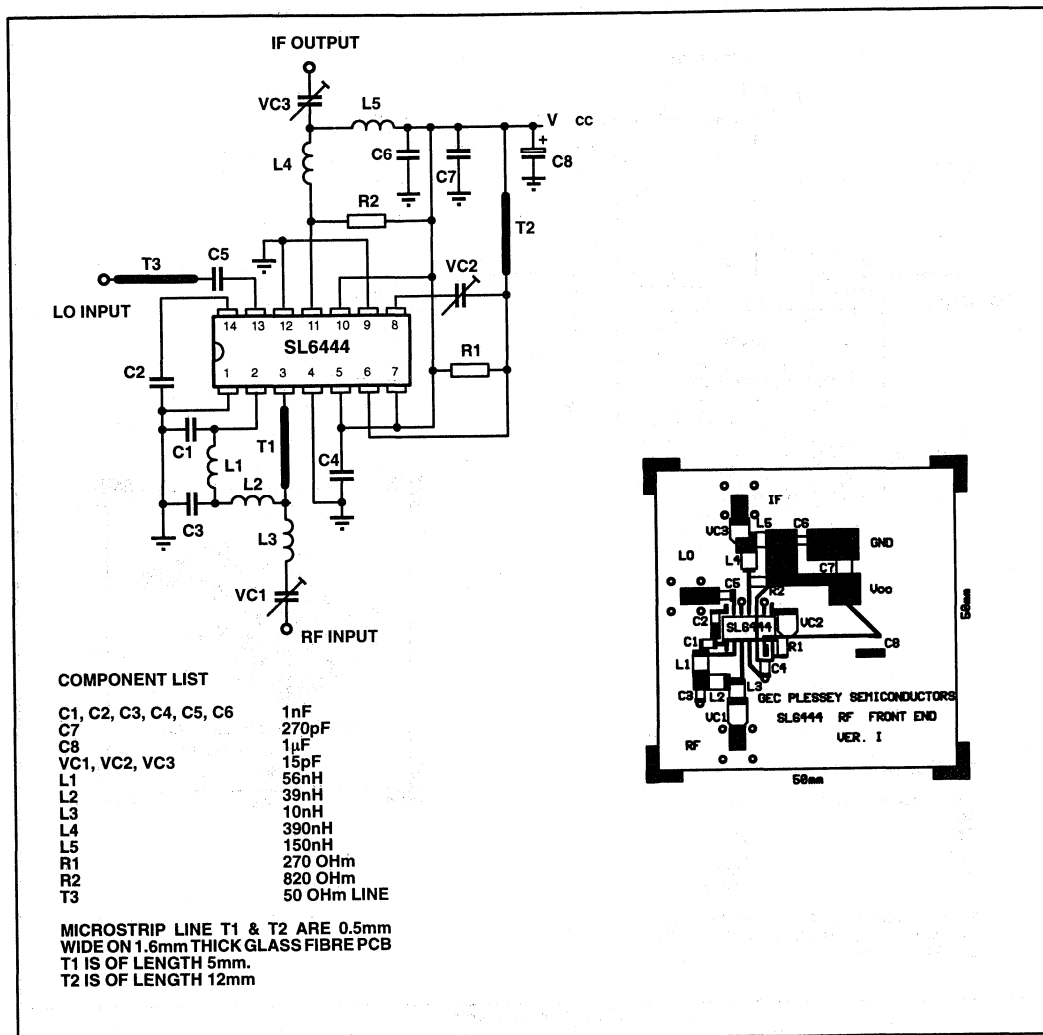


Fig. 17 RF front end.

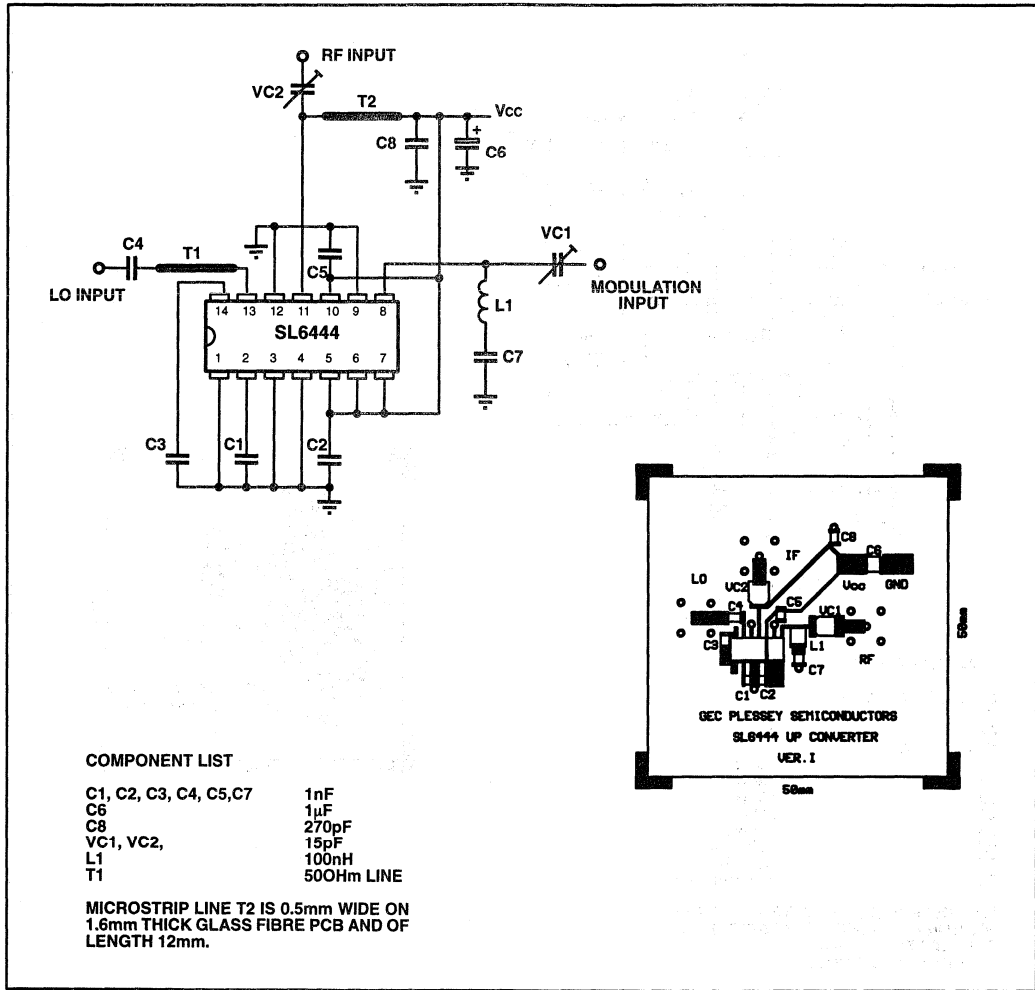


Fig. 18 Up converter

APPENDIX

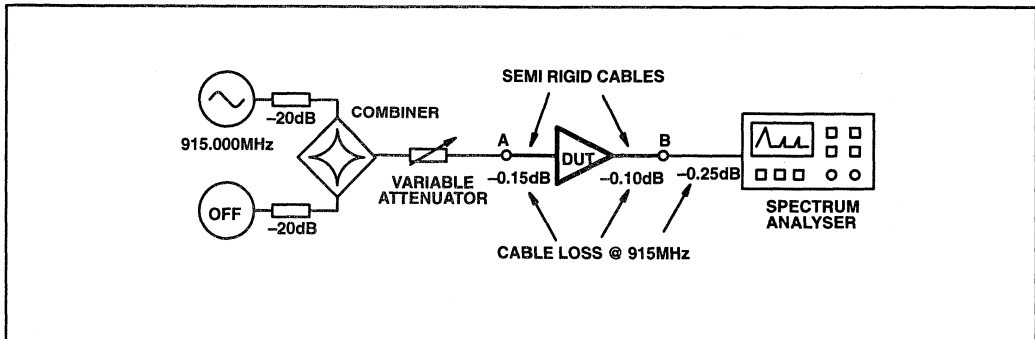


Fig. A1 RF amplifier forward gain

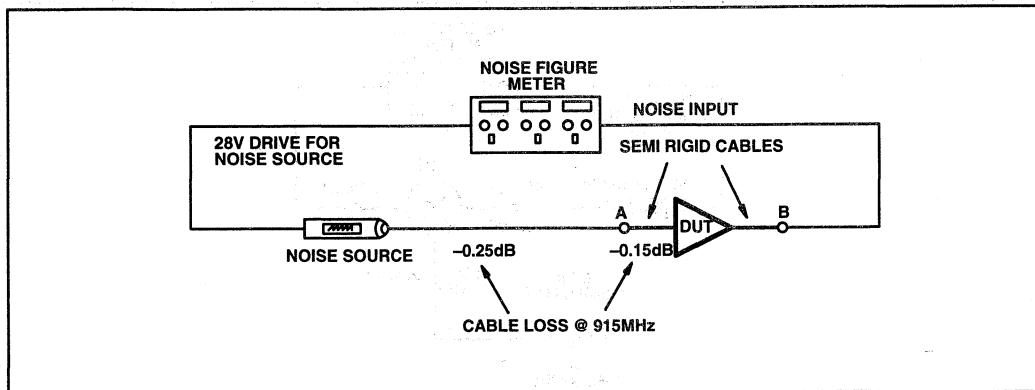


Fig. A2 RF amplifier noise figure

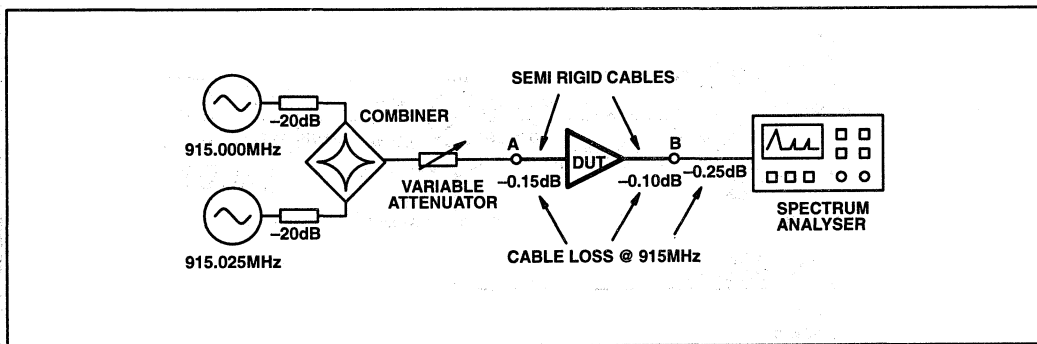


Fig. A3 RF amplifier third order intercept

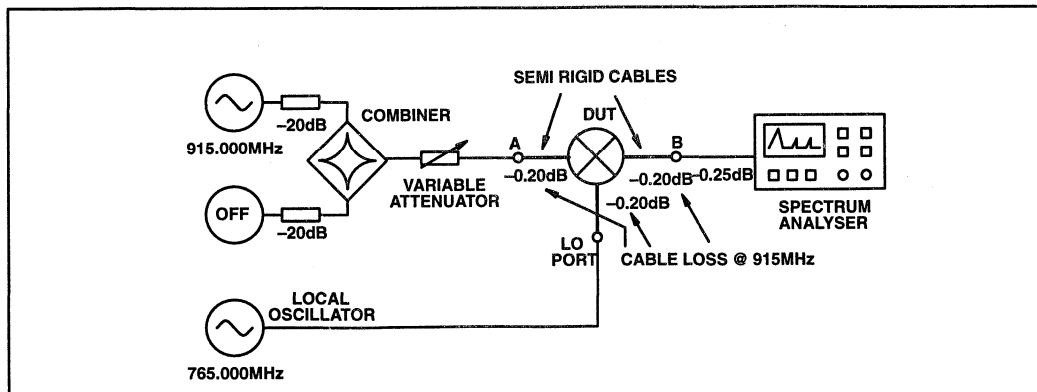


Fig. A4 Mixer conversion gain

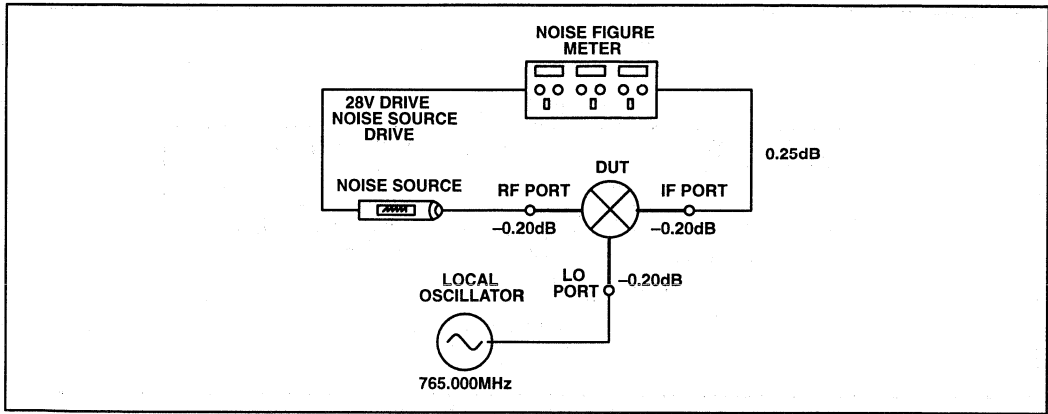


Fig. A5 Mixer noise figure

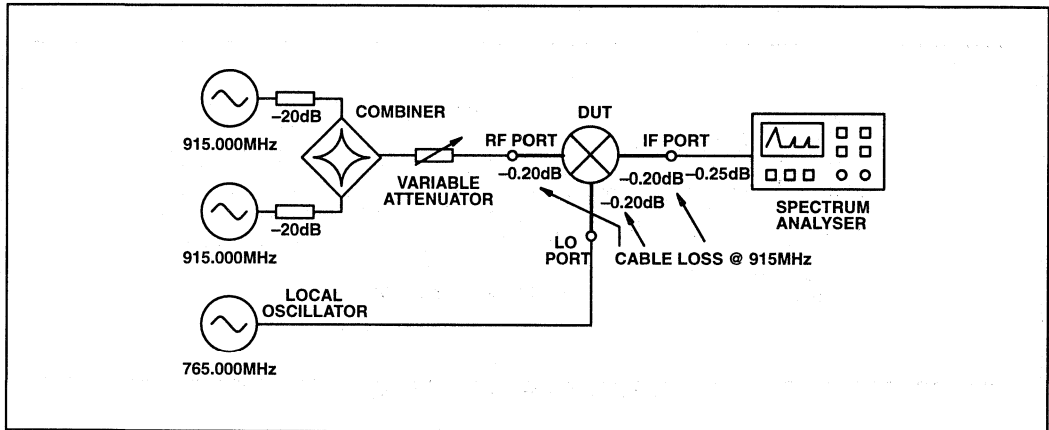


Fig. A6 Mixer output third order intercept

# SL6609

## ADVICE ON USING THE SL6609 DIRECT CONVERSION RECEIVER

(Supersedes September 1993 edition)

### Introduction

This application note outlines a basic circuit for the SL6609 Direct Conversion Pager Receiver for use at 153, 282MHz 350 and 450MHz with 4KHz deviation and at 1200bps data rate.

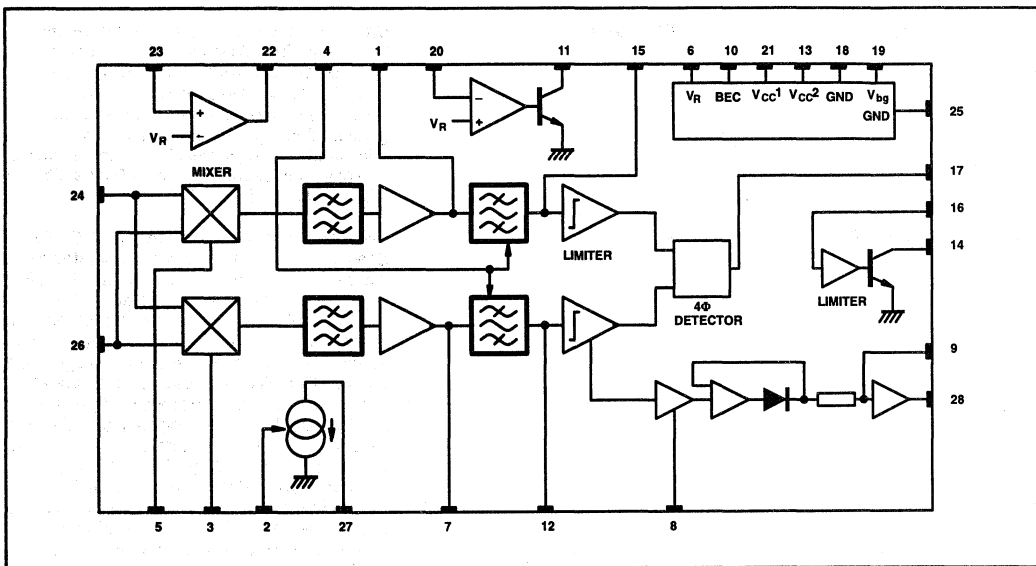


Fig. 1 SL6609 Internal block diagram

### SL6609 Pin Description

A schematic of the SL6609 is shown in Fig. 1. This shows the pin allocation and the connection with the internal structure of the device.

Pin No	Pin Name	Pin Description	Pin Details
1	TPX	Channel X test point	Channel X, Internal amplifier output/Gyrator filter input. The pin is used to measure the receiver signal level during receiver set-up. It may also be used in conjunction with pin 15 (TPLIMX) to measure the response of the Gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor. For details see "Set-up for Optimum Performance".
2	RFIADJ	Current Source ADJ	Pin 2 allows adjustment of the current source which is designed for use with the external RF amplifier. See "Circuit facilities"

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3	LOY	Mixer L.O. Input	The local oscillator signal is applied to pin 3 in phase quadrature to pin 5. For the phase quadrature circuit see "RF Amplifier and Local Oscillator". The L.O. input of the mixers require a bias path to $V_{CC1}$ (see R5 & R6 on the Applications Circuit)
4	GYRI	Gyrator Filter Adjust	The bandwidth of the on-chip gyrator filter can be adjusted using a resistor from pin4 to GND. For values see "Set-up for Optimum Performance".
5	LOX	Mixer L.O. Input	See pin 3.
6	VR	$V_R$	1V Internal reference voltage. It may be used for bias of external RF Amplifier and L.O. circuits. It is also a reference for pins no 1,7,8, and 9.
7	TPY	Channel Y.	Channel Y, Internal amplifier output/Gyrator filter input. This pin is used to measure the received signal level during receiver set-up. It may also be used in conjunction with pin 12 (TPLIMY) to measure the response of the gyrator filters. It can be used to add additional filtering in the channel in the form of an additional external capacitor. For details see "Set-up for Optimum Performance".
8	GTHADJ	Audio AGC Level ADJ.	Level adjustment for the external AGC drive. See Fig. 5. The voltage at pin 8 is dictated by an external resistor (R16 in Applications Circuit) and an internal current source driven by the wanted audio (baseband) signal level. With no signal input to the receiver, the output of current source 1 tends to zero and so the voltage at pin 8 is $V_R$ . This gives the result that the OP of current source 2 (pin 28) tends to $-0\mu A$ . (i.e. the AGC is disabled). With a signal incident on the receiver, current source 1 driving pin 8 is turned on and there is a voltage drop across the external resistor (R16). The value of the external resistor (R16) dictates the voltage drop and hence the sensitivity of the AGC circuit. For a value of the external resistor (R16). See Application circuit.
9	TCADJ	Audio AGC Time Constant	The attack (turn on) and decay (duration) times of the audio AGC are set by an RC network connected to pin 9. See Application Circuit for details.
10	BEC	Battery Economy	Battery economy facility allows the device to be powered down by pulling pin 10 to GND. If not required this should be connected to $V_{CC2}$ .
11	BATTFL	Low Battery Flag O.P	The battery flag is the output of an on-chip comparator with $V_R$ as a reference voltage. When $V_{IN}$ (pin20) > $V_R$ , Battery Flag O/P is Low. BATTFL is an open collector output.
12	TPLIMY	Y Gyrator Filter Output	See pin7. Pin 12 provides a monitor of the gyrator filter output of channel Y, to enable the response of the filter to be accurately measured and adjusted using pin 4. For details refer to "Set-up for Optimum Performance".
13	Vcc2	Vcc2	$V_{CC2}$ supply. This requires adequate audio decoupling to GND. If a DC-DC converter is used to generate this voltage care must be taken to prevent power supply noise reducing the sensitivity of the device.

14	DATAOP	Data Output	Open collector data output. This requires a pull-up resistor to a suitable voltage reference. e.g. $V_{CC2}$ .
15	TPLIMX	Test Point 4	See pin 1. Pin 15 provides a monitor of the gyrator filter output of channel X, to enable the response of the filter to be accurately measured and adjusted using pin 4. For details refer to "Set-up for Optimum Performance".
16	BRF2	Data Buffer Input	Input to the data limiter. This pin is normally connected directly to pin 17.
17	BRF1	Phase Detector Output	Output of the phase detector. For optimum performance a Bit Rate filter can be applied to this pin. This is achieved by applying a capacitor between pin 17 and GND. The value of this capacitor is dependent on the data rate. For the value of this capacitor see "Set-up for Optimum Performance".
18	DIGGND	Digital GND	This is the ground for the digital circuits in the receiver.
19	VBG	$V_{BANDGAP}$	Bandgap voltage reference (1.2V). This may be used for bias of an external RF amplifier. See Application Circuit Requirements for details.
20	VBATT	Battery Flag Input	If a 1V threshold is required, connect to pin 21, ( $V_{CC1}$ ). Alternative thresholds may be determined using an external potential divider. See Application Circuit requirements for details.
21	Vcc1	$V_{CC1}$	$V_{CC1}$ supply. This requires adequate Audio and RF decoupling if the device sensitivity is to be achieved.
22	REGCNT	Voltage Regulator Control OP	1V on chip voltage regulator output. Used to drive a suitable PNP transistor. See "Set-up for Optimum Performance". For stability purposes a capacitor should be applied between pin 22 and pin 23. The regulator is only specified for $V_{CC1} \geq 1.1V$ .
23	VREG	Voltage Regulator Sense	This should be connected to the load of the regulator. If the regulator is not required, and no active components are connected to pin 22 and pin 23, then pin 23 should be connected to $V_{CC2}$ .
24	MIXB	Mixer RF Input	Input to the device from an external RF amplifier. The signal should be applied differentially between pin 24 and pin 26. The differential signal to the mixers may be DC coupled if no DC voltage is applied, otherwise AC coupling should be used.
25	GND	Receiver ground	Ground for the RF receiver circuits.
26	MIXA	Mixer RF Input	Differential input from external RF amplifier. See pin 24.
27	IRFAMP	Current source	An on chip current source for use in RF amplifier designs. This allows the current in the RF amplifier to be independent of supply voltages. See Application Circuit Requirements for details. It is very important to use the current source with the RF amplifier. The current source incorporates an RF signal AGC. This ensures optimum operation of the device for a high input signal.

See Fig. 5. A current source controlled by the Audio signal level and the AGC threshold adjust (pin 8). The current source is intended to sink current from a PIN diode on the RF input and hence reduce the RF signal incident on the RF amplifier input.

### Application Circuit Requirements

The example application circuit is shown in Fig. 2. To achieve optimum performance of the device it is necessary to incorporate a Low Noise RF amplifier at the front end receiver. This is easily biased using the on-chip facilities provided.

The receiver also requires local oscillator at the wanted channel frequency .

### RF Amplifier and Local Oscillator Network

The design of the RF amplifier is simplified by the on-chip current source and the two voltage references.

A suitable circuit is shown in Fig. 3. The current through the load and hence the gain of the amplifier is controlled by the on chip current source. This ensures that the gain of the amplifier is independent of the supply voltages. Also, as  $V_D$  and  $V_{BG}$  are independent of supply voltage it ensures that the bias points of the transistors are also stable and independent of supply voltage, with each transistor simply biased via a series resistor to the appropriate voltage reference.

The RF amplifier current source (pin 27) may be adjusted with the use of an external resistor connected between pin 2 and a voltage reference or ground. For details see "RF Amplifier Current Source Adjustment". Also the RF amplifier current source forms the RF AGC by reducing the RF amplifier current if excessive signal is incident on the mixer inputs. It is very important to use the current source in the design of the RF amplifier. This ensures that the SL6609 will operate with a high level input signal.

The differential input required by the mixers is applied from the RF amplifier via a suitable transformer. This forms a tuned load with the variable capacitor (VC1). This load is tuned to the operating frequency of the device. The normal operating gain of the RF amplifier is also controlled by the load resistor (R13) in parallel with the transformer.

The input to the amplifier is a LC network (C26, L1 and C27) designed for optimum noise figure of the RF amplifier to give best overall device sensitivity.

For optimum sensitivity, adjacent channel and third order intermodulation performance refer to "Set-up for Optimum Performance" for the gain distribution requirements of the receiver chain.

The local oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their  $-3dB/45^\circ$  transfer characteristic at the local oscillator frequency, giving a full  $90^\circ$  phase differential between the LO ports of the device. (see fig. 4). Each LO port of the device also requires an equal level of drive from the oscillator. In this applications circuit the local oscillator is supplied by a signal generator with a source impedance of 50Ohms hence the total RC network (including mixer bias) is designed to have this input impedance.

N.B. All voltage and current sources used for bias of the RF amplifier and receiver mixers should be decoupled at RF and Audio frequencies using a suitable capacitor. RF decoupling should be as close as possible to the RF circuit.

### Regulator Requirements

The on-chip regulator must be used in conjunction with a suitable PNP transistor to achieve reliable regulation. As the transistor forms part of the regulator feedback loop, the transistor should exhibit the following characteristics:

$$H_{FE} \geq 100 \text{ for } V_{CE} \geq 0.1V$$

A suitable transistor is specified in the application circuit.

### RF and Audio decoupling Requirements

All voltages and references should be adequately decoupled at audio (baseband) frequencies. Also where a voltage or current supply or reference is used to bias the RF or LO circuits it is necessary to apply RF decoupling to the supply at the point of connection.

### Open Collector Outputs

The Data Output and the Battery Flag output are open collector and require a pull up resistor to a suitable voltage reference. Care must be taken to ensure that the pull-up resistor is adequate to supply sufficient current to the load.

## CIRCUIT FACILITIES

### Audio AGC Circuit

Fig. 5 shows the internal structure associated with the Audio AGC facility.

The Audio AGC facility consists of a current sink which is controlled by the audio (baseband) signal amplitude. It has three parameters that may be controlled by the user; the Attack (turn on) time, Decay (duration) time and threshold level.

#### Attack time

The Attack time is simply determined by the value of the external capacitor connected to pin9 (TCADJ). The external capacitor is in series with an internal 100kOhm resistor and the time constant of this circuit dictates the attack time of the AGC.

$$\text{i.e. } T_{\text{attack}} = 100k * C_{TC} \quad (* = \text{multiplied by})$$

#### Decay Time

The decay time is determined by the external resistor connected in parallel to the capacitor  $C_{TC}$ . The Decay time is simply  $T_{\text{decay}} = R_{\text{decay}} * C_{TC}$ .

#### Threshold level

When a large audio (baseband) signal is incident on the input to the AGC circuit, (see fig. 5) the variable current source is turned on. This causes a voltage drop across R16. The voltage potential between  $V_D$  and the voltage on pin 8 causes a current to flow in pin 9. This charges up  $C_{TC}$  through the 100K internal resistor. As the voltage across the capacitor increases, current source 2 is turned on and this sinks current from pin 28.

The current sink on pin28 can be used to drive the external AGC circuit by causing a Pin diode to conduct, reducing the signal to the RF amplifier.

The relationship between the incident audio signal and current source 1 is shown in Fig. 8. This can be used in conjunction with the R16 value to set the voltage at Pin 8 for any particular signal level.

The relationship between the voltage at Pin 8 and the output of current source 2 is given in Fig. 9.

Using both figures, the value of R16 can be selected to give the required output current at Pin 28 for any particular input signal level. Note however that the maximum Audio signal and



hence the Audio AGC current (pin 28) is limited by the internal RF AGC action to approximately 65µA.

#### Disabling the Audio AGC Circuits

The audio AGC may be simply disabled by connecting Pin 8 (GTHADJ) to  $V_r$ . Alternatively the audio AGC may be disabled by connecting Pin 28 (IAGCOUT) to  $V_{CC2}$  and connecting Pin 9 (TCADJ) directly to  $V_r$  (Pin 6). This would then allow the use of the voltage drop across R16, when connected to Pin 8, to be used as a RSSI (Received Signal Strength Indicator).

#### R.F. Current Source Adjustment.

With Pin 2 open circuit and with Pin 27 connected to a potential of 0.2V (i.e. the emitter of a transistor with the base voltage  $V_b = 1V$  (i.e.  $V_r$ )), the current is nominally set to give  $I_{RF} = 500\mu A$ .

The current source may be adjusted by connecting pin 2 via a suitable resistor to a voltage reference or ground.

The value of the resistor is determined by the required increase or decrease in  $I_{RF}$  from the nominal 500µA. (i.e. Pin 2 Open Circuit).

The nominal voltage of Pin 2 is 0.7V.

To decrease  $I_{RF}$ , connect Pin 2 to ground using a resistor R where;

$$R = \frac{0.7V}{\left(\frac{500\mu A - I_{req}}{5}\right)}$$

Where  $I_{req}$  = Required  $I_{RF}$

To increase  $I_{RF}$  connect Pin 2 to a voltage reference (e.g.  $V_{bg}$ ) using a resistor R where;

$$R = \frac{V^* - 0.7V}{\left(\frac{I_{req} - 500\mu A}{5}\right)}$$

Where  $I_{req}$  = Required  $I_{RF}$   
and  $V^*$  = Voltage reference used.

#### Notes

- $V_{bg}$  should not be used to sink current
- The on-chip voltage Reference  $V_r$  should not be used as a reference for Pin 2 as it is not capable of sourcing the required current.

#### On Chip Voltage References.

The on-chip voltage reference  $V_{bg}$  (1.2V) may be used to bias an external RF amplifier and as a reference for the on-chip RF AGC (see Pin 2).  $V_{bg}$  can source a maximum current TBD (200µA preliminary).  $V_{bg}$  should not be used to sink current.

The on-chip voltage reference  $V_r$  (1.0V) may be used to bias an external RF amplifier and as a reference for Pins 1, 7, 8 and 9.  $V_r$  can source or sink a maximum current of 10µA.

#### Battery Flag Input

The battery flag threshold may be simply increased by using a suitable potential divider so that at the required battery threshold voltage, the voltage at Pin 20 (VBATT) is 1V

#### Set-up for Optimum Performance

To obtain optimum receiver sensitivity it is necessary to have a Low Noise RF Amplifier at the front end of the receiver, (see "RF Amplifier and Local Oscillator"). However to achieve optimum Third Order Intermod rejection it is essential to ensure that the amplifier gain is not greater than the value necessary to achieve good sensitivity. Similarly to achieve

optimum Adjacent Channel rejection it is necessary to limit the internal gain of the device to that required to obtain sensitivity. Increasing the internal or the RF Amplifier gain beyond these points will degrade the receiver performance.

The procedure outlined here represents a method of obtaining optimum performance under the following operating conditions:

Frequency of Operation	282MHz
Local Oscillator Input Power	-15dBm (50Ohm source impedance)
Power Supply $V_{CC1}$	1.3V
Power Supply $V_{CC2}$	2.7V
Nominal Gytrator Pin4	100kOhm
R 1	Open Circuit
R8	Open Circuit
C1-C7	1nF

If the proposed frequency of operation is different to that stated above, the signal levels stated should be used as a guide to obtaining the optimum gain distribution within the receiver and RF amplifier.

N.B. The following set up procedure was undertaken using the RF Amplifier specified in Fig. 2 and should only be used as guidance if alternative RF amplifiers are proposed.

Note. Having obtained the component values for optimum performance for a specified RF amplifier, circuit layout, and operating conditions then provided the RF amplifier design is not device dependent, it should not be necessary to undertake the set-up procedure for each individual circuit.

#### Set-up Procedure

a) Apply a signal with a frequency of LO +4kHz, -73dBm to the input of the RF amplifier.

b) Monitor test point TPX (pin 1) with an oscilloscope. Determine that the signal is at a frequency of 4kHz. Adjust LO or RF frequency to achieve this. Adjust VC1 on the RF amplifier load until the 4kHz signal level is maximum. (This should be >200mV pk-pk).

N.B. If the level of the signal is above 260mV pk-pk the signal will not be sinusoidal due to the saturation of the receiver.

c) Using a parallel load resistor (R13) on the RF amplifier reduce the gain of the RF amplifier to obtain a level of 200mV ±10mV pk-pk at TPX. Ensure that the signal at TPY (pin 7) exhibits a similar gain.

d) Apply a capacitor between pin 16 and GND in accordance with the following table

Data Rate	Capacitor required
512	2nF
1200	1nF
2400	470pF

#### Fine adjustment of the Gytrator Filter

Due to the tolerance of the manufacturing process the gytrator response may vary by ±15% for a given value of resistor connected between pin 4 and GND. For accurate alignment the filter will require adjustment. This is simply achieved by undertaking the following procedure:

N.B. for the following levels to apply this procedure should be undertaken following "Set-up for Optimum Performance".

a) Set the input RF frequency to LO+4kHz, (No Modulation).

b) Monitor the signal at the test point TPX (pin 1). Check that the signal frequency is 4kHz. Adjust the LO or RF frequency to obtain this. Adjust the RF signal input level until

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a signal of 40mV pk-pk is measured.

c) Monitor the test point TPLIMX (pin 15) and note the pk-pk signal level. (this should be approximately 170mV pk-pk but not limiting).

d) Adjust the frequency of the RF signal generator until the signal level drops to 70.8% of the level noted in c (-3dBs).

e) Note the frequency of the RF signal generator. The difference between the LO frequency and the RF input frequency represents the filter 3dB response of the filter.

Using a 100kOhm resistor to set the Gyrator filters will give a nominal 3dB cut off 7.5kHz. Changing this resistor value causes a linear change in the frequency of the filter cutoff. e.g if a 100kOhm resistor results in a filter 3dB cut off 7.5kHz then a 136kOhm resistor will give a 5.5kHz 3dB cut off.

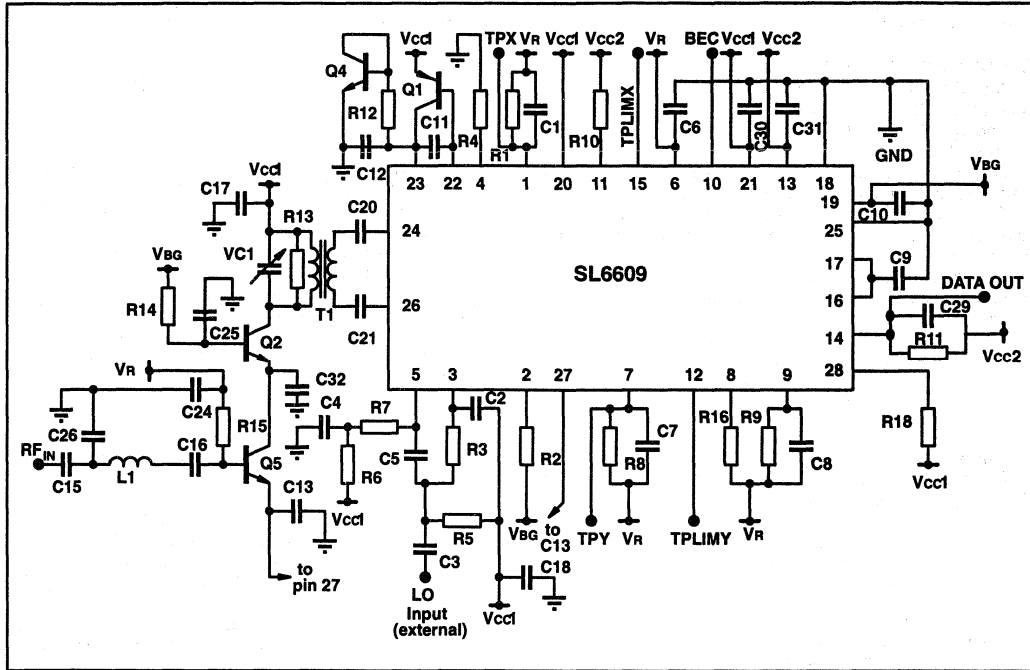


Fig. 2 Basic SL6609 Application circuit (282MHz receiver), showing RF amplifier with external rejected LO (no Audio AGC)

## Component Values (for general demonstration circuit (282MHz))

Resistors		Capacitors		Inductors	
R1	open circuit	C1	1n	L1	100n <sup>(4)</sup> (6)
R2	open circuit	C2	5p6 <sup>(6)</sup>	T1	1:1 30nH transformer
R3	100	C3	1n	e.g. Collcraft M1686-A	
R4	100k	C4	1n		
R5	100	C5	5p6 <sup>(6)</sup>		
R6	100	C6	2μ2		
R7	100	C7	1n		
R8	open circuit	C8	100n		
R9	220k	C9	2n <sup>(2)</sup>		
R10	1M	C10	2μ2		
R11	100k <sup>(5)</sup>	C11	100n		
R12	330 <sup>(3)</sup>	C12	1n		
R13	see note (1)	C13	1n		
R14	4k7	C14	not used		
R15	4k7	C15	1n		
R16	47k	C16	1n		
R17	not used	C17	1n		
R18	0R	C18	1n		
		C19	not used		
		C20	1n		
		C21	1n		
		C22	not used		
		C23	not used		
		C24	1n		
		C25	1n		
		C26	5p6 <sup>(4)</sup> (6)		
		C27	not used		
		C28	not used		
		C29	100p		
		C30	2μ2		
		C31	2μ2		
		C32	2p7		
		VC1	1-10p		

### Active Components

Q1	Zetex FM589
Q2	Philips BFT25A
Q3	Not Used
Q4	Philips BFT25A <sup>(3)</sup>
Q5	Philips BFT25A

Note:-

The Audio AGC components are not included in this component list.

**NOTES**

- (1) The value of this component is determined by the set up procedure. See "Set up for Optimum Performance".
- (2) The value of C9 is determined by the output data rate. Use 2nF for 512bps, 1nF for 1200bps and 470pF for 2400bps.
- (3) R12 and Q4 form a dummy load for the regulator. Permitted load currents for the regulator are 250 $\mu$ A to 3mA
- (4) L1, and C26 form the low noise matching network for the RF amplifier. The values given are for the RF amplifier specified in the Applications Circuit with no Audio AGC connected.
- (5) The value of R11 is dependent on the data output load. R11 should allow sufficient current to drive the data output load.
- (6) The values of these components are dependent on the frequency of operation.

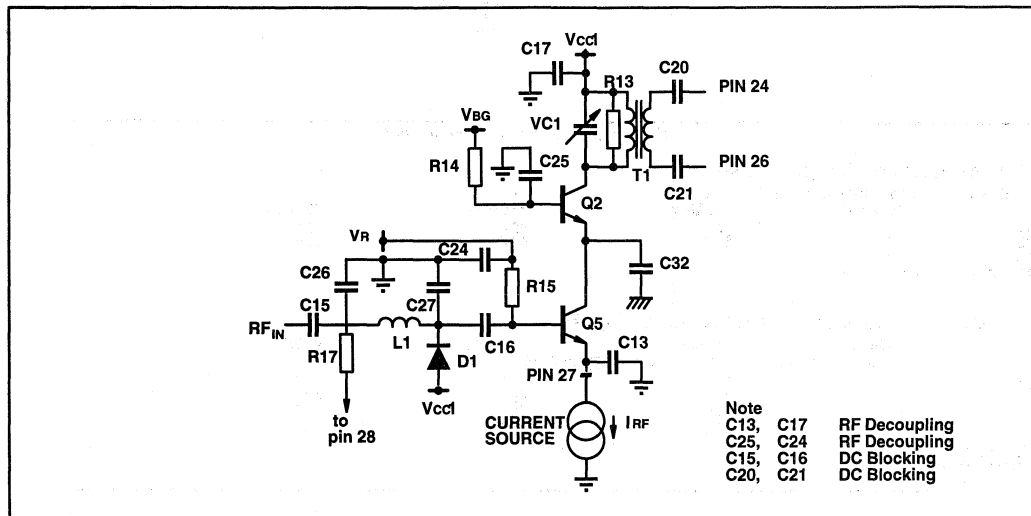


Fig. 3 RF amplifier

**RF Amplifier Component Values**

Resistors		Capacitors	
R14, R15	4K7	C13, C15	1nF
R13	see note 1	C16, C17	1nF
		C20, C21	1nF see note 2
		C24, C25	1nF

**Notes**

- (1) The value of R13 is determined by the set up procedure (See "Set up for optimum performance")
- (2) C20 and C22 are purely for demonstration purposes. Pin 24 and Pin 26 may be DC coupled provided that no DC voltage is applied to the mixer inputs.

**Frequency Dependant Components**

	153Mhz	280MHz	350MHz	450MHz
C26	not used	5p6	4p7	1-10pf
C27	3p3	not used	not used	not used
L1	180nH	100nH	82nH	39nH
C32	3p3	2p7	not used	not used
T1	100nH	30nH	30nH	16nH
VC1	Coilcraft N2261-A	Coilcraft M1686-A	Coilcraft M1686-A	Coilcraft Q4123-A
(See also LO drive Network)	1-10pF	1-10pF	1-5pF	1-3pF

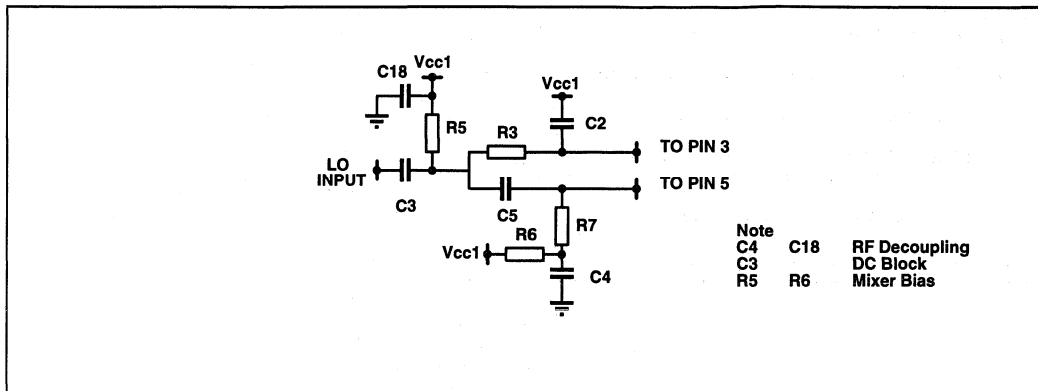


Fig. 4 Local oscillator drive network

**LO Drive Network Component Values**

50Ohm input impedance (External LO injection)

	153Mhz	280Mhz	350Mhz	450Mhz
C2	10p	5p6	4p7	3p3
C5	10p	5p6	4p7	3p9
C3, C4, C18 = 1n				
R3, R5, R6, R7 = 100Ohms.				

**Higher Input Impedance (crystal oscillator input)**

	153Mhz	280Mhz	350Mhz	450Mhz
C3	Set by load allowable on crystal oscillator (typical 4p7)			
C2	4p7	5p6	4p7	3p3
C5	4p7	5p6	4p7	3p7
R3	220	100	100	100
R7	220	100	100	100
R6, R7, = 1K				
C4, C18 = 1n				

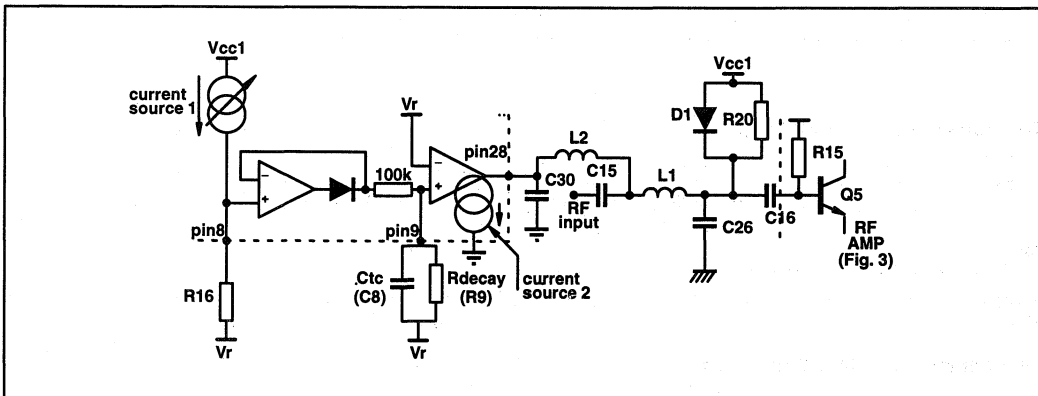


Fig. 5 AGC Schematic

**AGC Components Values (282MHz RF amplifier)**

R9	220K	C15	1n	L1	63n
R15	4K7	C16	1n	L2	220n
R16	see note	C26	5p6	D1	MA862 (Panasonic)
R20	47K	C30	1n	C8	see note

Note:  
R16 sets the gain (sensitivity) of the audio AGC. If R16 is increased then the audio AGC will become active for a lower wanted signal level. Increasing R16 can cause the audio AGC loop to become unstable. C8 should be increased to increase the turn on/off time to prevent oscillation occurring.

**Recommended Values**

R16 = 33K	R16 = 62K
C8 = 100nF	C8 = 470nF

Fig. 6 shows a typical response of the AGC with wanted and unwanted rejection level.  
If the AGC is required to become active earlier it is possible

to use the circuit shown in Fig. 7 to replace R16. However, it should be noted that the AGC has a fixed dynamic range.

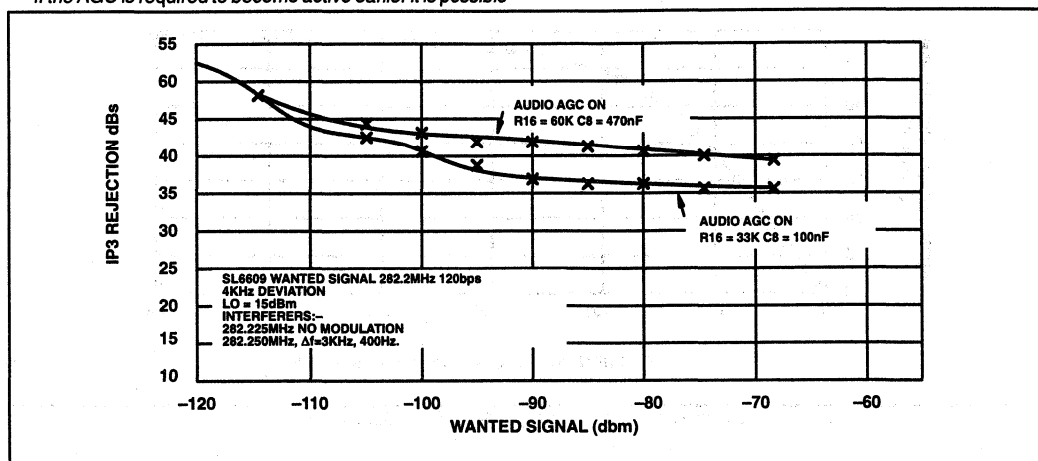


Fig. 6.

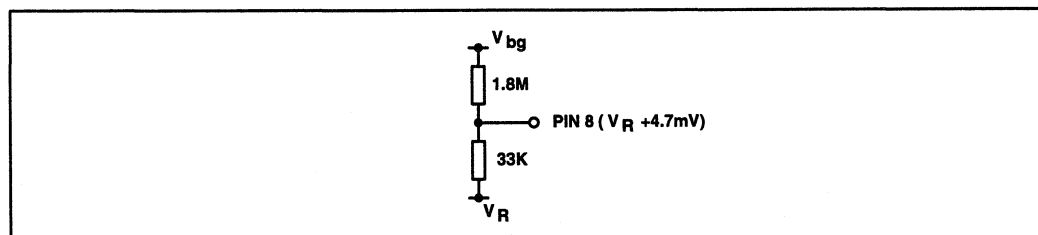


Fig. 7.

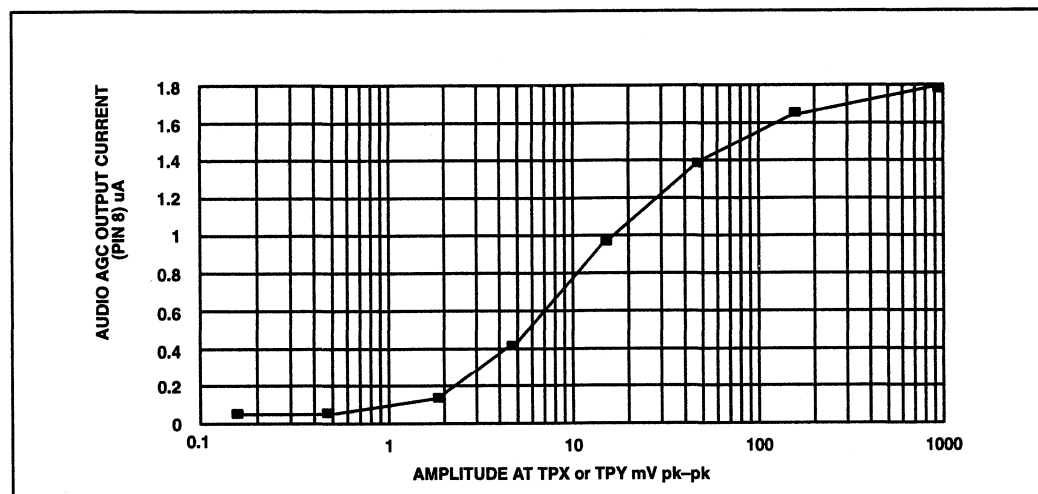


Fig. 8 RSSI Audio AGC vs Signal level at TPX or TPY

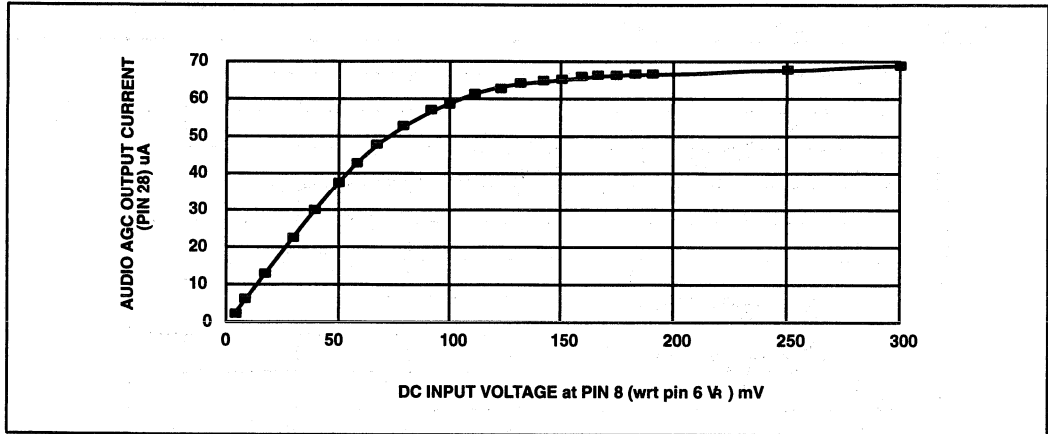


Fig.9 Audio Output Current at pin 28 vs DC Voltage at pin 8

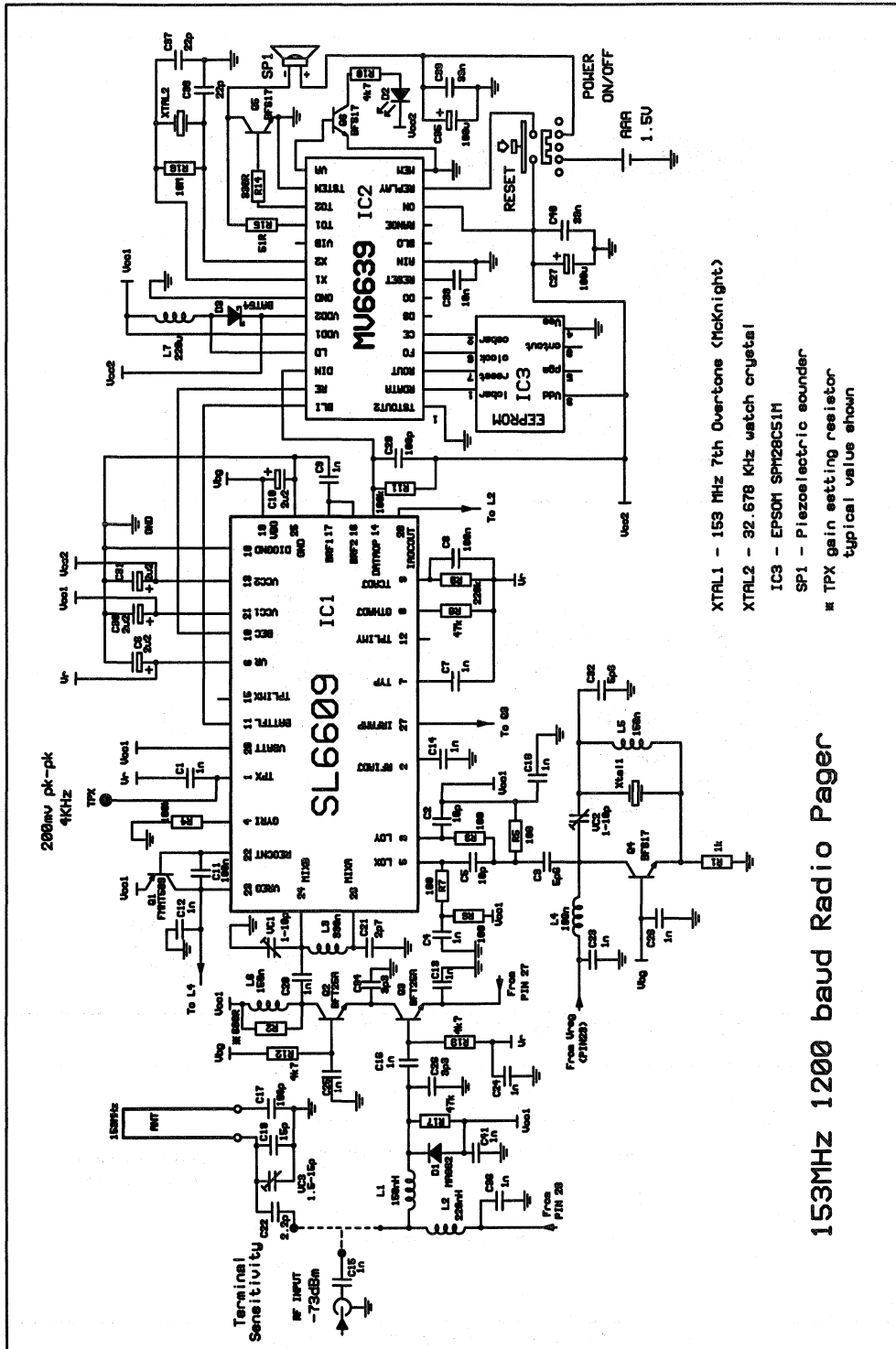


Fig.10 Circuit diagram

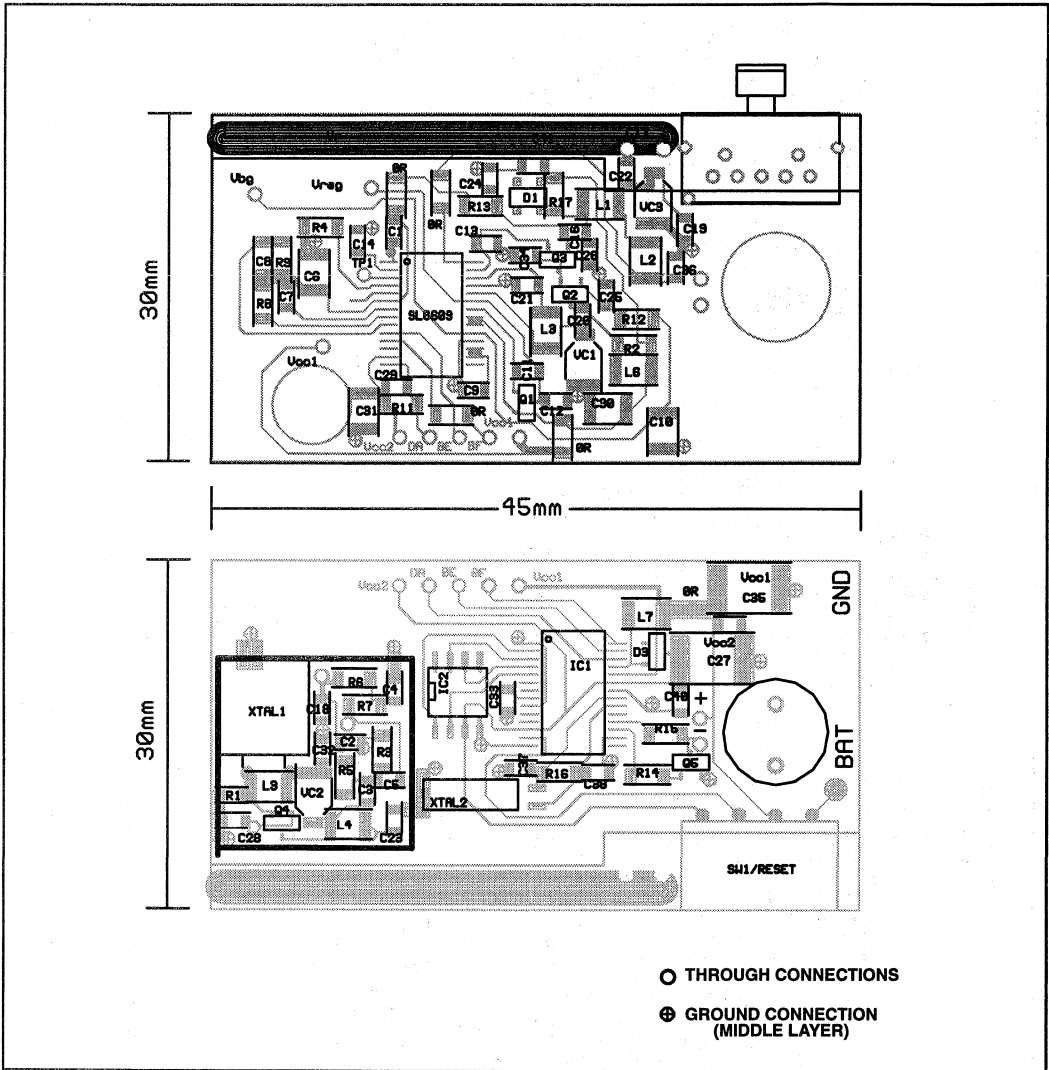


Fig. 11 Layout for box pager. Inc antenna (3 layers middle layer ground).

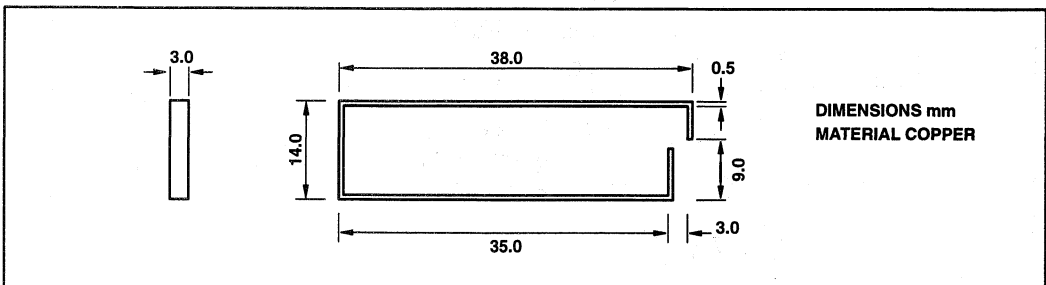


Fig. 12. 153MHz pager loop antenna (suitable for box pager)



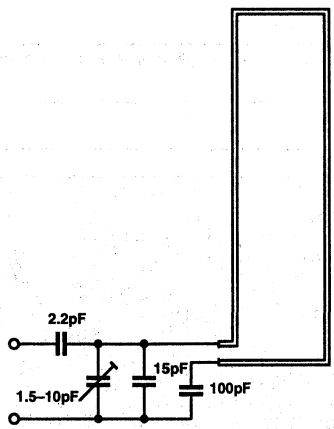
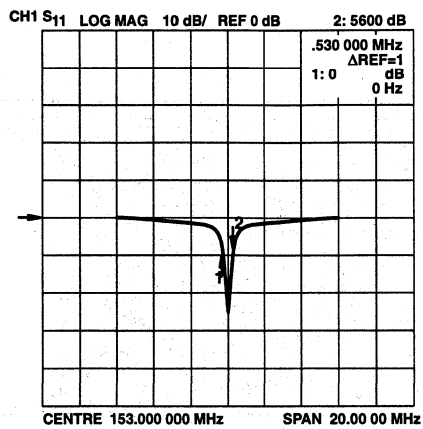


Fig. 13. Loop antenna matching circuit

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**A CREDIT CARD PAGER**

A credit card size pager can be produced using single sided 0.5mm duroid with the antenna printed directly on the circuit board.

N.B. the ground plane should be removed from behind the

antenna.

A ground plane is required behind all other circuit components.

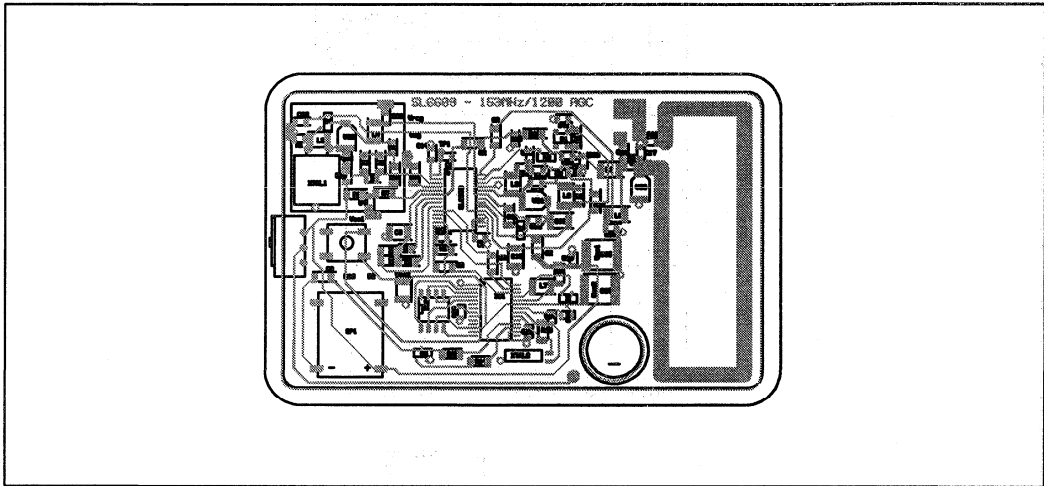


Fig. 14 Credit card pager (Actual size) 0.5mm duroid

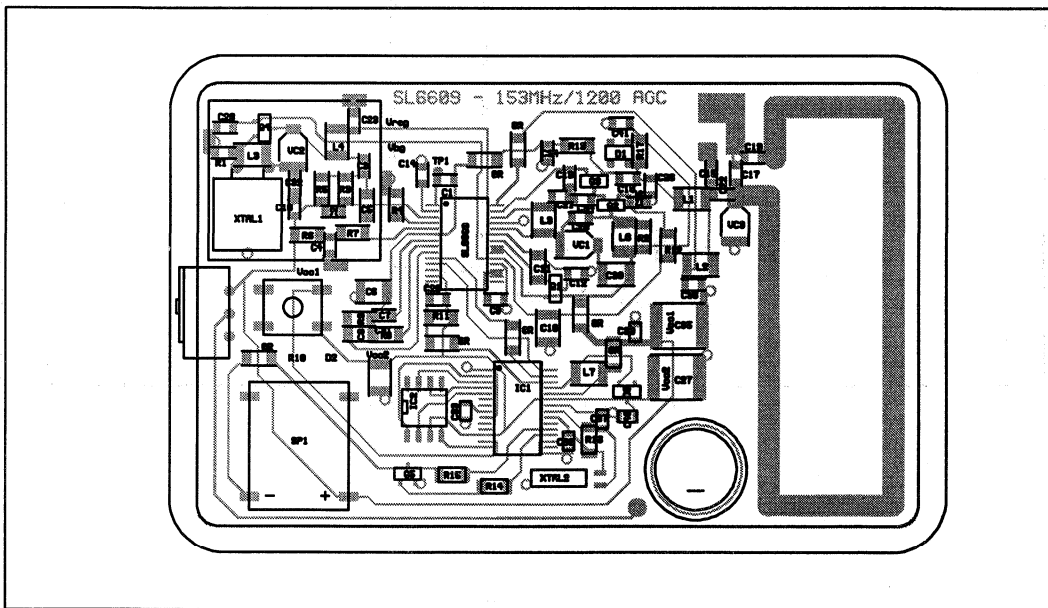


Fig. 15 Credit card pager

## GUIDANCE ON BOARD LAYOUT FOR A RADIO PAGER

It is important to adhere to several basic RF design rules when attempting to layout a radio pager. These rules are simple and may appear trivial, but if not adhered to will result in the performance of the radio pager not being as expected. At best this will result in a poorer performance, at worst it will prevent the circuit from operating at all. Sometimes poor layout will result in unexpected feedback in the circuit causing oscillation.

At RF frequencies printed circuit board pads and tracks may appear capacitive or inductive. If a track between two components is long and thin then it will appear as a series inductor and hence will become a part of the RF circuit. If a pad is too large then this may appear as a parallel capacitive element. This will also become part of the RF circuit. The general rule here is that all RF circuit components that are connected together should be as close together as possible and not separated by any large length of track.

All RF circuits should ideally be mounted on a single side with an earth plane on the opposite side of the board. This ensures that any electric field generated by the RF circuit is contained within the circuit and not radiated away to be picked up by other circuits. It also helps prevent the RF circuit from picking up other stray signals e.g the local oscillator. Different RF circuits within the same design should be kept away from each other to prevent any interaction between them. This is especially the case when both circuits are designed to operate at the same frequency as is the case with direct conversion receivers. A large ground plane also ensures that a good RF ground can be achieved anywhere within the circuit. This is important for achieving a good definition between the RF circuit and the DC circuit.

The position at which the RF circuit interfaces with the DC circuit should be well defined and decoupled to ensure these

points are RF ground e.g DC bias for the RF amplifier. This ensures that the DC bias circuit components do not become part of the RF circuit. In the case of the SL6609 circuit all of the 1nF capacitors connected to ground perform this function. It is important to ensure that the ground to which the decoupling capacitors are connected is a true RF ground and not just a DC ground. As stated this is usually achieved with the use of a ground plane. As this is normally a large area of conductor it ensures that the point at which the RF ground is required is not separated from the true ground by an inductive length of line.

RF circuits are made to respond to high frequencies. As fast data edges contain high frequency components, RF circuits should be kept away from data lines. In the case of the SL6609 the Data Output line to the decoder should not pass underneath any of the RF circuit components. This includes the device, the RF amplifier or the LO circuits.

If it is necessary to use a double sided design then the two sides of the boards should be isolated from each other with the use of a 3 layer board with middle layer used as the ground plane.

Fig.1 shows an example of a required circuit. Notice that this includes the DC circuit. The position at which the RF circuit is connected to the DC circuit is decoupled by a capacitor which provides a low impedance to ground at the frequency of operation. These capacitors are C4 and C3.

Fig.2 shows the correct layout for achieving the required RF circuit operation. Notice that the RF track lengths are short and the decoupling capacitors are connected directly to the ground plane. All DC grounds are connected through to the ground plane which is not shown.

Fig.3 shows a poor layout for the amplifier.

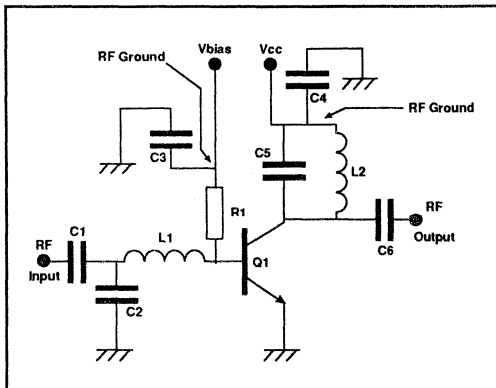


Fig.1 Required RF amplifier circuit

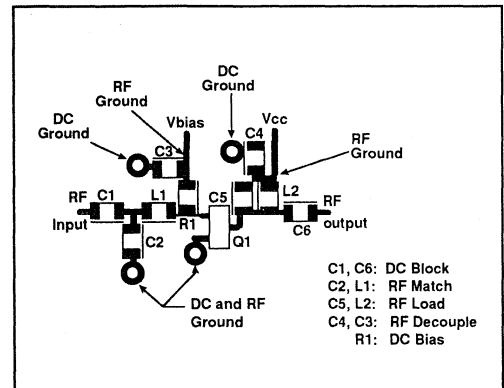


Fig.2 Good RF amplifier layout showing DC and RF grounds

- C1, C6: DC Block
- C2, L1: RF Match
- C5, L2: RF Load
- C4, C3: RF Decouple
- R1: DC Bias

Fig.4 shows the effect of poor layout of the circuit. The inductors ( $L^*$ ) will interact with the RF load, and RF match to cause a change in the amplifier characteristics. Also C3 and C4 are now not directly connected to the amplifier in the position required and hence part of the bias circuit is now incorporated into the RF circuit. This will also cause a change in the amplifier characteristics.

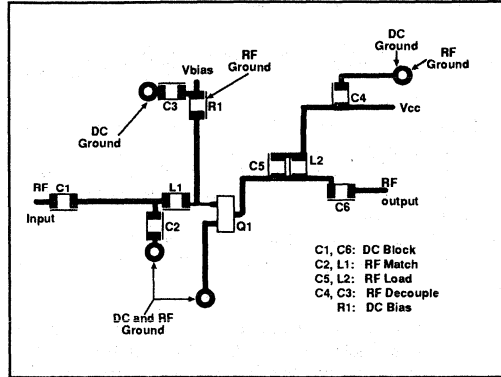


Fig.3 Poor RF amplifier layout showing DC and RF ground points

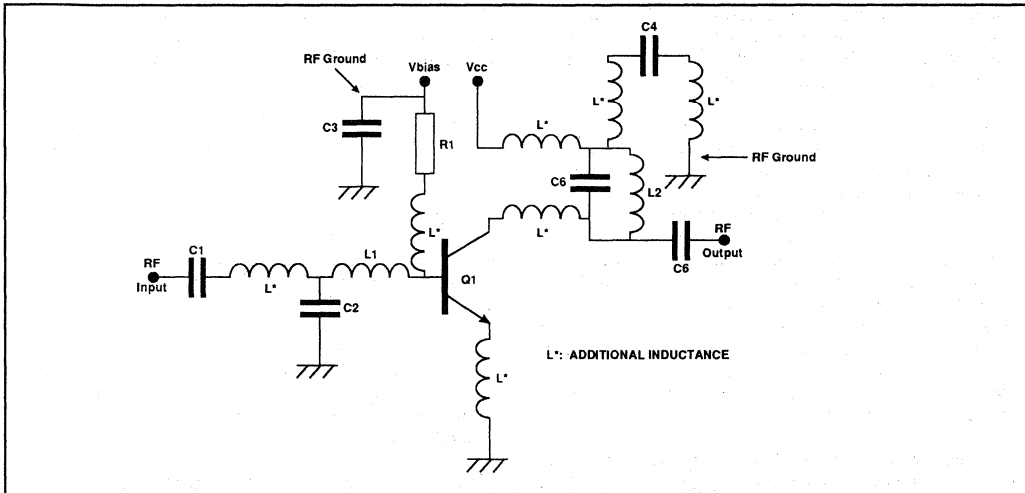


Fig.4 Shows effects of poor layout

## RADIO PAGER DESIGN USING THE SL6649-1 & MV6639

### INTRODUCTION

The SL6649-1 is a Direct Conversion Receiver which receives Frequency Shift Keying (FSK) RF signal up to 200 MHz and converts it into digital data for decoding. All the appropriate filtering is done on-chip. Two voltage references are available for external RF amplifier biasing if required.

The MV6639 is a POCSAG decoder and voltage doubler combined. The voltage doubler can be used to power a micro and LCD display in a normal pager. The decoder has low power consumption and can operate down to 1 V.

This application note gives full detail of the circuit, PCB layout and adjustment procedures of a 153 MHz, 512 baud tone only radio pager using the GPS SL6649-1/MV6639 chip-set. The demonstration board has an integral loop antenna for field measurement purposes. An additional connector is provided for initial adjustment and terminal sensitivity evaluation.

Data sheets of the SL6649-1 and MV6639 should be referred to where necessary. Further detail on the design of the receiver can be found in the SL6649-1 applications note AN118 "Using the SL6649-1 in Low Profile Applications at Frequency below 200 MHz".

### RF AMPLIFIER

The two on-chip voltage references are used to bias an external cascode amplifier which feeds the differential inputs of the mixer through a transformer. Fig. 1 shows the complete circuit diagram of the pager demonstration board. The position of the base decoupling capacitor C11 of the transistor TR1 is important and should be as close to the base as possible for repeatable and stable operation of the amplifier.

The value of the load resistor R4 sets the maximum available gain of the amplifier. The trimmer capacitor VC2 together with the transformer form the output tuned load of the amplifier.

The input LC network ( L4, C31, C32 ) to the amplifier is designed for an optimum noise figure to give the best overall device sensitivity.

### LOCAL OSCILLATOR

The local oscillator utilises the 280µA current source provided by the SL6649-1 at pin 21. The purpose of the inductor L1 is to tune out the crystal capacitance and suppress oscillation at the fundamental frequency. Crystals from different manufactures may require a different value for L1.

The output circuit at the collector of TR3 is designed to be resonant at 153 MHz. The output signal is fed to a RC quadrature network consisting of R7/C18 and R6/C17 then to the mixer LO input ports.

The entire local oscillator should be screened to minimise radiation feed-through from the LO to the RF amplifier/antenna front-end. The result of any appreciable radiation feed-through tends to desensitise the receiver. At least 10-15 dB additional isolation can be achieved by proper screening of the LO.

### DATA BUFFER

The transistor pair TR4-TR5 shown in the data buffer section of Fig. 1 forms the data buffer which provides isolation between the receiver data output and the POCSAG decoder data input. The high impedance at the buffer input reduces current surge at the data output of the receiver and minimises interference.

### DECODER

The POCSAG data from the data buffer is connected to the input to the MV6639. The 32 kHz reference frequency of the decoder is generated by an on-chip oscillator with an external 32 kHz watch crystal.

The RIC ( Radio Identification Code ), baud rate selection and other housekeeping information are stored in the EEPROM (IC3). Upon switch on, the decoder resets itself and loads the appropriate programmed data from the EEPROM.

After receiving a correct message, the sounder will sound at a low level for 4 seconds then at a higher level for another 12 seconds. The alert tone will sound for 16 seconds in total if it is not terminated before by closing the reset switch SW2.

### VOLTAGE DOUBLER

The voltage doubler provided by the MV6639 is used to power the VCC2 of the receiver at 2.7V. A Schottky rectifying diode should be used for D1 for high doubling efficiency.

The oscillator frequency within the voltage doubler varies with the amount of current drawn from it. As with all voltage doubling circuits the output voltage decoupling is very important. The decoupling capacitors should be placed as close to the doubler output as possible. Detail decoupling requirement can be found in the MV6639 data sheet. In the pager demonstration board the doubler runs at about 40 KHz and the ripple on the output of 2.7V is approximately 5mVpk-pk.

Although the oscillator frequency of the voltage doubler is considered to be out-of-band it is recommended to screen D1 and L5 to minimise possible interference.

### ANTENNA

Fig. 2 shows the physical dimensions of the loop antenna used in the pager demonstration board. Fig. 3 shows the input impedance of the loop as measured on a network analyser.

Fig. 4 shows the antenna matching circuit with 50 ohm source impedance reference and the measured resonant dip at 153 MHz. VC1 is capable of tuning the resonant dip to at least  $F_0 \pm 5$  MHz. The coupling capacitor C9 also contributes to the tuning of the resonant dip but for high Q operation its value should be kept small.

The material used for the antenna should have high conductivity e.g. copper. This is due to the fact that the radiation resistance of this type of antenna is very low so any significant ohmic loss will degrade the overall antenna efficiency.

The impedance level at the interface between the RF amplifier and the antenna is designed to be 50 ohm. This simplifies the design and the measurement tasks of the individual RF amplifier and antenna.

## AN172

### TERMINAL SENSITIVITY MEASUREMENT

Fig. 5 shows the pager demonstration board PCB layout and components placement. For terminal sensitivity measurement the input signal goes through C31 and L4 then to the RF amplifier.

Fig. 6 illustrates the measurement set-up for terminal sensitivity.

### MEASUREMENT PROCEDURE

a) Apply a signal from a 50 ohm source impedance signal generator at a nominal frequency of 153.000 MHz and level of -73 dBm to the SMA connector on the demonstration board.

b) Monitor test point TB (pin 28 on the SL6649-1) with an oscilloscope set at 20mV/div.

c) Adjust trimmer VC3 until maximum signal is obtained on the oscilloscope.

d) Adjust the signal generator frequency  $f_o$  until a 4 kHz signal appears on the oscilloscope.

e) Re-adjust VC3 to peak the amplitude of the 4 kHz signal.

f) To acquire the optimum gain of the RF amplifier, adjust the trimmer VC2 until maximum amplitude is obtained at the test point. The overall gain can be increased by increasing the value of the load resistor R4 and vice versa until an optimum level of  $100\text{mV} \pm 10\text{mV}$  pk-pk is reached at the test point.

g) Adjust the signal generator frequency  $F_o$  until the frequency at the test point is zero i.e. zero beat. The pager local oscillator frequency is then equal to the signal generator frequency  $F_o$

h) Encode the signal generator with a POCSAG encoder as shown in Fig. 6. Reduce the signal level until 4 out of 5 calls are correctly received by the pager. This level is considered to be the terminal sensitivity and should be at -126 dBm or lower.

### EVALUATION OF OVERALL SENSITIVITY

Absolute pager sensitivity in terms of  $\mu\text{V/m}$  cannot easily be measured without the use of a screened enclosure and a calibrated field strength meter. The pager demonstration board was evaluated in a TEM cell whose detail is shown in Fig. 7. Measurements were carried out by comparing the demonstration pager sensitivity with other commercial pager of known absolute sensitivity. Fig. 8 shows the measurement set-up.

### TUNING PROCEDURE

a) It is assumed that the demonstration pager board has been adjusted for maximum terminal sensitivity as detailed above.

b) Disconnect the signal path from L4 to C31, instead connect L4 to C9.

c) Disable the encoding signal to the signal generator and offset the centre frequency  $F_o$  to  $F_o+4\text{kHz}$ , and set the output amplitude to about -50 dBm.

d) Place the pager board in a TEM cell and monitor the 4kHz signal at the test point using an oscilloscope set at 20mV/div. Adjust the trimmer VC1 until the amplitude of the 4kHz signal is at maximum.

e) Change the signal generator frequency back to  $F_o$ . The tuning procedure of the pager board is now complete.

f) Encode the signal generator with a POCSAG encoder as illustrated in Fig. 8. Orientate the pager board within the TEM cell until the most sensitive position is obtained. Reduce the signal generator output level until 4 out of 5 calls are correctly received by the pager. This is the overall sensitivity of the pager measured in this particular TEM cell. Relative performance can be obtained by carrying out similar measurement on other pagers with known sensitivity.

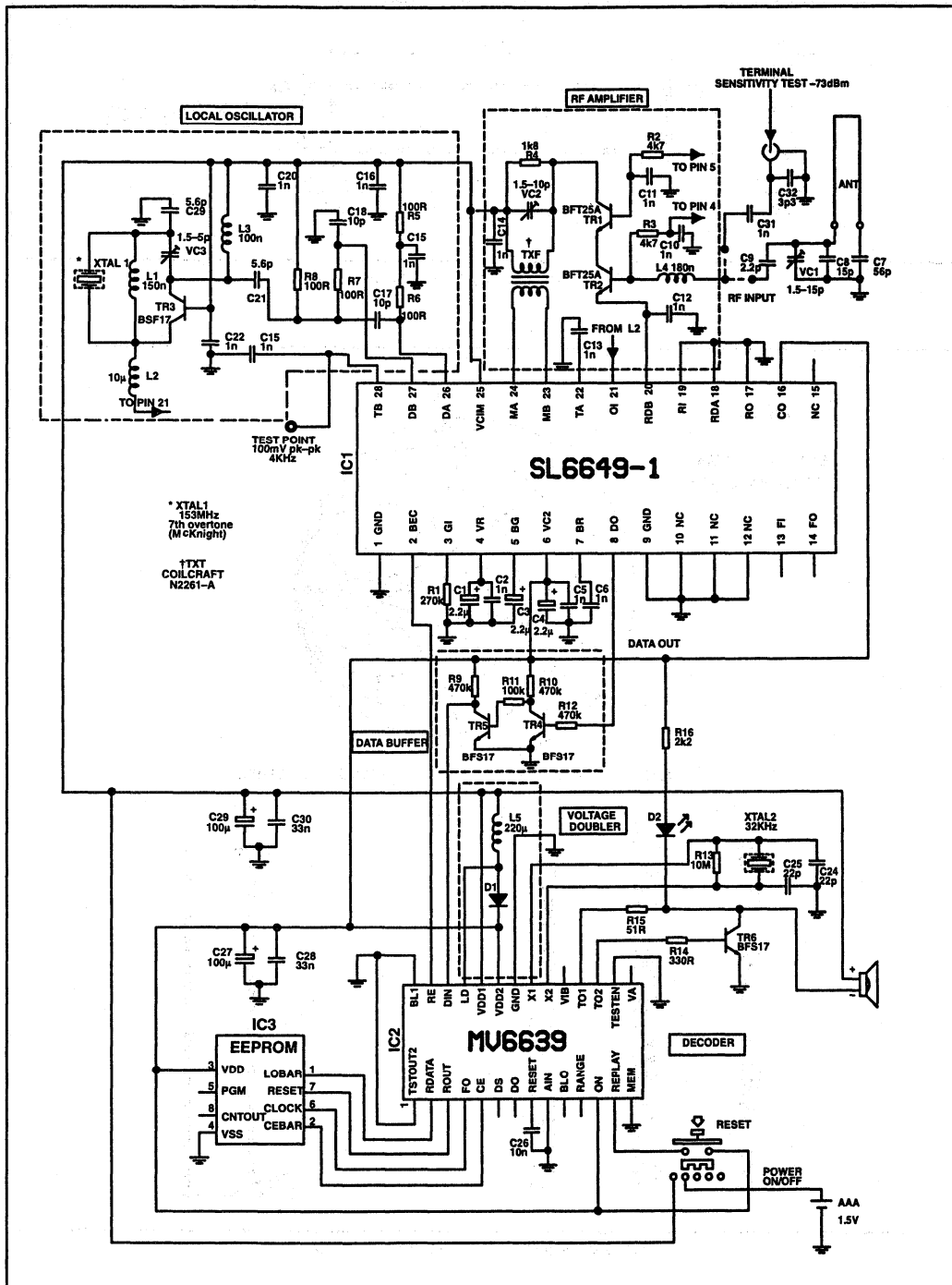


Fig. 1 SL6649-1/MV6639 radio pager

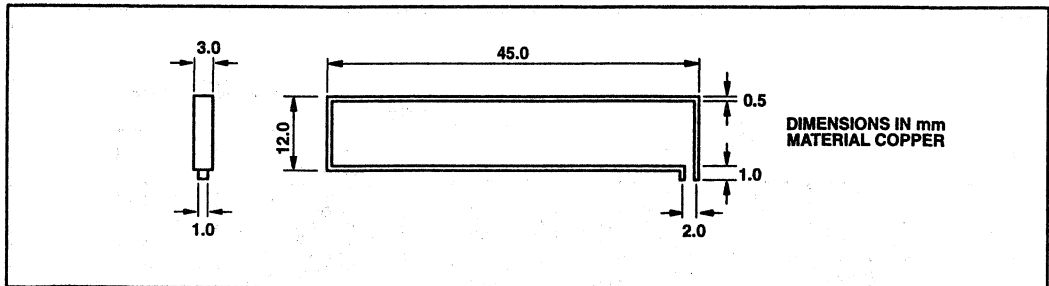


Fig. 2 153MHz pager loop antenna

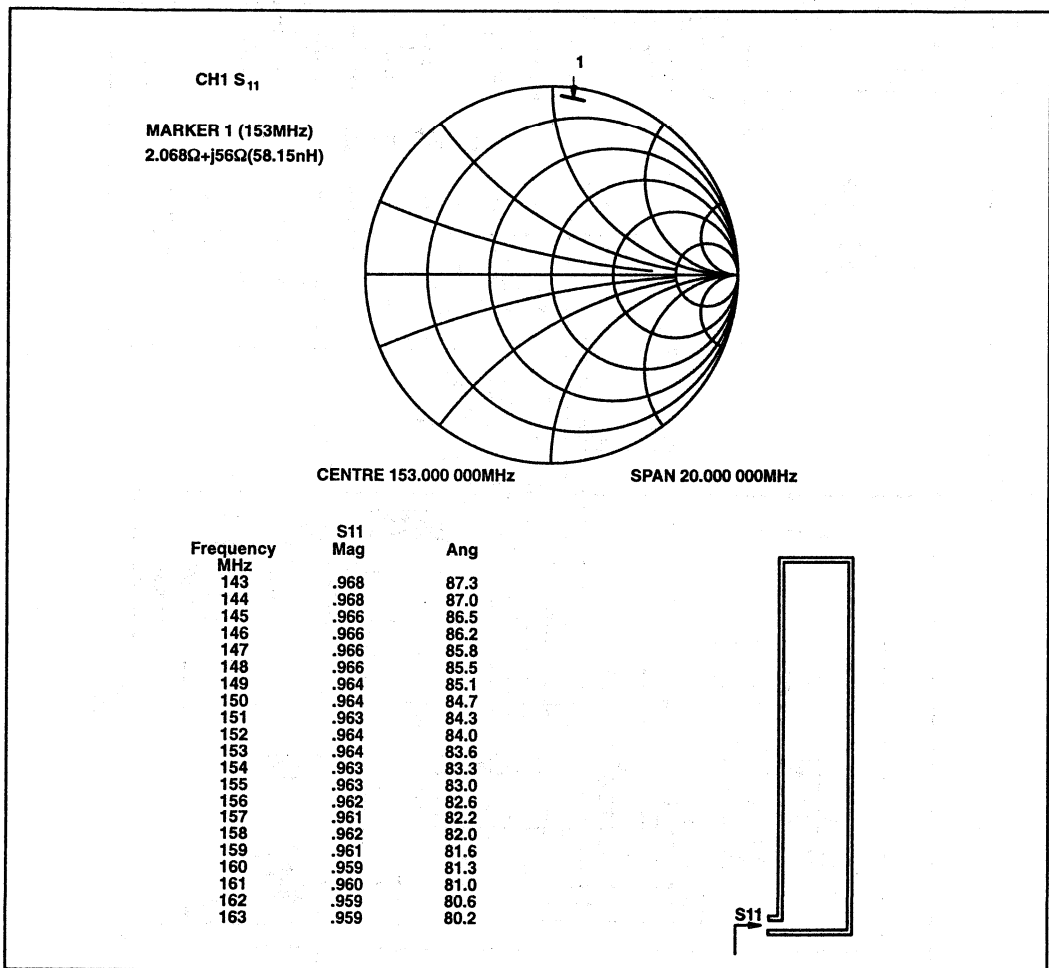


Fig. 3 Input S-parameter of the loop antenna



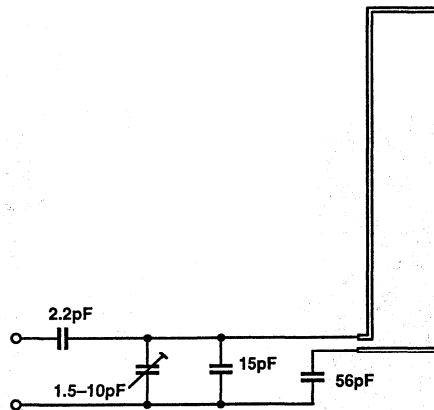
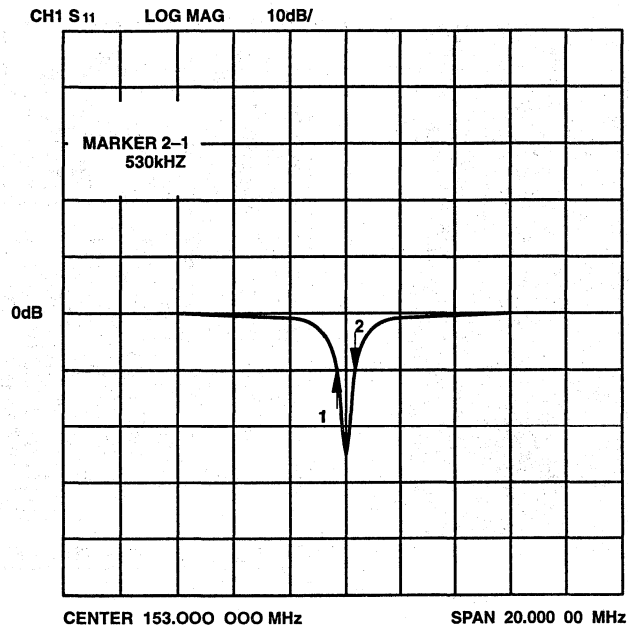


Fig. 4 Loop antenna matching circuit

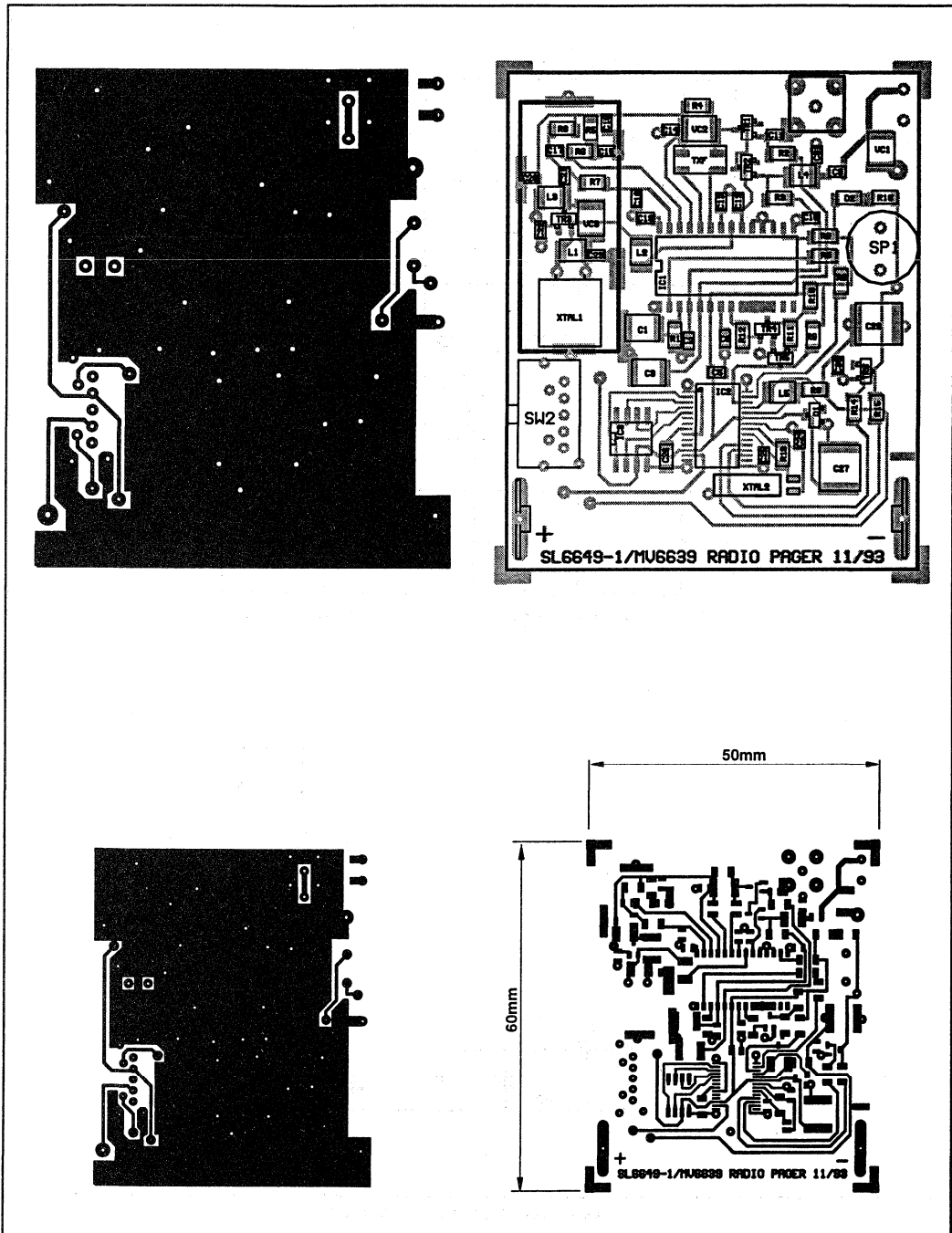


Fig. 5 Pager demonstration board PCB layout and component placement

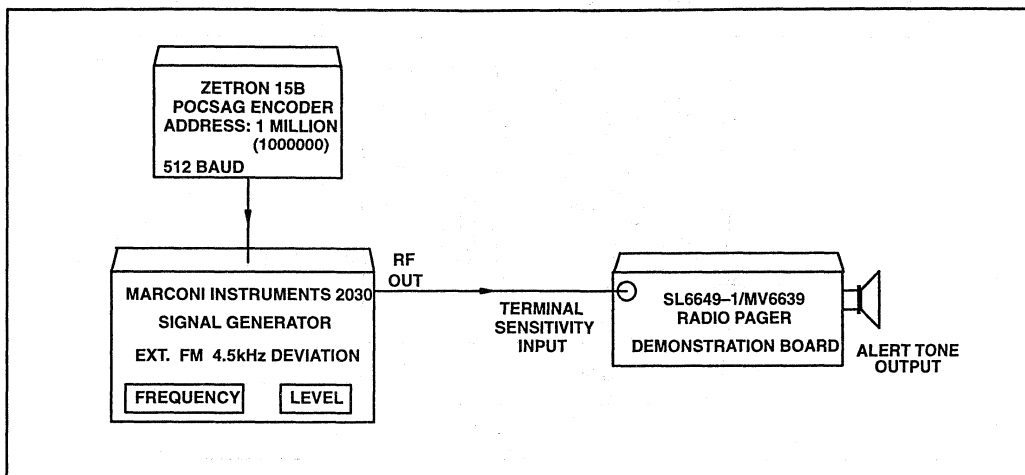


Fig. 6 Terminal sensitivity measurement set-up

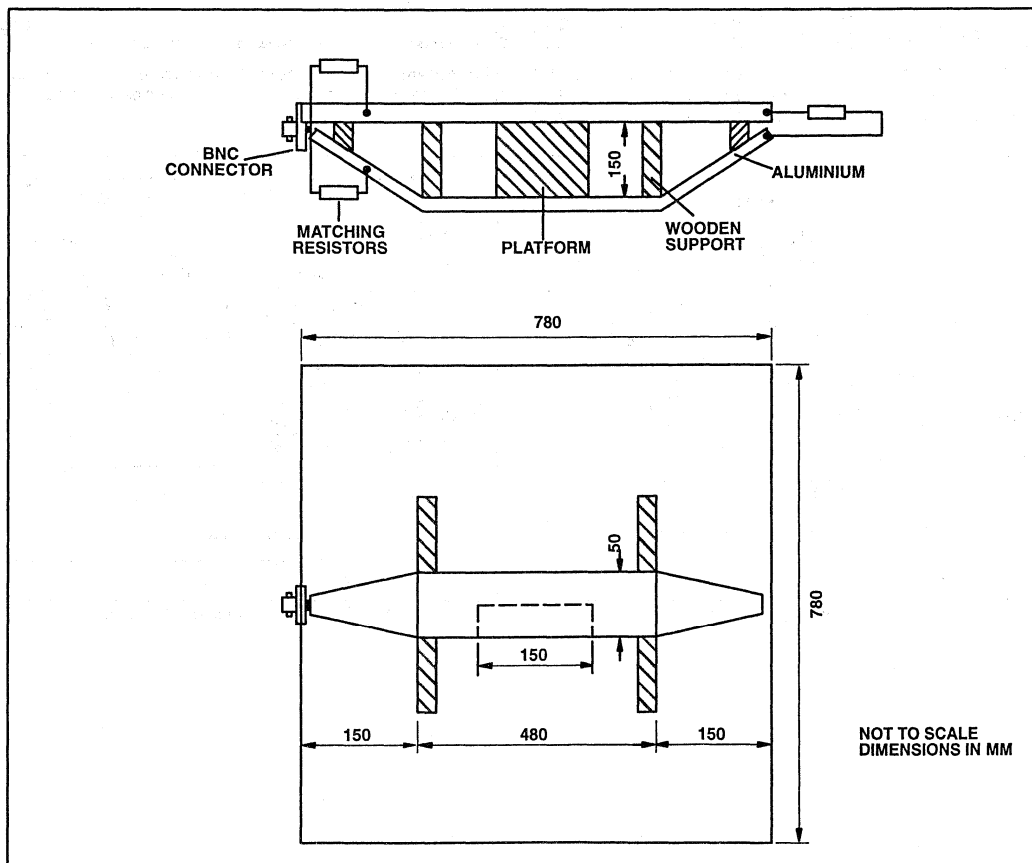


Fig. 7 Overall sensitivity measurement TEM cell

# 154MHz Local Oscillator for the SL6649-1

AB38

Fig. 1 shows a 154MHz local oscillator circuit for the SL6649-1 FSK data receiver, using a 3rd overtone crystal which is series resonant at half the required output frequency.

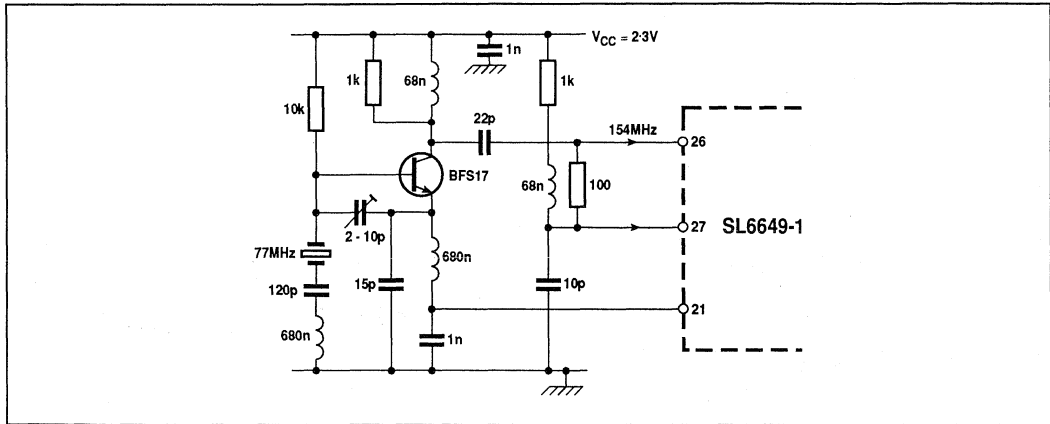


Fig. 1

# Using the SL6649-1 at 230MHz

AB39

The SL6649-1 will operate at 230MHz using the internal LNA, although with reduced sensitivity. Suggested circuits for the LNA and local oscillator are shown in Figs. 1 and 2, respectively. X1 in Fig. 2 is a 3rd overtone series resonant crystal with a nominal frequency of one third the required LO frequency.

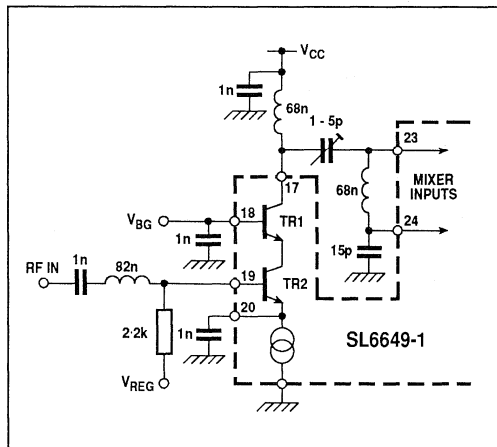


Fig. 1 230MHz LNA circuit

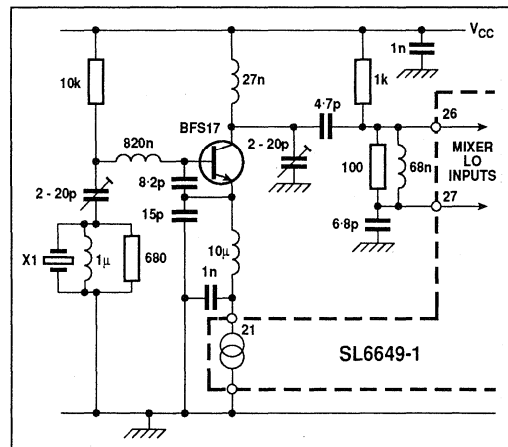


Fig. 2 230MHz local oscillator circuit

## USING THE SL6649-1 IN LOW PROFILE APPLICATIONS AT FREQUENCIES BELOW 200MHz

### INTRODUCTION

This Application Note describes the use of the SL6649-1 at frequencies below 200MHz. A new circuit design has been used which eliminates the transformers that were used in previous demonstration boards for this device. This has the benefit of being able to use small, low profile components enabling a receiver to be built with a maximum component height of 2mm. (using the low profile chip carrier package).

The AC characteristics given in the SL6649-1 data sheet are based on the use of transformer matching from the RF amplifier to the mixer. Use of the transformerless circuit can result in a lower front end gain and thus may degrade the overall receiver performance. Improved performance may be achieved by the use of an external low noise, high gain transistor amplifier in place of the on-chip cascode arrangement.

### RF AMPLIFIER

The on-chip amplifier consists of two transistors configured in cascode. This is illustrated in Fig.1. Bias is provided by a current source on pin 20 and the voltage  $V_{BG}$  and  $V_A$  via R1. At high signal levels this current source is dependent on the R.F. level at the mixer inputs and can therefore provide an automatic gain control (AGC) function.

Pin 20 is decoupled to ground by a 1nF capacitor. The upper transistor being in common base has its base decoupled to ground by a 1nF capacitor.

The input to the cascode is matched to a 50 Ohm source by a single series inductor (L3). It is also wise to include a 1nF dc blocking capacitor (C11) between the signal source and the input circuit. The output load is a tuned circuit with a capacitor tap to match the combination of an LC phase shift network (L5 and C21) and the differential mixer inputs. The component values for the LC phase shift network are chosen to give equal amplitude and 180 degrees phase shift between the mixer R.F. inputs. This circuit will be dependant on the impedance of the mixer input. Some experimentation with the values of L5 and C21 may be necessary to achieve optimum gain and intermodulation performance.

The internal cascode amplifier works optimally at frequencies up to 200MHz. Above 200MHz the receiver will work with reduced sensitivity due to the bandwidth and noise figure limitations of the internal amplifier. For use at frequencies up to 500MHz where high performance is required, an external amplifier is recommended.

### LOCAL OSCILLATOR

The L.O. which is shown in Fig. 2, uses an external transistor which is connected to a 280 $\mu$ A current source on pin 21 of the SL6649-1 via inductor L6. The oscillator feedback circuit comprises a capacitor tap (VC2, C23 and C18) and a series resonant crystal which is shunted by an inductor (L4) to suppress oscillation at the crystal fundamental frequency by tuning out the holder capacitance. The base of the transistor is connected to  $V_{CC1}$  and decoupled to ground by a 1nF capacitor. The collector circuit is designed to be resonant at the required oscillator frequency and the output signal is fed to an RC quadrature network consisting of R6, R7, C13 and C15 via a capacitor (C17) and then to the mixer L.O. input ports. This RC network is designed such that R and the reactance of the capacitor, C, equals 100 Ohm at the wanted frequency.

### OVERALL RECEIVER CIRCUIT

The complete receiver block schematic is shown in Fig. 3 and illustrates the remaining ancillary components which are not dependant on the RF frequency used.

### RECEIVER ALIGNMENT

Monitor the output at pin 28 of the device with an oscilloscope set to 20mV/div. (A.C. coupled). Feed the R.F. input from a 50 Ohm signal generator set at the nominal crystal frequency at a level of about 20 $\mu$ V (-80dBm). Tune VC2 for a zero beat at pin 28 (channel B test). Now offset the generator frequency by 2-3 KHz, this should give a sine wave output of about 50mV p-p. Tune VC1 for a maximum at the pin 28 test point.

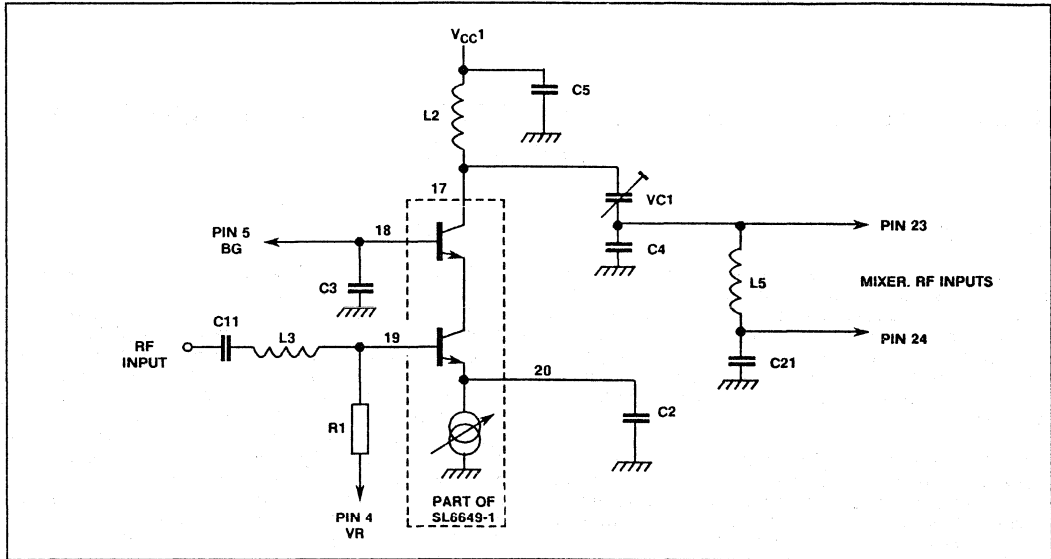


Fig. 1 R.F. amplifier

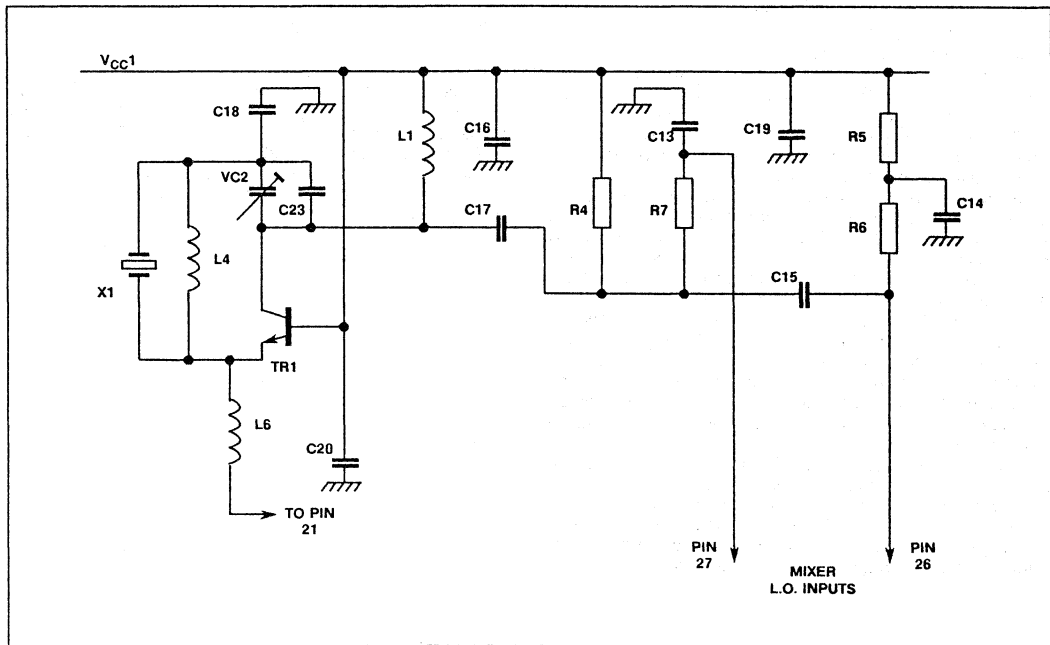


Fig. 2 Local oscillator

COMPONENTS	50MHz	153MHz	173MHz	COMPONENTS	50MHz	153MHz	173MHz
C1	1nF	1nF	1nF	L1	470nH	100nH	100nH
C2	1nF	1nF	1nF	L2	1μH	100nH	100nH
C3	1nF	1nF	1nF	L3	390nH	100nH	100nH
C4	-	22pF	33pF	L4	-	220nH	220nH
C5	22nF	1nF	1nF	L5	470nH	150nH	100nH
C6	2.2μF	2.2μF	2.2μF	L6	10μH	10μH	10μH
C7	2.2μF	2.2μF	2.2μF	R1	2.2K	2.2K	2.2K
C8	1nF	1nF	1nF	R2	270K	270K	270K
C9	2.2μF	2.2μF	2.2μF	R4-R7	100	100	100
C10	2.2μF	2.2μF	2.2μF	R8	100K	100K	100K
C11	1nF	1nF	1nF	TR1	BFS17	BFS17	BFS17
C12	1nF	1nF	1nF	TR2	BFS17	BFS17	BFS17
C13	33pF	10pF	10pF	VC1	1.5-10pF	1.5-10pF	1.5-10pF
C14	1nF	1nF	1nF	VC2	1.5-10pF	1.5-10pF	1.5-5pF
C15	33pF	10pF	10pF				
C16	1nF	1nF	1nF	X1	50MHz series res.	153MHz series res.	173MHz series res..
C17	3.3pF	3.9pF	3.9pF				
C18	18pF	4.7pF	1.5pF				
C19	1nF	1nF	1nF				
C20	1nF	1nF	1nF				
C21	33pF	10pF	10pF				
C23	39pF	-	-				

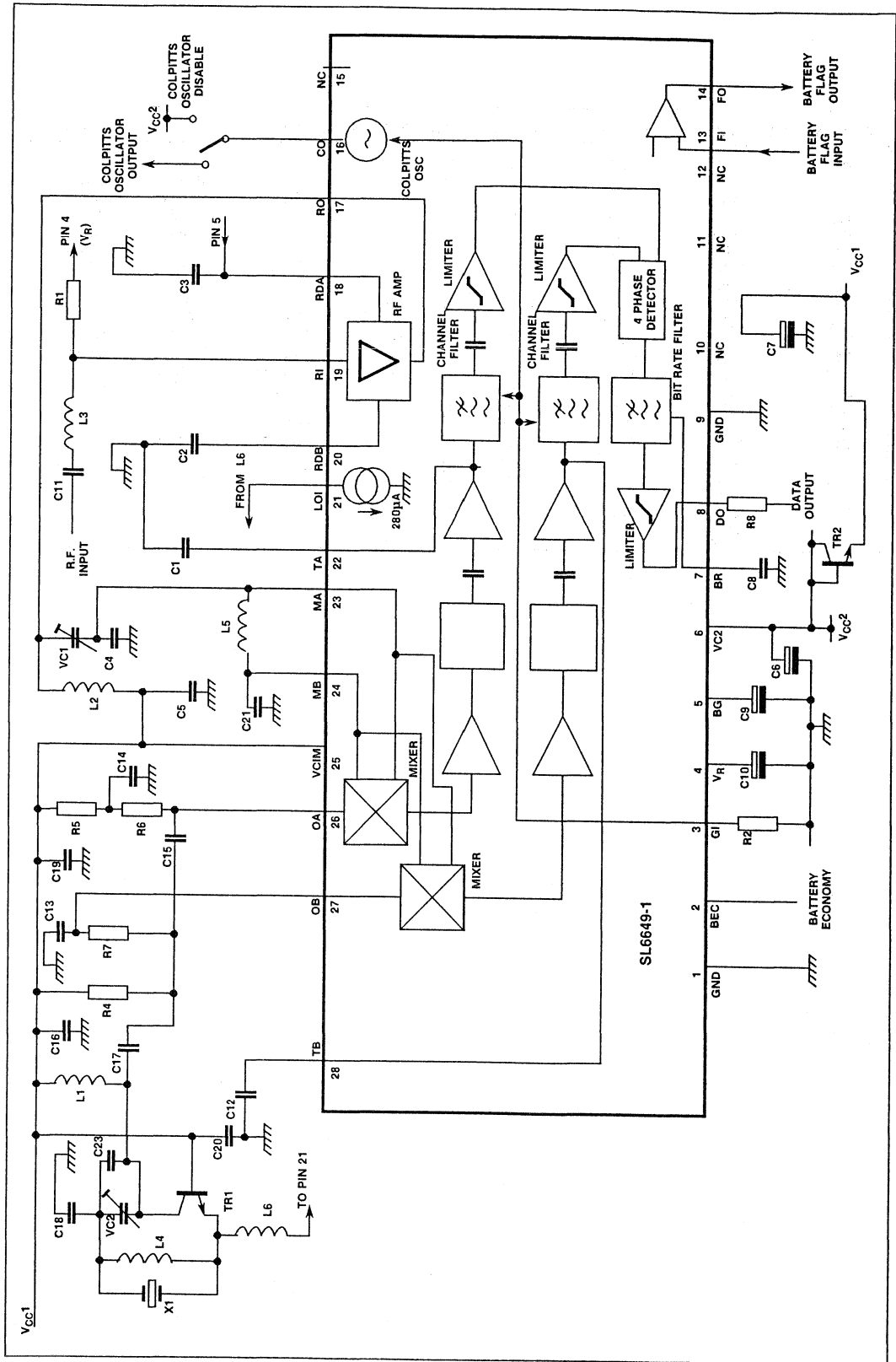
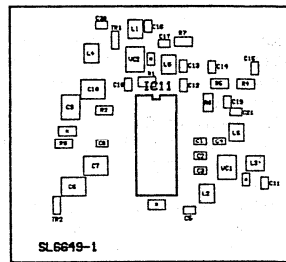
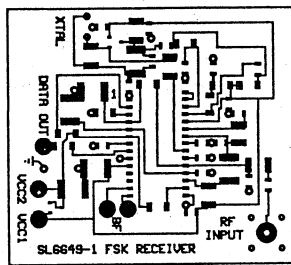


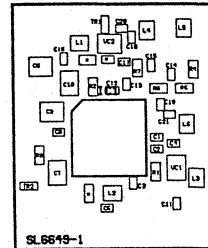
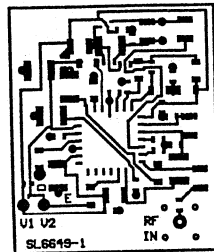
Fig. 3. Circuit diagram of receiver



P.C.B. LAYOUTS  
MP PACKAGE



P.C.B. LAYOUTS  
LCPACKAGE



The SL6649-1 is a single chip radio receiver. The input signal is analog, and can be as low as 100nV RMS while the output is a digital signal of >2V p-p. The large differences in signal levels around the chip make careful layout essential if the full performance of the device is to be achieved.

Where possible a layer of the PCB should be used as a ground plane. This helps minimise stray inductance in the ground connections of the circuit. Careful decoupling at both radio and audio frequencies is required to achieve optimum performance. RF decoupling capacitors should be placed close to the circuit they are decoupling to minimise stray inductance.

In a direct conversion receiver, such as the SL6649-1, the local oscillator is on the receive frequency. The antenna is tuned to this frequency so can pick up significant local oscillator power. This can be at a high enough level to cause a significant degradation in receiver performance unless a few simple precautions are taken. Where an antenna is fitted on or close to the receiver board it is important to position the oscillator as far as possible from the antenna. Screening of the oscillator circuit helps reduce oscillator pick up in the antenna. The most important components to screen are the inductors, because these produce the largest radiated field. The can of the crystal should be connected to ground. The local oscillator circuit should be well separated from the RF amplifier to prevent coupling of the local oscillator circuit into the RF amplifier.

## 1. Gnd

The main ground pin for the IC.

It should be connected to the ground plane. Track length must be kept to a minimum.

## 2. Battery Econ

A digital control signal used to enable and disable the receiver. During the receive period this pin is held at a constant high voltage, so should not cause any problems.

## 3. Gyrator Current Adjust

Input used to tune the gyrator filter.

A resistor is connected from this pin to 0V. No special precautions are required for this pin.

## 4. Reference Voltage

A reference voltage used internally in the chip.

This pin must be decoupled by a capacitor of 2.2µF minimum. The capacitor should be as close as possible to the chip. If this output is to be used to bias the RF amplifier it should also be decoupled at radio frequencies, using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced onto this pin from the data output.

## 5. Bandgap Voltage Reference

A reference voltage used internally in the chip.

This pin must be decoupled by a capacitor of 2.2µF minimum. The capacitor should be as close as possible to the chip. If this output is to be used to bias the RF amplifier it should also be decoupled at radio frequencies, using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced onto this pin from the data output.

## 6. V<sub>CC</sub> 2

The higher voltage power supply to the chip.

This pin should be decoupled at radio frequencies by a 1000pF capacitor as close as possible to the pin. It may also be necessary to provide audio frequency decoupling using a much larger capacitor, usually 2.2µF-10µF is sufficient.

## 7. Bit Rate Filter

The signal on this pin has a large voltage swing so should be kept well away from the RF input, oscillator circuit and reference voltages. This can be achieved easily if the bit rate filter capacitor is fitted close to the pin.

## 8. Data Output

Received data output.

The data output is a digital signal going between 0v and V<sub>CC</sub> 2. This is a source of noise which can degrade the performance of the receiver. A 100kΩ resistor should be connected to the data output pin and placed as close as possible to the chip. The data output signal should be routed so that it is well away from the RF input, oscillator circuits and reference voltages.

## 9. Ground

Additional ground pin for the chip.

It should be connected to the ground plane. Track length should be kept as short as possible.

## 10, 11, 12. Not Connected

These pins are not connected to the chip.

Where possible connect these pins to ground rather than leaving them floating.

## 13. Battery Flag Input

Low battery detector output.

When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.

## 14. Battery Flag Output

When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.

## 15. Not Connected

This pin is not connected to the chip.

Where possible connect this pin to ground rather than leaving it floating.

## 16. Colpitts Oscillator Output/Disable

Gyrator filter tuning output.

This pin should be connected to V<sub>CC</sub> 2. No special precautions are required.

## 17. RF Amplifier Output

Cascode RF amplifier output.

The output from the RF amplifier should not pass close to the RF input (pin 19). The load inductor for the RF amplifier should be close to this pin. RF decoupling of 1000pF should be provided on the positive supply connection to the inductor.

## 18. RF Base Decouple

RF amplifier bias decoupling.

A 100 pF decoupling capacitor should be connected from ground to this pin. It should be as close to the pin as possible.

## 19. RF Base Input

Cascode RF amplifier input.

This is the most sensitive part of the circuit. All tracks from the RF input should be kept separate from the RF amplifier output, i.e. they should not run parallel. Also the RF input should be well separated from the oscillator circuit to prevent stray coupling. Bias to the RF amplifier is provided by the reference voltage (pin 4). This should be connected via a 2.2kΩ resistor.

## 20. RF Emitter Decouple

Emitter of RF cascode amplifier.

A 100pF capacitor must be connected to ground from this pin. It should be connected as close to the pin as possible.

## 21. Local Oscillator Current Sink

Current sink used to power the local oscillator.

A small amount of the local oscillator signal will be present on this pin so the track from it should not pass close to the RF input. Also the local oscillator is sensitive to audio frequency noise so the track should be kept away from the data output.

## 22. Channel A Test

Mixer A output test point.

This output is often used for production testing so should have a test point. It is sensitive to audio frequency noise so

# ADVICE ON USING THE SL6649-1

## INTRODUCTION

This application note describes the use of the SL6649-1 direct conversion radio receiver, and how to obtain the optimum performance from the device. Additional application notes are available for this device in specific application areas, such as low profile applications from GEC Plessey Semiconductors.

This note is split into three main sections to assist uses of the device. These are:-

1. Layout around the SL6649-1 which gives guidance on the PCB layout for the receiver.
2. Gain distribution in the SL6649-1 which defines the gain at various steps of the receiver.
3. RF amplifiers for the SL6649-1 which provides information with regard to the internal RF amplifier plus some suggestions for an external amplifier.

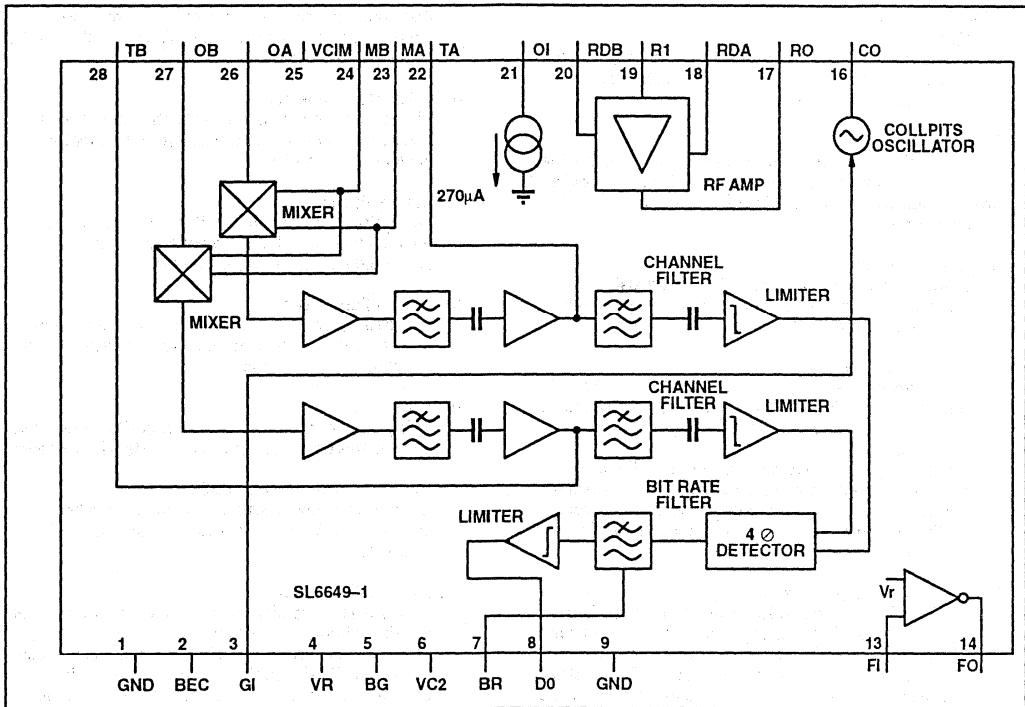


Fig. 1 Functional block diagram of the SL6649-1

## AN141

### INTRODUCTION

The SL6649-1 is a single chip radio receiver. The input signal is analogue and can be as low as 100nV rms while the output is a digital signal of >2vp-p. The large differences in signal levels around the chip make careful layout essential if the full performance of the device is to be achieved. Where possible a layer on the PCB should be used as a ground plane. This helps minimise stray inductance in the ground connections of the circuit. Careful decoupling at both radio and audio frequencies is required to achieve optimum performance. RF decoupling capacitors must be placed close to the circuit, they are decoupling to minimise stray inductance. In a direct conversion receiver, such as the SL6649-1, the local oscillator is on the receive frequency. The antenna is tuned to this frequency so L.O. pick up can cause significant degradation in receiver performance unless a few simple precautions are taken. Where an antenna is fitted on or close to the receiver board it is important to position the oscillator as far as possible from the antenna. Screening of the oscillator circuit helps reduce oscillator pick up in the antenna. The most important components to screen are the inductors, because these produce the largest radiated field. The can of the crystal should be connected to ground. The local oscillator circuit should be well separated from the RF amplifier to prevent coupling of the local oscillator signal into the RF amplifier.

### Pin description

- 1. Gnd**  
The main ground pin for the IC. It should be connected to the ground plane. Track length must be kept to a minimum.
- 2. Battery Econ**  
A digital control signal used to enable and disable the receiver. During the receive period this pin is held at a constant high voltage so should not cause any problems.
- 3. Gyator current adjust**  
Input used to tune the gyator filter. A resistor is connected from this pin to 0V. No special precautions are required for this pin.
- 4. Reference voltage**  
A reference voltage used internally in the chip. This pin must be decoupled by a capacitor of 2.2uF minimum. The capacitor should be as close to the chip as possible.  
If this output is used to bias the RF amplifier it should also be decoupled at radio frequencies using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced into this pin from the data output.
- 5. Bandgap voltage reference**  
A reference voltage used internally in the chip. This pin must be decoupled by a capacitor of 2.2uF minimum. The capacitor should be as close to the chip as possible. If this output is used to bias the RF amplifier it should also be decoupled at radio frequencies using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced into this pin

- 6. Vcc2**  
The higher voltage power supply pin to the chip. This pin should be decoupled at radio frequencies by a 1000pF capacitor as close as possible to the pin. It may also be necessary to provide audio frequency decoupling using a much larger capacitor, usually 2.2-10uF is sufficient.
- 7. Bit rate filter**  
The signal on this pin has a large voltage swing so should be kept well away from the RF input, oscillator circuit and reference voltages. This can be achieved easily if the bit rate filter capacitor is fitted close to the pin.
- 8. Data Output**  
Received data output. The data output is a digital signal going between 0V and Vcc2. This is a source of noise which can degrade the performance of the receiver. A 100k resistor should be connected to the data output pin and placed as close as possible to the chip. The data output signal should be routed so that it is well away from the RF input, oscillator circuit and reference voltages.
- 9. Ground**  
Additional ground pin for the chip. It should be connected to the ground plane. Track length must be kept to a minimum.
- 10,11,12 Not connected**  
These pins are not connected to the chip. Where possible connect these pins to ground rather than leaving them floating.
- 13. Battery flag input**  
Low battery detector input. When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.
- 14. Battery flag output**  
Low battery detector output. When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.
- 15. Not connected**  
This pin is not connected to the chip. Where possible connect this pin to ground rather than leaving it floating.
- 16. Colpits oscillator output/disable**  
Gyator filter tuning output. This pin should be connected to Vcc2. No special precautions are required.
- 17. RF amplifier output**  
Cascode RF amplifier output. The output from the RF amplifier should not pass close to the RF input (pin 19). The load inductor for the RF amplifier should be close to this pin. RF decoupling of 1000pF should be provided on the positive supply connection to the inductor.

18. **RF base decouple**  
RF amplifier bias decoupling. A 1000pF decoupling capacitor should be connected to ground from this pin. It should be as close to the pin as possible.
19. **RF base input**  
Cascode RF amplifier input. This is the most sensitive part of the circuit. All tracks to the RF input should be kept separate from the RF amplifier output, ie they should not run parallel. Also the RF input should be well separated from the oscillator circuit to prevent stray coupling. Bias to the RF amplifier is provided by the reference voltage (pin 4), via a 2K2 resistor.
20. **RF emitter decouple.**  
Emitter of RF cascode amplifier.  
A 1000pF decoupling capacitor should be connected to ground from this pin. It should be as close to the pin as possible.
21. **Local oscillator current sink**  
Current sink used to power the local oscillator. A small amount of the local oscillator signal will be present on this pin so the track from it should not pass close to the RF input. Also the local oscillator is sensitive to audio frequency noise so the track should be kept away from the data output.
22. **Channel A test**  
Mixer A output test point. This output is often used for production testing so should have a test point. It is sensitive to audio frequency noise so should be separated from noise sources such as the data output. A 1000pF capacitor must be connected from this point to ground, because this forms part of the adjacent channel filtering.
23. **Mixer input**  
RF input to the mixer. Pin 23 and 24 form the differential RF input to the SL6649-1 mixers. Tracks to these pins should be short to minimise stray inductance and capacitance.
24. **Mixer input**  
See Pin 23.
25. **Vcc1**  
The lower voltage power supply pin to the chip. This pin should be decoupled at radio frequencies by 1000pF capacitor as close as possible to the pin. It may also be necessary to provide audio frequency decoupling using a much larger capacitor, usually 2.2-10  $\mu$ F is sufficient.
26. **Local oscillator input A**  
Local oscillator input to mixer A. A high level of local oscillator signal is present on this pin so the track to it should be routed away from the RF input. Radiation from the track to the antenna can degrade receiver performance so the track length should be kept short.
27. **Local oscillator input B**  
Local oscillator input to mixer B.  
See pin 26
28. **Channel B test**  
Mixer B output test point. This output is often used for production testing so should have test point. It is sensitive to audio frequency noise so should be separated from noise sources such as the data output. A 1000pF capacitor must be connected from this point to ground, because this forms part of the adjacent channel filtering.

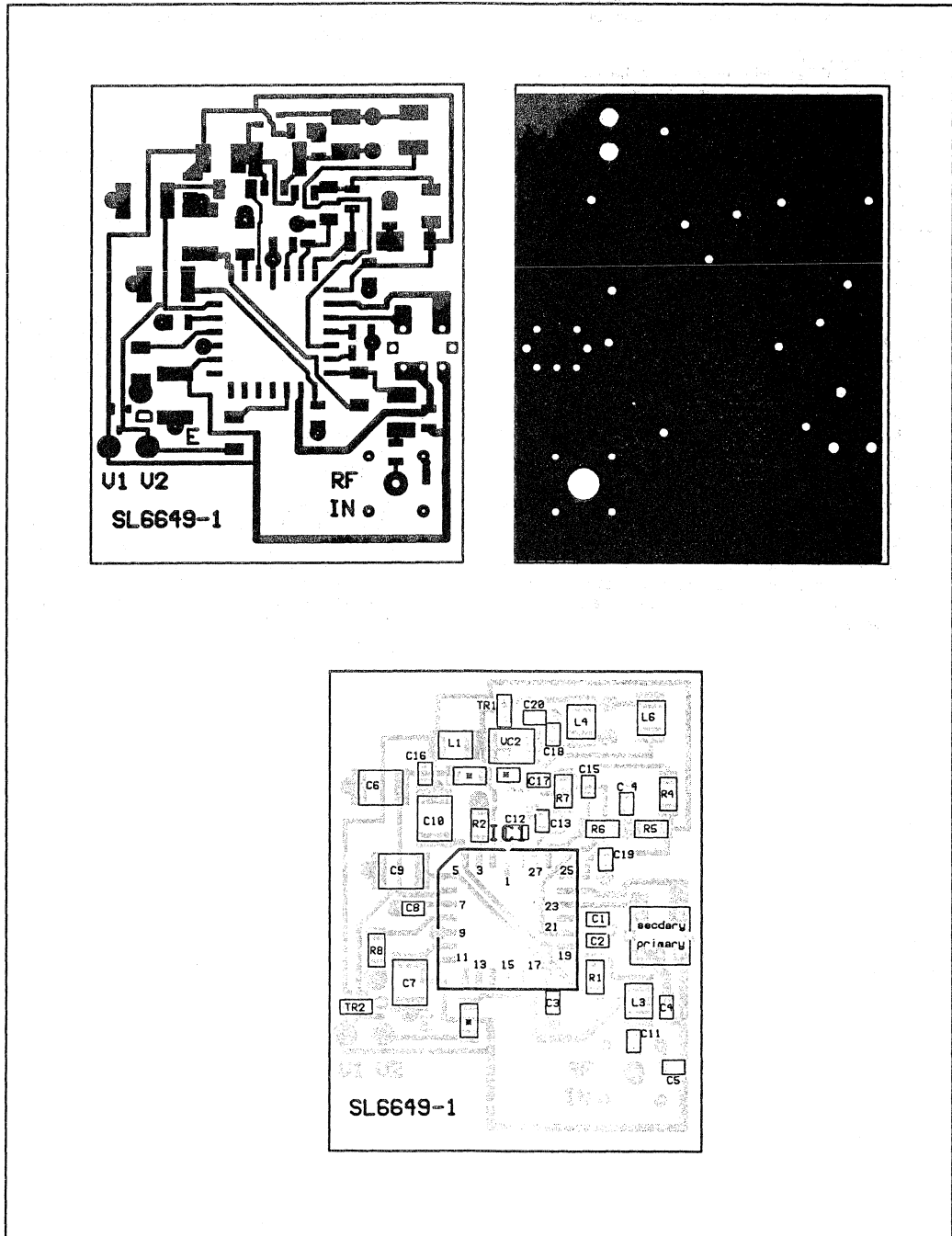


Fig. 2. Example demo board layout (transformer version at 153MHz LCC package)

**COMPONENT LIST****(SL6649-1 Example Demo Board)**

C1 = 1000pF  
 C2 = 1000pF  
 C3 = 1000pF  
 C4 = 2p2  
 C5 = 1000pF  
 C6 = 2 $\mu$ 2  
 C7 = 2 $\mu$ 2  
 C8 = 1000pF  
 C9 = 2 $\mu$ 2  
 C10 = 2 $\mu$ 2

R1 = 2K2  
 R2 = 270K  
 R3 = /  
 R4 = 100R

TR1 = BFS17 (NPN)  
 TR2 = BFS17 (NPN)

L1 = 100nH  
 L2 = /  
 L3 = 150nH

VC2 = 1.5pF to 10pF  
 X1 = 153MHz crystal (series resonant)  
 \* = optional component

C11 = 1000pF  
 C12 = 1000pF  
 C13 = 10pF  
 C14 = 1000pF  
 C15 = 10pF  
 C16 = 1000pF  
 C17 = 3p9  
 C18 = 4p7  
 C19 = 1000pF  
 C20 = 1000pF

R5 = 100R  
 R6 = 100R  
 R7 = 100R  
 R8 = 100K

L4 = 220nH  
 L5 = /  
 L6 = 10 $\mu$ H

Tran = 1:1 transformer (100nH)  
 IC1 = SL6649-1 (LCC 28)

**GAIN DISTRIBUTION IN THE SL6649-1****Introduction**

The circuit design around the SL6649-1 helps to define the gain of various stages in the receiver. It is important to achieve the correct gain distribution if optimum performance is to be achieved. If the gain is too low the receiver noise figure will be dominated by the mixer and poor sensitivity will result, but if the gain is too high the adjacent channel rejecting and intermodulation performance will be degraded due to distortion in the mixer.

**Definition of receiver Gain**

The front end gain of a receiver circuit using the SL6649-1 is defined as the gain from the RF input to the test pins on channel A and B, ie pins 22 and 28 at an IF of the peak deviation frequency.

**Measurement of Receiver Gain**

Receiver gain is normally measured in a circuit where the RF amplifier input is matched to the 50 $\Omega$  output impedance of a signal generator. The generator is set at a standard test level of -73 dBm (50  $\mu$ V rms) and frequency of the nominal channel centre frequency plus the peak deviation frequency eg for a 153 MHz receiver 153 MHz + 4.5 kHz = 153.0045 MHz. Then the peak to peak output level is measured at pins 22 and

28 using a high impedance (>500k) probe on an oscilloscope. The gain is normally expressed purely in terms of the peak to peak amplitude rather than converting this into a true gain from the RF input.

**Factors Affecting the Receiver Gain**

In addition to the chip itself both the RF amplifier gain and the local oscillator level into the mixer will effect the receiver gain. It will also be dependant on temperature and supply voltage.

**Local Oscillator Level**

The mixer is normally operated in a linear region where the gain is directly proportional to the local oscillator input level, ie 1dB increase in local oscillator level will increase the gain by 1dB. The normally recommended local oscillator level is 20 mV rms into the resistor - capacitor phase shift network which gives 10mV rms at the mixer input pins of the chips, pin 26 and 27. However it is possible to achieve acceptable performance with local oscillator levels of up to 6dB greater or 3dB less than this nominal level as long as the RF amplifier gain is adjusted to give the correct receiver gain.

## AN141

### RF Amplifier

The gain of the RF amplifier may be varied by changing the matching between its output and the mixer RF input. Alternatively an off chip RF amplifier may be used in place of the on chip cascode circuit. This gives more flexibility, but may add to the cost and power consumption. The aim of the RF amplifier design is to achieve a low noise figure and the correct level of gain.

### Optimum Receiver Gain

A receiver with optimum gain will produce an output of 100 to 140 mV p-p at the test points A and B for the standard test signal level of -73dBm. Any increase in gain beyond this level will produce very little improvement in the sensitivity, but will significantly degrade both the intermodulation and adjacent channel performance of the receiver. A lower gain will lead to poor sensitivity.

### Insufficient or Excess Receiver Gain

Some designs fail to give reliable results because the receiver gain is inadequate. In designs where an external RF amplifier or the local oscillator are biased directly from Vcc1, in such a way that the current varies with Vcc1, low gain at low Vcc1 has been a major cause of poor performance. Poor local oscillator design can also produce variable receiver gain.

Excessive receiver gain caused by large oscillator drive to the mixer or high RF amplifier gain will degrade the intermodulation and adjacent channel rejection. This can be encountered in circuits where bias currents are dependent on Vcc1. Also if a designer is unable to achieve adequate sensitivity a common solution is to increase the RF amplifier gain or local oscillator drive level. This should not be adopted as a solution if the gain is already adequate as defined above.

### Summary

The overall gain of the receiver must be correct if optimum performance is to be achieved. It is affected by the RF amp gain and the local oscillator level, as well as temperature and supply voltage. The combination of local oscillator drive level and RF amp gain should be set so that for a -73dBm input to the receiver the output from pins 22 and 28 is 100 – 140 mV peak to peak. This should not vary significantly as supply voltage varies. Too low a gain will give poor sensitivity, but gain above this specified level will degrade the adjacent channel rejection and intermodulation performance.

## AUDIO FREQUENCY NOISE AND THE SL6649-1

### Introduction

The SL6649-1 is a direct conversion receiver chip and, much of the signal processing is done at base band. In the case of the receiver this covers frequencies in the audio spectrum, the pass band of the channel filter is from about 1 – 8 kHz. As a result the device is sensitive to audio frequency noise, unlike most RF devices, so careful consideration must be given to potential AF noise sources where one would normally consider noise at a 455 kHz IF a problem in a superheterodyne design.

### Noise on Vcc2

The SL6649-1 requires a low noise Vcc2 supply, ie little ripple. In a pager, using a single cell, Vcc2 is derived from a DC DC converter which often has a high output impedance and may inherently produce a significant output ripple due to the operation of a regulator. Unless reasonable care is taken the sensitivity of the receiver IC may be degraded. If reduced sensitivity due to noise on Vcc2 is suspected connecting a large (>100uF) capacitor on the Vcc2 supply close to the chip will confirm that performance improves when there is less ripple on Vcc2. When this test improves the receiver performance it is necessary to use some or all of the following techniques to reduce the noise level, unless it is possible to fit a very large capacitor in the receiver.

### Loading of The Data Output

One common source of noise on the Vcc2 supply to the chip is large loading of the data output from the device. The data output swings between ground and Vcc2. When current is taken from the data output this is supplied from Vcc2. The increased load on the Vcc2 supply may cause the voltage to drop. This produces a ripple on the supply at the data rate which can degrade the performance. To prevent this problem it is recommended that a 100k resistor is fitted in series with the data output close to the pin. This reduces the effect of any capacitive loading due to the track to the decoder IC and that no more than 1 uA current should be taken from this output. This is adequate to drive most CMOS ICs.

### Noise on Bandgap or Vref

The bandgap and Vref pins are the main voltage references used throughout the receivers internal circuitry. If excessive noise is injected onto these pins the whole receivers performance will be degraded. Particular care should be taken to ensure that these pins are adequately decoupled at both audio frequencies using a minimum of 2.2 uF and at radio frequencies using, typically 1000pF. No circuitry should be biased from these points if the current consumed will contain a varying component within the receiver AF pass band.

### DC DC Converters Ripple Reduction

It is often possible to control the ripple frequency from a DC DC converter so that no components lie in the pass band of the receiver. Most DC DC converter circuits switch at a frequency in the region of 50 to 500 kHz, which is well above the pass band of the receiver. Where a DC DC converter has some hysteresis in its regulator section this will appear as a ripple on the output. One of the factors that determines the ripple frequency is the load capacitance on the output. The larger this capacitance the lower the frequency of the ripple and it is common that the combination of the hysteresis and the load capacitor will produce about 10 mV ripple at a few kHz. It is possible to push the frequency of this ripple above the pass band by using a smaller load capacitor. A separate resistor with a larger value capacitor can be used after the DC DC converter to further reduce the ripple. For example a 2.2 uF load capacitor on the output of the DC DC converter followed by a filter consisting of a 47 Ohm resistor and a 33 uF capacitor will often prove an effective starting point for the design.



## Summary

Audio frequency noise can degrade the performance of the SL6649-1. If a large capacitor on Vcc2 improves the performance of the receiver, Vcc2 noise needs to be reduced to achieve optimum performance. This can be caused by excessive loading of the data output from the chip or by ripple from the power supply. If a DC DC converter is used to generate Vcc2, careful control of the spectrum of the output ripple is required. The bandgap and Vref pins are also sensitive to AF noise. All these potential problem areas can be overcome by careful design.

## RF AMPLIFIERS FOR THE SL6649-1

### Introduction

The SL6649-1 includes an RF amplifier on the chip. If the performance specified in the data sheet is to be achieved the external components of the RF amplifier circuit must be correctly specified and the circuit layout must be good. It is possible to use an external RF amplifier in place of the on-chip amplifier to achieve a lower overall noise figure for the receiver which will improve its sensitivity.

### On Chip RF Amp

A cascode RF amplifier is provided on the SL6649-1, see SL6649-1 data sheet and figure 3. The transistors are biased using the voltage sources (vref pin4 and Vbg pin 5) and a current sink (pin 20) provided by the chip. A DC blocking capacitor is normally required between the input signal source and the base of the first transistor in the cascode, pin 19. This may be used to form part of the input matching network. The output pin17 an open collector, which must be connected to Vcc1 via an inductor to provide proper DC bias. Adequate RF decoupling of the bias and power supply is essential. The output from the RF amplifier is connected to the mixer RF inputs, pin23 and 24 which form a differential input. A DC path must be provided between the mixer inputs for bias reasons.

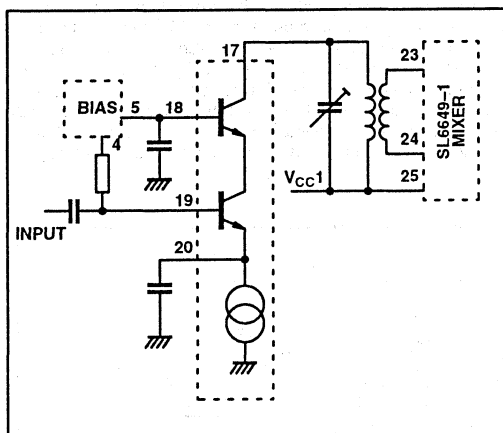


Fig. 3 The SL6649-1 on-chip RF amplifier

## Transformer Matching

Normally a 1 to 1 ratio RF transformer is used to match the RF amplifier output to the mixer input. The primary is the load for the RF amplifier. This can be tuned by a parallel capacitor. Small variations in the input impedance from device to device makes it advisable to make either the transformer inductance or the capacitance variable to allow the circuit to be tuned to the operating frequency. The transformer secondary connects to the differential input on the mixer and provides the required DC path for the bias.

## RF Amplifier Gain

The RF amplifier gain has to be chosen so that the overall system gain is maintained at the correct level, see "Gain distribution in the SL6649-1". The gain of the RF amplifier may be varied by changing the load impedance at the output of the RF amplifier. To a first approximation in the normal operating range the higher the load impedance the higher the gain will be. With a 1 to 1 ratio transformer the load impedance is determined by the input impedance to the mixer and the Q of the transformer.

At a frequency of 153 MHz at GPS we normally use a 1 to 1 transformer with a primary inductance of 100 nH and a Q of about 50 (Toko type 5CE part No.432AN-1211X). This transformer has been used successfully for frequencies between 130 and 180 Mhz.

At lower frequencies it may be necessary to increase the inductance of the transformer. If excessive gain is obtained a resistor in parallel with the primary may be used to lower the load impedance of the RF amplifier and thus reduce its gain. At the top of the SL6649-1 RF amplifiers operating range, 200 MHz, it may be necessary to use a transformer with a higher Q to obtain adequate gain to achieve optimum performance.

## Frequency Response

The tuned load to the RF amplifier forms an RF filter which helps to improve the rejection of signals at tens of MHz away from the wanted channel. This can be important where there are very high level interfering signals, eg 100 MHz FM broadcast transmitters. It is possible to improve this performance by maximising the loaded Q of the RF amplifier load. A lower inductance, higher Q transformer will improve the performance.

A high Q load can also be used to help reduce spurious responses in pager designs where the local oscillator is derived from a multiplier. For instance in a 153 MHz receiver where the local oscillator is derived from a multiplied 51 MHz crystal oscillator there may be spurious responses at 51 MHz, 102 MHz, 204 MHz etc. A high Q circuit will reduce the gain of the RF amplifier at these frequencies and therefore reduce the spurious responses.

**Automatic Gain Control**

The SL6649-1 includes an automatic gain control (AGC) system. An RF signal level detector is included at the input to the mixer, pin 23. When a high level signal is detected the current supplied to the RF amplifier via the current sink is reduced, which causes the gain of the RF amplifier to fall. This reduces the RF input level to the mixer and prevents the mixer becoming overloaded by the high RF signal level. This ensures the receiver continues to work when very high level signals are received which increases the overall dynamic range of the receiver. Without AGC the dynamic range would be significantly reduced and the power consumption of the SL6649-1 would increase significantly when very high level signals are received. It is important that whatever RF amplifier configuration is used the AGC system is still active, ie the current source must be used to control the bias current in the RF amplifier.

**External RF Amplifiers**

An external RF amplifier can be used in place of the on-chip cascode RF amplifier. This can have several advantages:

- Increased flexibility, especially in terms of layout
- Lower noise figure giving improved sensitivity
- Higher operating frequency
- Improved local oscillator isolation from the antenna.

The most common type of off chip amplifier is a simple cascode amplifier. See Fig. 4. It is recommended that this is biased using the on-chip references of  $V_{BG}$  and  $V_R$ . It is also recommended that on chip current source (pin 20) is used. This will ensure that the gain of the amplifier is held constant throughout the operational supply voltages and that the on-chip AGC is active. The load for the transistor is formed by the primary of a transformer and a capacitor resonant at the frequency of operation. The secondary of the transformer is used to provide the required differential input to the mixers whilst also providing the required DC path between the mixer inputs. At 153MHz a suitable low profile, 1:1 100nH transformer can be used (Coilcraft type 1812 No: N2261-A). For applications above 200MHz it is recommended that a transformer with a lower inductance is used, eg. Coilcraft 1812 No: M1686-A (30nH). The gain distribution of the receiver outlined earlier still applies and it is recommended that the gain of the RF amplifier is controlled with the use of a load resistor in parallel with the secondary of the transformer.

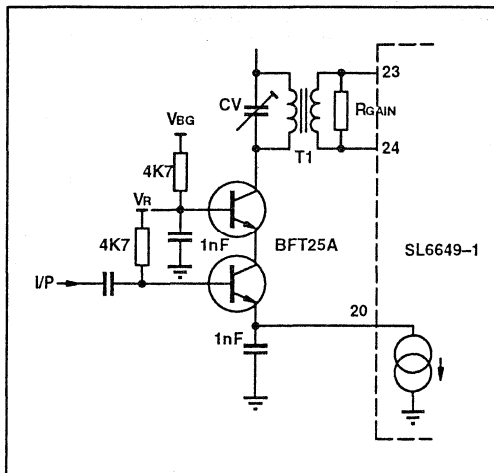


Fig.4 An external RF amplifier for the SL6649-1

**Operation above 200MHz**

The SL6649-1 RF amplifier is specified to operate at frequencies of up to 200 MHz. Above this frequency the gain of the on-chip RF amplifier and mixer both fall so optimum sensitivity can not be achieved using this gain stage. However it is possible to use the device at frequencies above 200 MHz with reduced performance. Alternatively an external RF amplifier in place of the on-chip amplifier will overcome the problems of the on-chip amplifier at high frequencies. A higher local oscillator level may be required to achieve adequate system gain, see notes on "gain distribution in the SL6649-1"

**Alternative Mixer Matching Circuits**

The use of a transformer to match from the RF amplifier to the mixer can prove difficult in some applications where space is very limited due to the relatively large size of readily available transformers. It is possible to use an alternative matching network between the output of the RF amplifier and the mixer. See figure 5. This is known as the transformer-less application circuit.

**Layout**

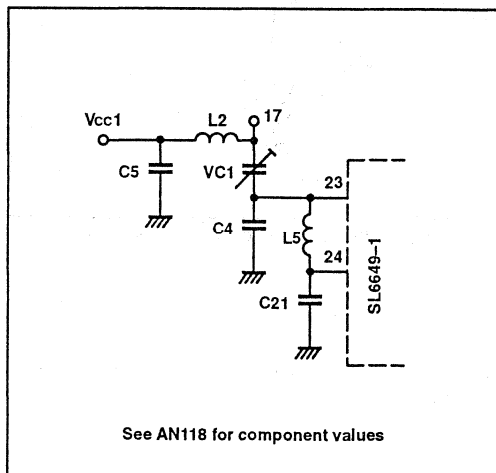
The layout of the RF amplifier section of the receiver is important. Common problems caused by layout faults include: Instability due to the amplifier output being too close to the input

- Noise pick-up from the data output or decoder circuit
- Local oscillator pick-up

See notes on "Layout around the SL6649-1".

**Summary**

The overall performance of a receiver based on the SL6649-1 is dependent on the performance of the RF amplifier. It is possible to use the on-chip amplifier where a highly integrated solution is required. Alternatively an external amplifier can be used for better sensitivity at high frequencies. By careful design of the transformer matching circuit between the RF amplifier and the mixer the gain and frequency response can be optimised to suit the application. Careful layout is required to give a predictable and reliable design.



See AN118 for component values

Fig. 5 Transformerless matching

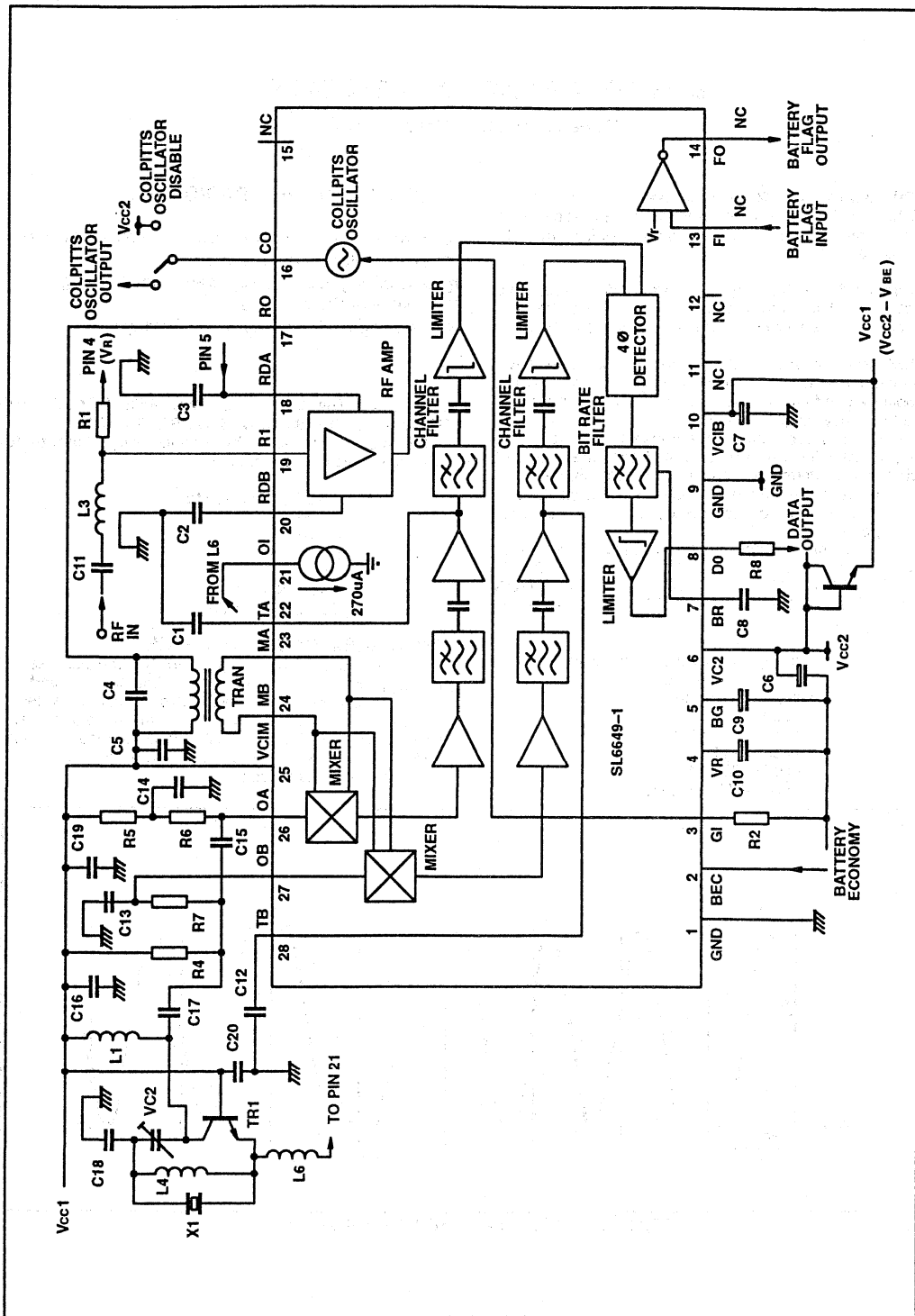


Fig. 6 Circuit diagram of receiver (transformer application)

## LOW COST RADIO DATA RECEIVER

(Supersedes May 1990 edition)

This Application Note describes the use of the GPS SL6659 FM receiver circuit for the demodulation of phase modulated data, now transmitted, in the UK, on BBC Radio 4.

From the first of February 1988 BBC Radio 4 long wave moved from 200kHz down to 198kHz. This new carrier now also contains data using phase modulation as shown in Fig.1.

Obviously this Data must not interfere with normal AM audio transmission quality, hence the data rate is restricted to 25bits/sec and can therefore be contained within the sub audio frequency range of 0 → 50 Hz.

Thirty blocks each minute are transmitted. Starting at the top of the minute with block 0, and ending at block 29 which contains information on time of day, month, year leap year and local offset. Each of these 2 second blocks also contain a CRC (cyclic redundancy check word) error checking code.

For more information about this data transmission medium a document entitled "L.F. RADIO - DATA: SPECIFICATION OF BBC PHASE - MODULATION TRANSMISSIONS ON LONG WAVE" can be obtained from, :-

British Broadcasting Corporation  
Research Department  
Kingswood Warren  
Tadworth  
Surrey KT20 6NP  
United Kingdom  
Tel.0737 832361  
Telex 265781 BBC HQ G

### APPLICATIONS FOR RADIO DATA

- Time + Date + Year Clocks (zero maintenance)
- Time Switching for Lighting
- Advertising 'LED Display' Message Updating
- Control of Street Lights
- Updating Exchange Rates on Displays

### TRANSMISSION DATA BLOCKS ARE LEASED TO GENERAL USERS BY BBC ENTERPRISES LTD.

For more information on licence requirements for reception of radio data contact:-

BBC Enterprises Ltd  
Woodland  
80 Wood Lane  
LONDON  
W12 0TT  
United Kingdom  
Tel 081 576 2563

### THE SL6659 RADIO RECEIVER

This GPS device was designed for general purpose FM radio applications. It contains a limiting IF strip and FM detector which are both utilised in this project. The device also contains an RSSI output and a mixer stage. This device runs from 2.5V to 7.5V and consumes less than 2mA. For a full description see our Personal Communications Handbook.

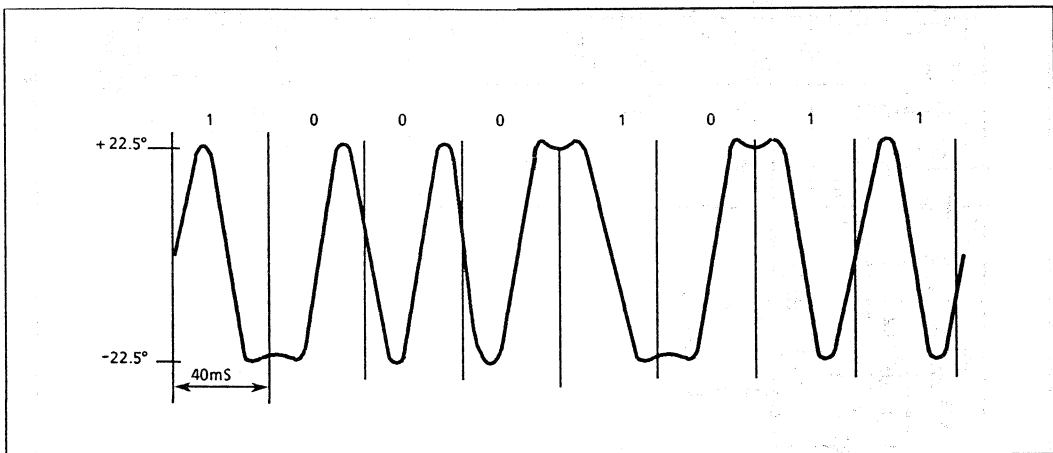


Fig.1 Phase Modulation on BBC Radio 4 Carrier

## USING AN FM DEMODULATOR TO DETECT PHASE SWITCHING INFORMATION

If an FM detector is used to demodulate phase modulation the resulting voltage output will be  $d\phi/dt$  and hence integration is needed to produce a voltage output that will represent phase. Following is a description of how a 1.8V p-p phase signal has been achieved from the  $\pm 22.5^\circ$  phase modulation on Radio 4, using a simple low cost FM demodulator IC (SL6659).

First the SL6659 is a frequency demodulator therefore from an FM signal :-

$$VF_m = V \sin(\omega_c t \pm \Delta\phi \sin \omega_m t), \quad \dots\dots\dots 1.$$

the SL6653 will give a demodulated output

$$V_0 = K \Delta\phi \sin \omega_m t$$

K is a constant determined by the Q of the  $90^\circ$  phase shifting circuit which forms part of the demodulator.

Now as frequency is the rate of change of phase and the modulation from Radio 4 is a phase shift of  $\Delta\phi = \pm 22.5^\circ$ .

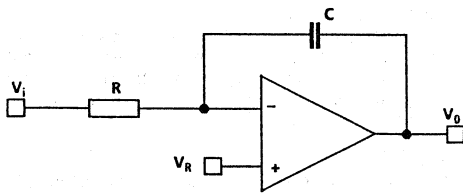
A differentiated output from the SL6659 is obtained of the form.

$$V_0 = K \frac{d}{dt} \Delta\phi \sin \omega_m t \quad \dots\dots\dots 2.$$

Hence integration is required to produce a true phase demodulator

$$V_0 = Kf \int \frac{d}{dt} \Delta\phi \sin \omega_m t. dt \quad \dots\dots\dots 3.$$

A simple op amp integrator following the FM detector is used:-



The output from this integrator is therefore

$$V_{PM} = K \Delta\phi \sin \omega_m t \quad \dots\dots\dots 4.$$

This equation is in the form  $V = Kfc$  where  $fc$  is the equivalent input frequency modulation required to produce  $\pm 22.5^\circ$  phase shift.

$$fc = \frac{\Delta\phi \sin \omega_m t}{\Delta\phi} = \pm 22.5^\circ$$

$$\sin \omega_m t = \frac{1}{40ms} = 25Hz$$

Therefore :-

$$\Delta\phi \sin \omega_m t = \frac{\pm 22.5 \times 2\pi \text{ RAD}}{360^\circ} \times 25Hz = \pm 9.8Hz$$

All we need now is a value for K.

In the SL6659 Data Sheet we are told that an output of about 100mV is obtained when using 1kHz deviation, with a Q of 30 in the quadrature circuit. Our 9.8Hz deviation would therefore only yield 1.95mV output (using the standard application circuit.) To increase this output voltage a quadrature coil Q factor of 200 is used, and gains of x 3 and x 47 have been introduced before the integrator.

From Data Sheet

$$K \text{ with } Q = 30, K = \frac{V_o}{fm} = \frac{100mV}{1K} = 0.1E^{-3}$$

Therefore :

$$K \text{ with } Q = 200, K = \frac{0.1E^{-3} \times 200}{30} = 0.66E^{-3}$$

If we include the two amplifiers of x 3 and x 47 we have a total K factor of  $0.66E^{-3} \times 3 \times 47 = 0.094$ .

Now to find the voltage from the integrator output. We can substitute for K and  $\Delta\phi \sin \omega_m t$  in equation 4.

$$\text{This gives } V_{PM} = 0.094 \times \pm 9.8Hz$$

$$\therefore V_{PM} = 1.84 \text{ V. (p-p)}$$

We can see from the above that the output voltage is dependant on the Q of the inductor used in the quadrature coil and also the gain of the op-amp before the integrator.

### COMPLETE CIRCUIT DESCRIPTION. AERIAL (see fig.2)

The 198kHz carrier from BBC radio 4 is received by the ferrite rod antenna and tuned using a 300pF in parallel with a 22pF variable capacitor. The wire used to wind the aerial is 36SWG.

The tuning capacitor should be adjusted for maximum p-p amplitude of 198kHz at TP1.

## BUFFER

The signal from the aerial is fed into a simple 'J' FET buffer. This provides a high impedance input to maintain the Q of the aerial and also a low impedance output to drive the crystal filter input.

## CRYSTAL FILTER

This is a special crystal which has been produced specially for Radio data applications. Due to the low frequency of Radio 4 the signal is prone to interference from switch mode power supplies. These are found mainly in TV sets and computer monitors.

With this crystal replaced by a link the radio will fail to work consistently at a distance of about a metre from most computers. When the crystal is in circuit the radio functions within a few cm of most computers or TV sets.

The series resistor reduces the Q of the crystal to allow adequate bandwidth for the modulation to pass through without distortion.

198kHz crystal filters can be obtained from:-

AEL Crystals Ltd.  
Worth Corner  
Turners Hill Road  
Surrey  
Pound Hill  
Crawley  
West Sussex RH10 7SL  
United Kingdom  
Tele (0293) 882299

The crystal is series resonant at 198.000kHz with an overall tolerance of  $\pm 100$  ppm. It is encapsulated in a HC-51/u holder with an earth lead soldered to the top.

## SL6659

The GPS SL6659 is used to limit the signal from the crystal to produce a 198kHz square wave at pin 1 of the device. This square wave is phase shifted by the quadrature tuned circuit and fed to the FM demodulator. This signal is compared with the in phase signal to produce a demodulated output  $d\phi/dt = 10\text{mV p-p}$  from pin 3 of the device.

The source impedance of this output is 40k ohm.

This device can be obtained from the offices listed at the back of this Applications Note.

## QUADRATURE COIL

RS part number for the former is RS 228-214, RM6/160.

This is a critical part of the radio design. Care should be taken with the design of this inductor as it is working at a high Q factor, (200) therefore drift due to temperature, winding settling and other aging effects are important. For the prototype radio 60 turns of 36SWG was used.

## THE OUTPUT TRANSISTOR

The SL6659 output impedance is 40k Ohm therefore a transistor is required to drive the input of the Sallen and Key filter. The common emitter configuration used also provides a DC gain of x 3. The DC voltage on the collector of this transistor is used to set the tuning of the quadrature circuit. When adjusted for resonance at 198kHz the output from this transistor will jump from 1.2V to 4V. The slug in the inductor can then be adjusted so the test point TP2 sits at 3V DC. (See Fig. 2)

## THE SALLEN AND KEY FILTER

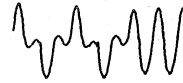
One quarter of the LM324 quad op-amp is used as a low pass filter. This filter prevents spurious signals such as audio AM to PM conversion or noise spikes being amplified and fed to the integrator. These signals would cause distortion and rapid DC shifts on the  $\phi$  output.

## AMPLIFIER LM324

The signal from the filter is now amplified by x 47. This gain can be adjusted to compensate for the Q factor obtained from the quadrature coil (adjust 47k Ohm feedback resistor).

NOTE: LP324 should not be used

A clean  $d\phi/dt$  signal should now be seen. AT TP4.



Signal between  
1.3V and 2V P-P

If this signal is distorted,



check the Sallen and Key filter bandwidth, the resistor in series with the crystal or the 330 $\mu\text{f}$  smoothing capacitor, which provides the DC reference for the amplifier.

## INTEGRATOR

This is a conventional capacitor feedback integrator with one small exception. The input DC reference is referred right back to the tuning of the quadrature detector. Therefore any drift in this tuned circuit will be automatically tracked out. The integrated output is now the phase signal shown in Fig. 1.

## THE COMPARATOR

The signal from the integrator will be between 1 and 3V p-p amplitude and has a DC component which can drift between 1.5 and 4 volts. The comparator removes this DC drift by comparing the smoothed DC signal with the original unsmoothed input.

## THE OUTPUT

The output signal from TP6 is capable of driving TTL or CMOS inputs. The LED helps as a visual indicator, also a small piezo-electric sounder across this output, aids in alignment, as the empty two second data packets are clearly audible.

## THE OUTPUT DATA see Fig.1.

The output data comprises of two frequencies 12.5Hz and 25Hz. From these two frequencies both data and clock can be recovered.

Clock recovery is best handled using a micro processor sampling the phase waveforms and looking for edges. When the clock is recovered the data is sampled to see if there is a falling or rising edge within the middle of each 40ms clock period. A falling edge will be a '1' and a rising edge will be a zero.

**CONCLUSION**

Using the methods described a radio data receiver can be built at a cost far below anything currently available. Some field trials were performed in the north and south of England. The radio operated successfully with only minor aerial direction adjustment.

A wide range of products can be produced using radio data, from simple time switches to complex data transmission systems, covering the whole of the U.K.

For volume applications it is more cost effective to combine the radio data product onto just three or possibly two chips.

GEC Plessey Semiconductors have experience with these types of data and CRC error checking systems. They would be pleased to review any volume applications, from simple display drive to complex power control systems. GEC Plessey Semiconductors range of Semi-custom Arrays range from 500K gates using CMOS to mixed analog and digital arrays on low power bipolar technologies.

**OTHER GEC PLESSEY DEVICES SUITABLE FOR RADIO DATA RECEPTION**

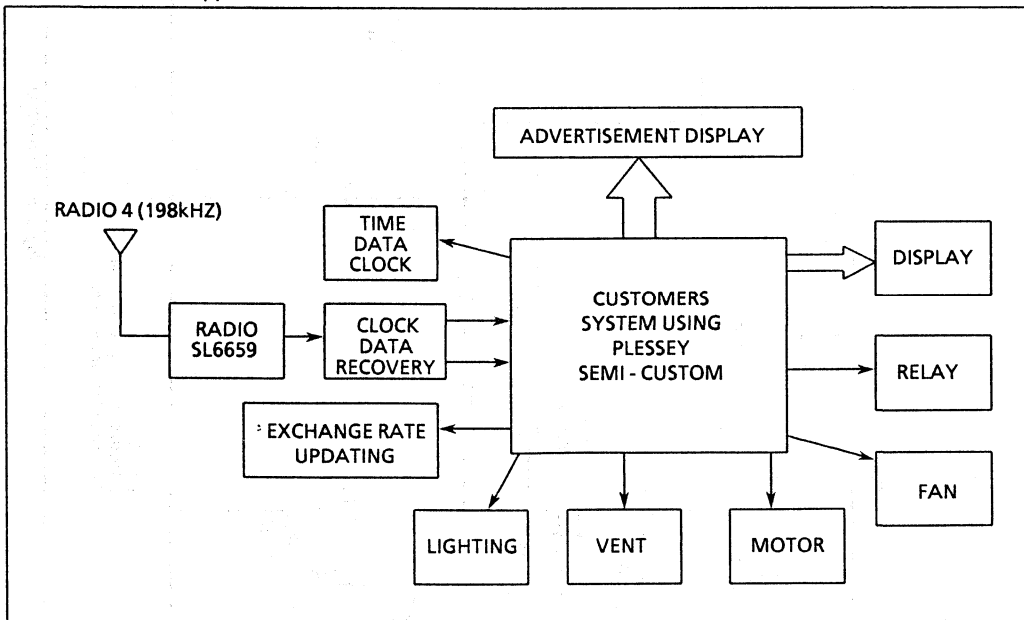
- SL560 Amplifier
- SL561 Amplifier
- SL562 Amplifier
- SL6270 AGC Amplifier
- SL6601 Phase Locked Loop for FM Detection

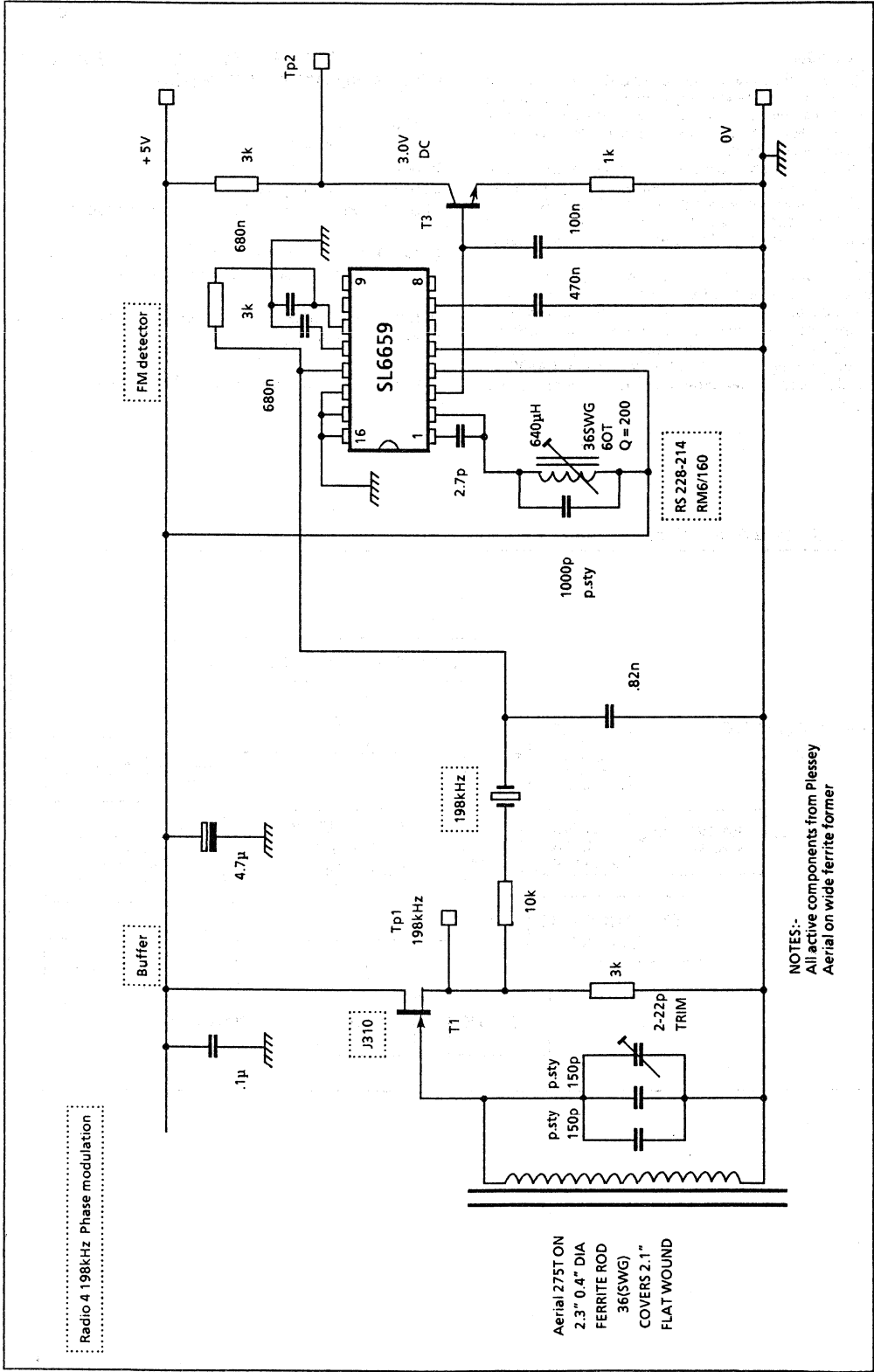
[ Ask also for the Personal Communications Hand Book and Semi-Custom Product Guide ]

**Acknowledgments** to GEC Plessey Semiconductors Radio Design Group.

BBC Research Department and AEL Crystals.

Radio Data Applications





Radio 4 198kHz Phase modulation

Buffer

FM detector

Aerial 275TON  
 2.3" 0.4" DIA  
 FERRITE ROD  
 36(SWG)  
 COVERS 2.1"  
 FLAT WOUND

NOTES:-  
 All active components from Plessey  
 Aerial on wide ferrite former

Fig 2. Radio Section



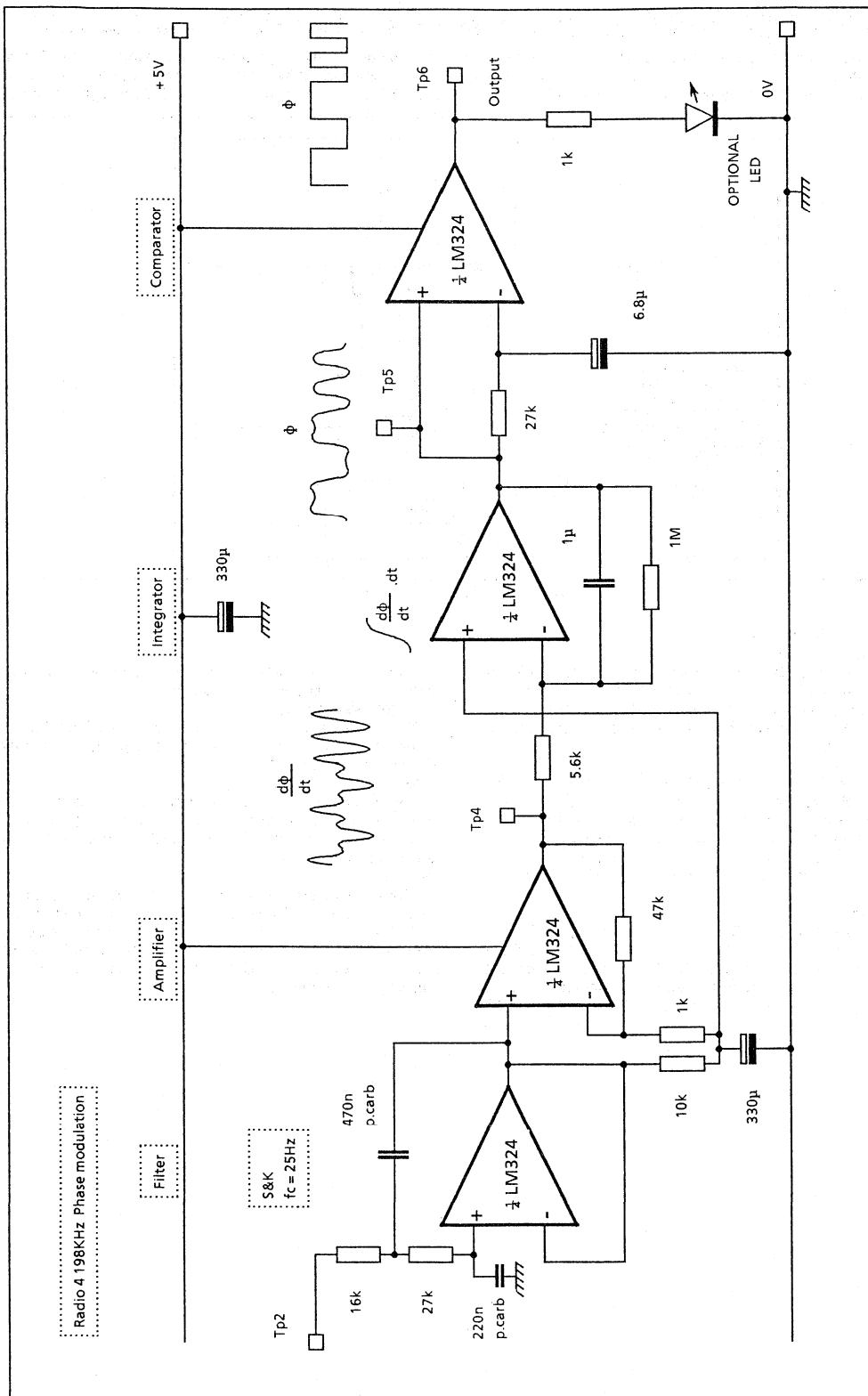


Fig 3. Radio Data Receiver Signal Processing

This application note describes a single conversion superhet receiver which operates at a nominal frequency of 173MHz. The nominal supply voltage is 5V. The circuit illustrated in Fig. 2 was designed for limited range reception of speech and data and achieves an input sensitivity of about 300nV for 12dB sinad. Fig. 1 is a block diagram of the SL6659 integrated circuit.

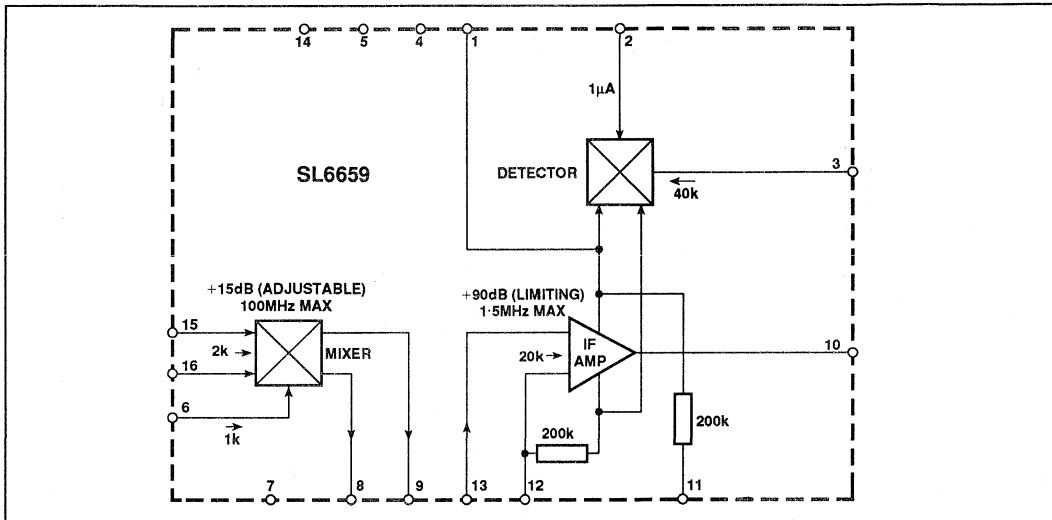


Fig. 1 Block diagram of SL6659

## DESCRIPTION (FIG. 2)

### RF amplifier.

This comprises a BFS17 transistor, TR2, configured in common emitter mode. The input is matched to a 50Ω source impedance by L6 and C13. The output load is a capacitor tapped tuned circuit consisting of L5, C14, C15, and the input capacitance of the mixer.

### Mixer.

The mixer input is fed from the RF amplifier output as described above. The local oscillator signal is obtained from a crystal oscillator via C4. DC bias is provided from the internal band gap reference via R3 to one LO input and decoupled by C5; the other input is biased via R4. The mixer output is terminated by R7 to provide the correct source impedance for the ceramic filter, F1.

### Local Oscillator.

The external transistor, TR1, is biased from  $V_{CC}$  via R1 and the base is decoupled by C23. The oscillator feedback circuit comprises a capacitor tap C1, C2, C3 and a series resonant crystal which is shunted by an inductor L3, to suppress oscillation at the crystal fundamental frequency. The emitter is DC

connected to ground by inductor L2; R2 is connected in parallel to damp out any spurious resonances.

### Voltage Reference.

The band gap reference is used in this application to bias the mixer inputs. It must be well decoupled to prevent oscillation. This is achieved by C11.

### IF Amplifier.

The limiting amplifier is fed from the mixer output via a ceramic filter F1. Its input and feedback decoupling is provided by C6 and C7 respectively. R6 provides the correct output termination for the filter.

### Detector.

The detector input is connected internally to the limiting amplifier output and also via a quadrature network consisting of C18, C17, L4 and R8. The audio output is filtered to remove the IF component by the detector output resistance and C19. The output bandwidth is limited by the addition of an RC network consisting of R9 and C20.

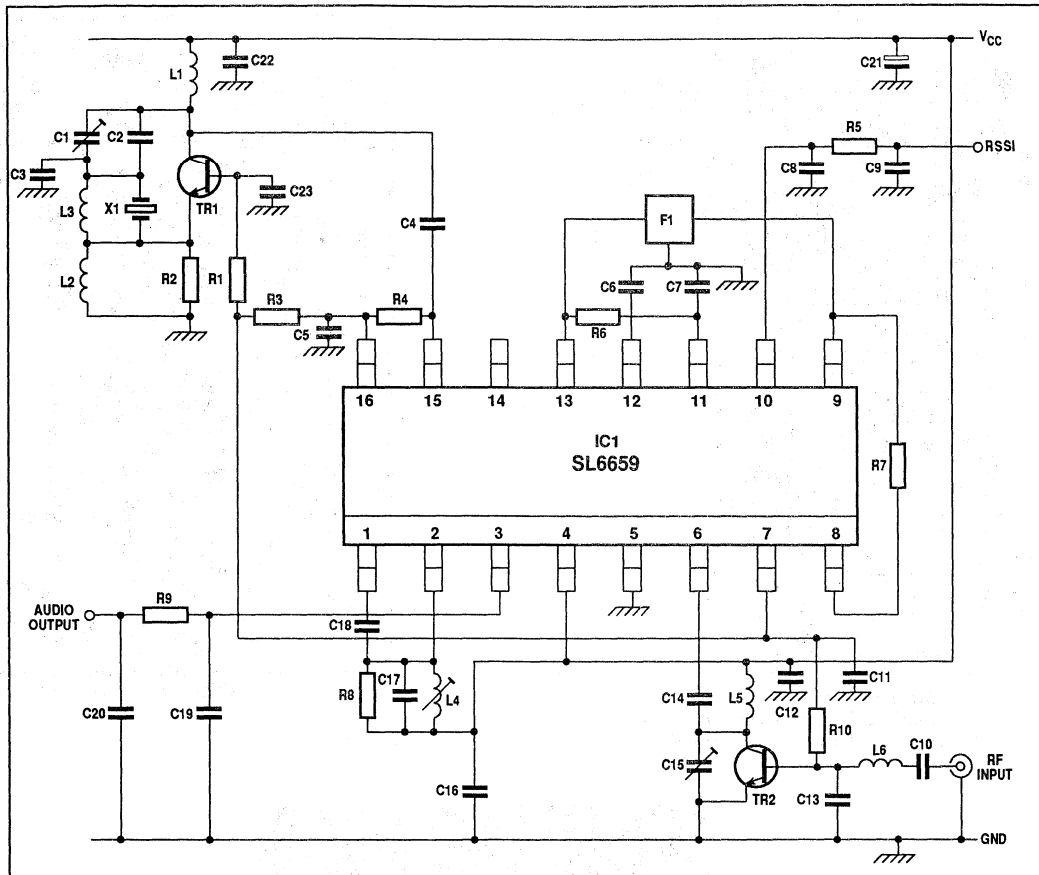


Fig. 2 SL6659 VHF superhet application circuit

## Component Values

R1	180k $\Omega$	L1	100nH	C1	1-5pF	C13	3-9pF	IC1	SL6659
R2	1k $\Omega$	L2	470nH	C2	5-6pF	C14	5-6pF	X1	173MHz Crystal
R3	10k $\Omega$	L3	220nH	C3	5-6pF	C15	2-20pF		
R4	470 $\Omega$	L4	390 $\mu$ H	C4	5-6pF	C16	220nF	F1	455kHz Ceramic
R5	1k $\Omega$	L5	100nH	C5	10nF	C17	330pF		
R6	1-5k $\Omega$	L6	100nH	C6	220nF	C18	10pF		
R7	1-5k $\Omega$			C7	220nF	C19	270pF		
R8	33k $\Omega$			C8	10nF	C20	4-7nF	TR1	BFS17
R9	1k $\Omega$			C9	100nF	C21	2-2 $\mu$ F	TR2	BFS17
R10	150k $\Omega$			C10	1nF	C22	1nF		
				C11	220nF	C23	1nF		
				C12	1nF				

## PCB Layout.

The layout of the pcb is shown in Fig. 3. This has been designed to make the maximum use of surface mount components and tuneable inductors have been eliminated except for one (L4) used in the detector quadrature network.

## Receiver Alignment.

The local oscillator is monitored by loosely coupling a frequency counter to the L.O. output and if necessary C1 is adjusted. The output of the ceramic filter is monitored on an oscilloscope and an unmodulated RF signal of about -50dB is fed into the RF input. Capacitor C15 is adjusted for a maximum amplitude 455kHz signal on the oscilloscope.

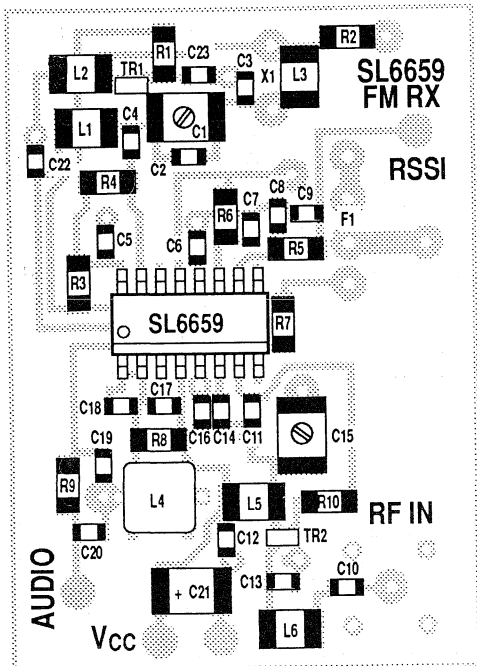


Fig. 3 PCB component layout. Scale = 2:1.  
 NOTE: X1, F1 and the RF connector are through-hole mounted from the ground plane side.

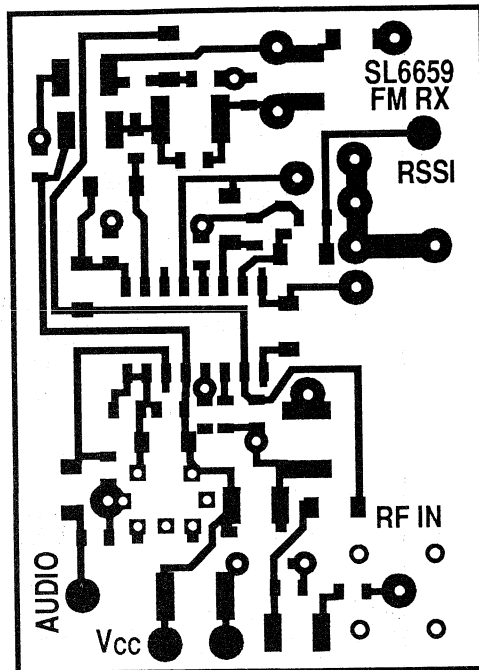


Fig. 4 PCB track. Scale = 2:1.

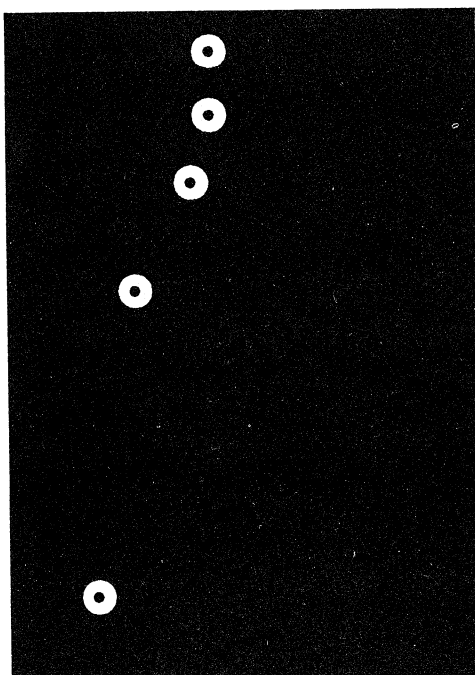


Fig. 5 PCB ground plane. Scale = 2:1.

# Section 9

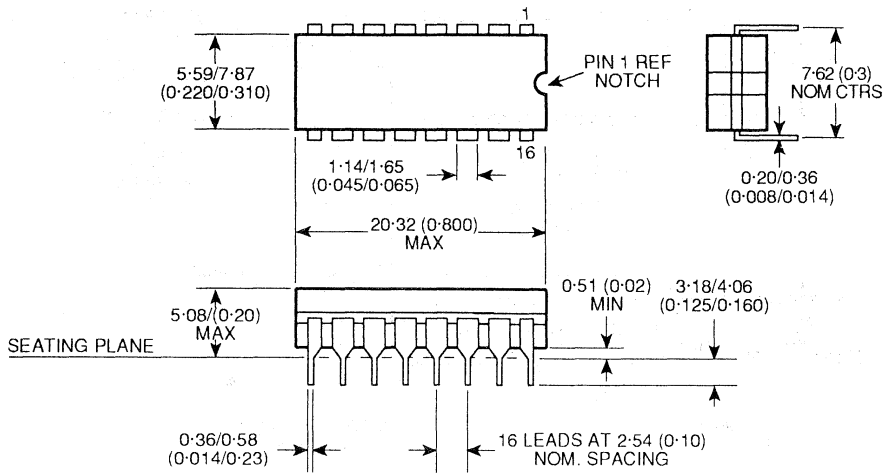
## Package Outlines

**NOTES**

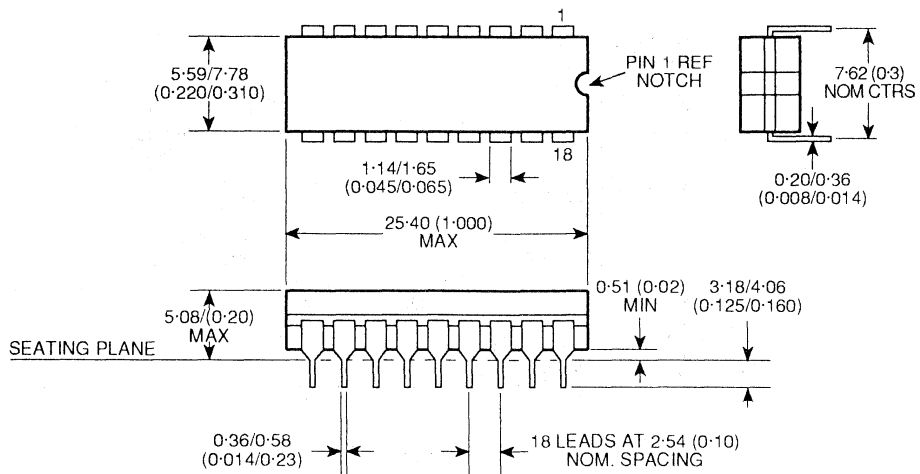
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.



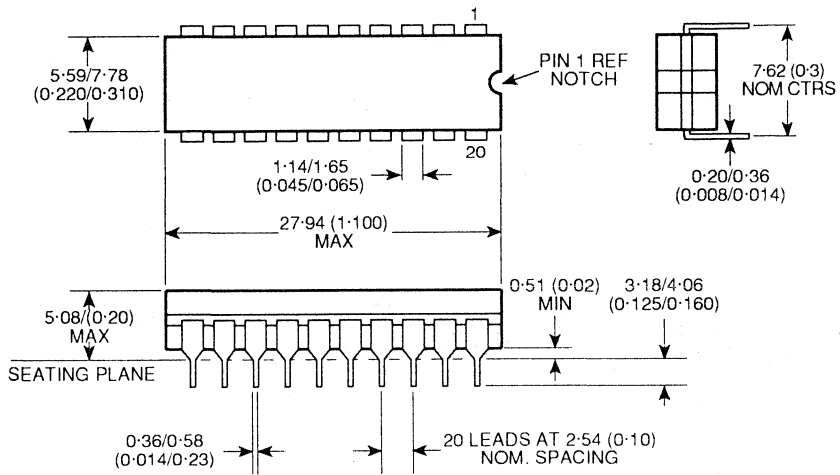




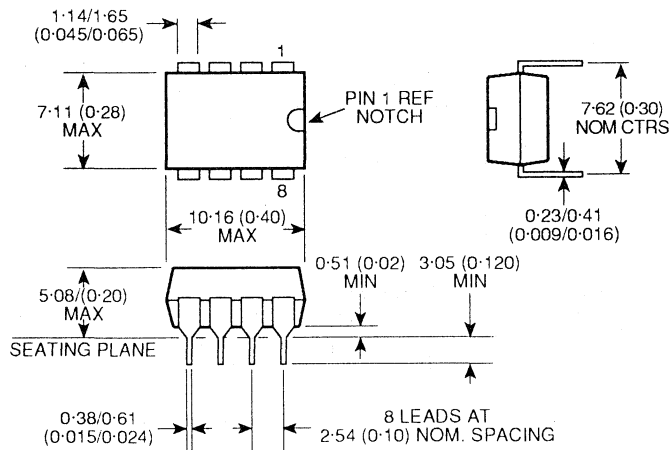
16-LEAD CERAMIC DIL - DG16



18-LEAD CERAMIC DIL - DG18

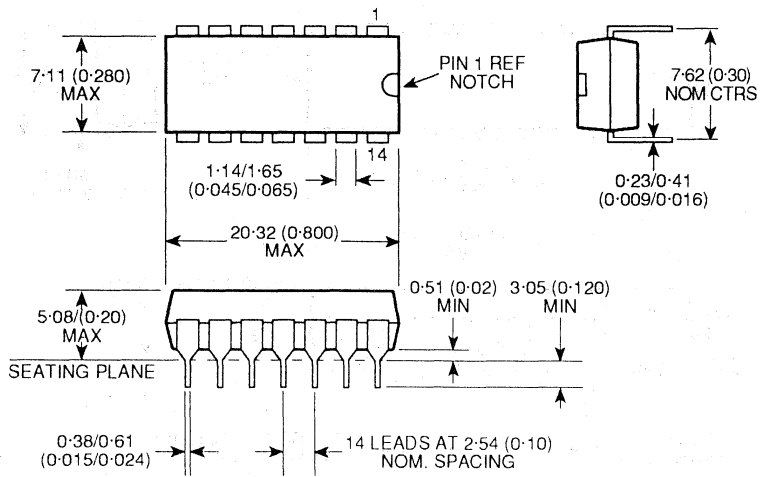


**20 LEAD CERAMIC DIL  
CERDIP - DG20**

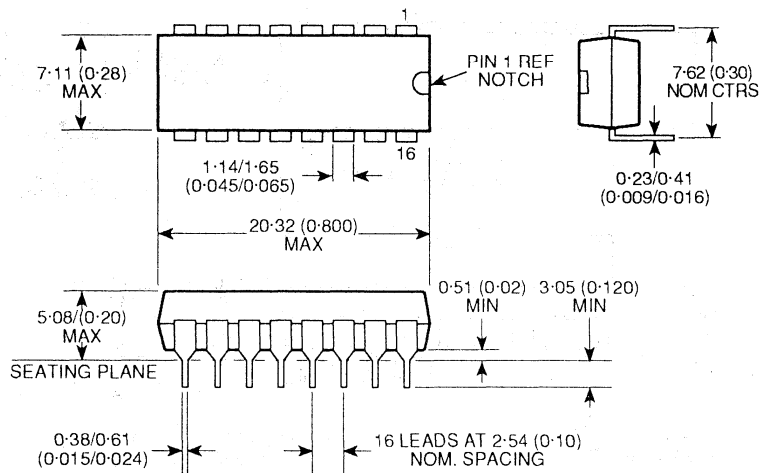


**8-LEAD PLASTIC DIL - DP8**

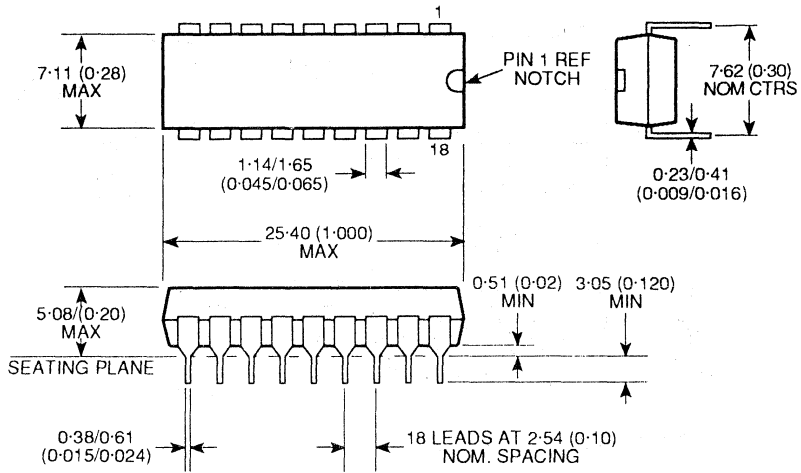




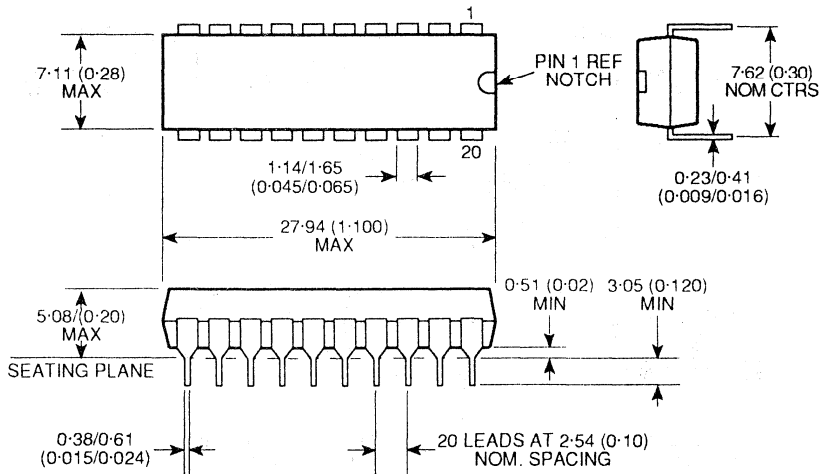
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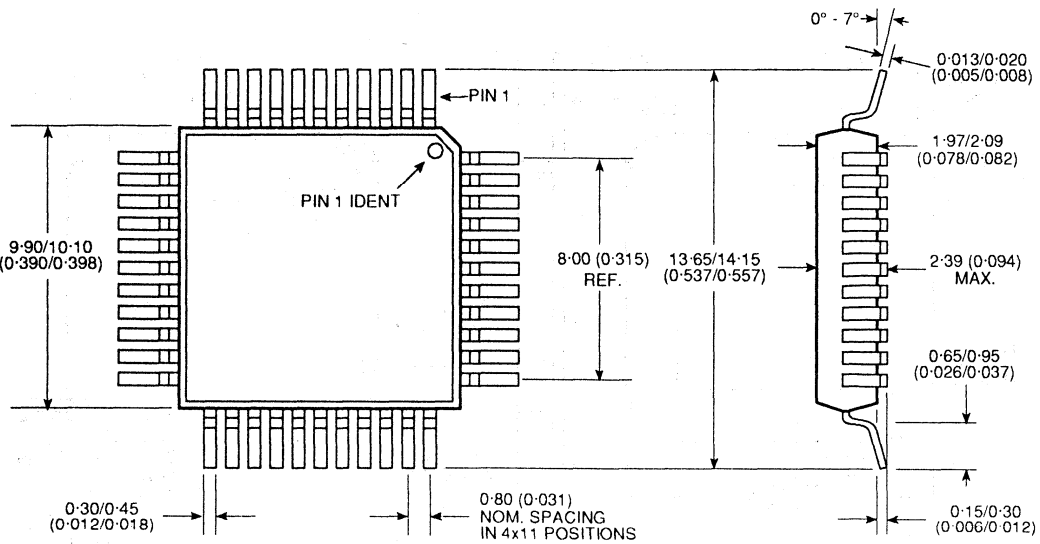
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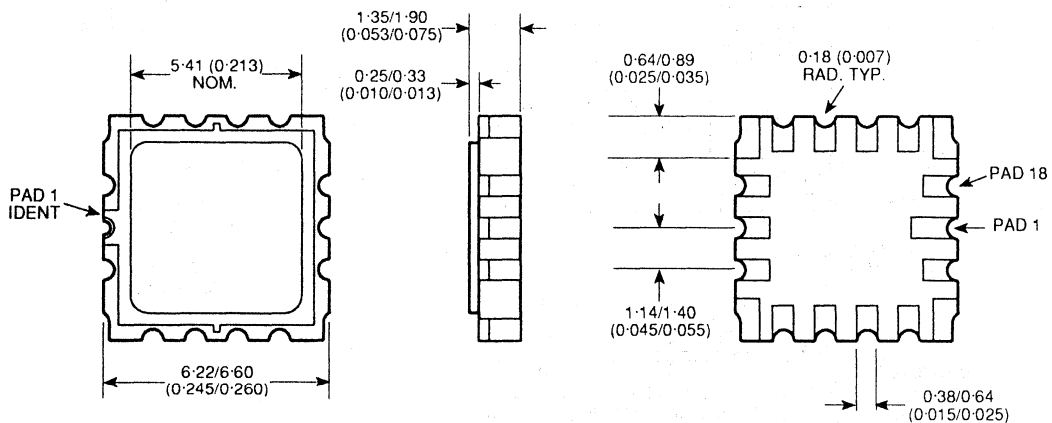
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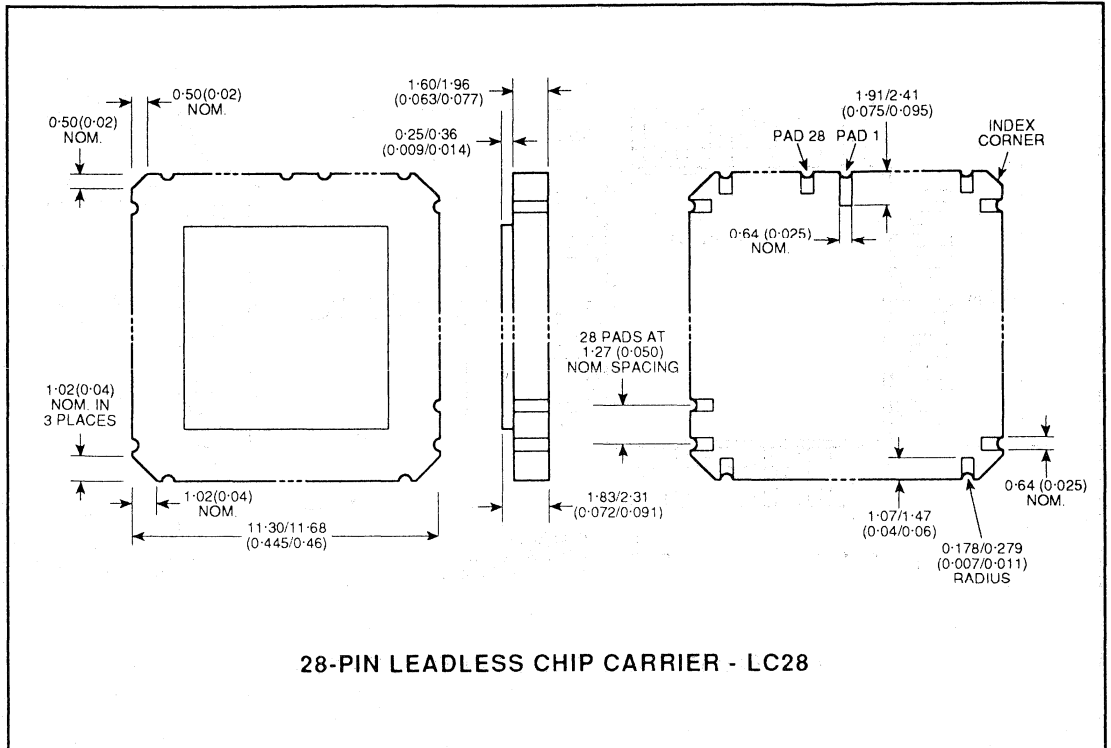
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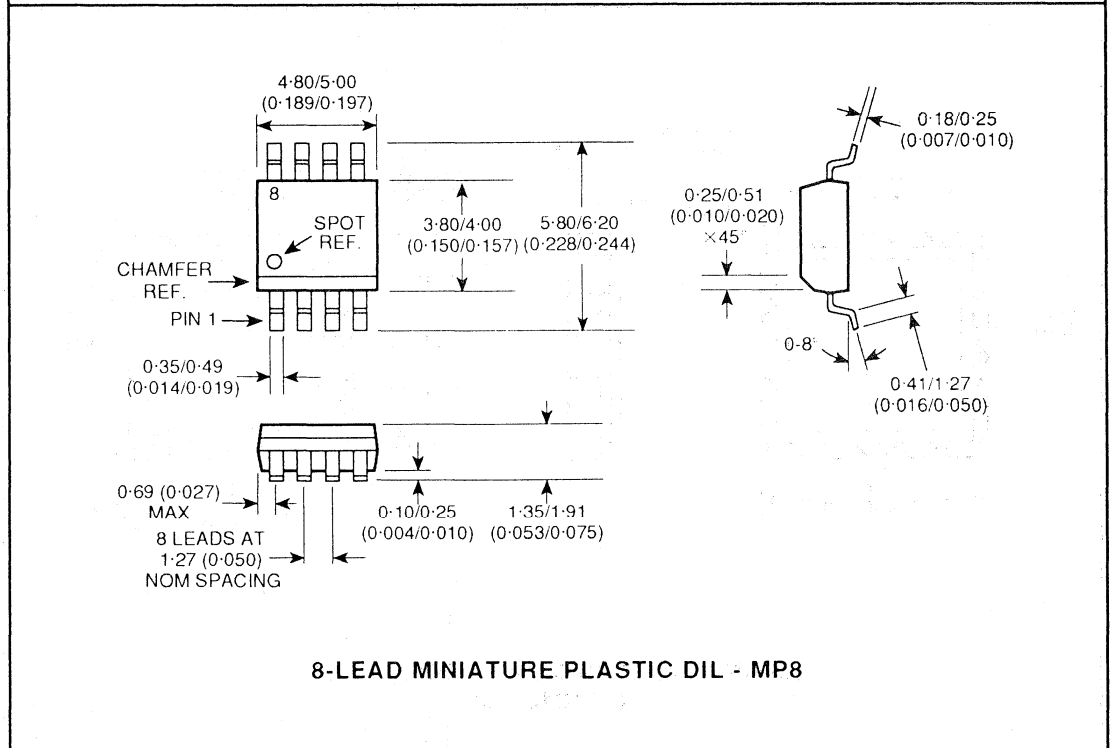
**44-LEAD PLASTIC QUAD FLATPACK - GP44**



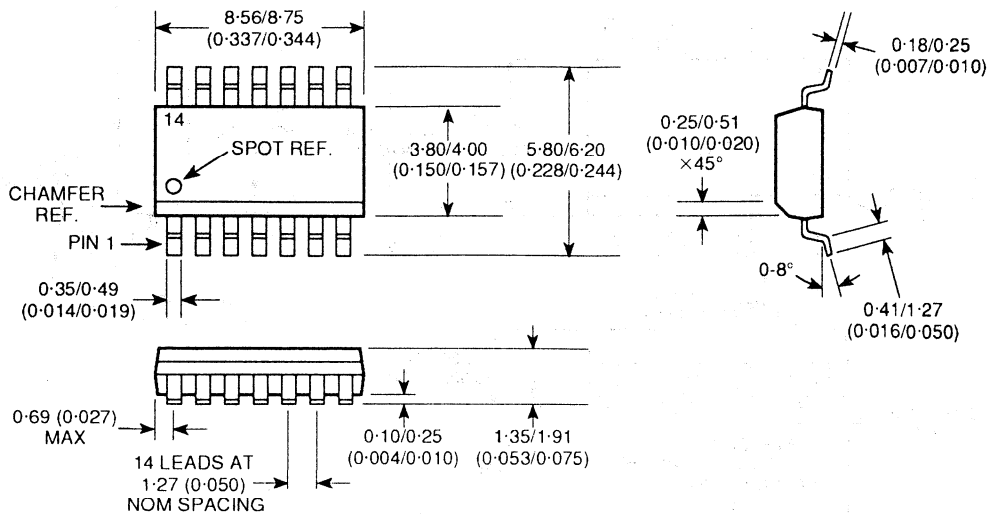
**18-PIN LEADLESS CHIP CARRIER - LC18  
(HERMETIC)**



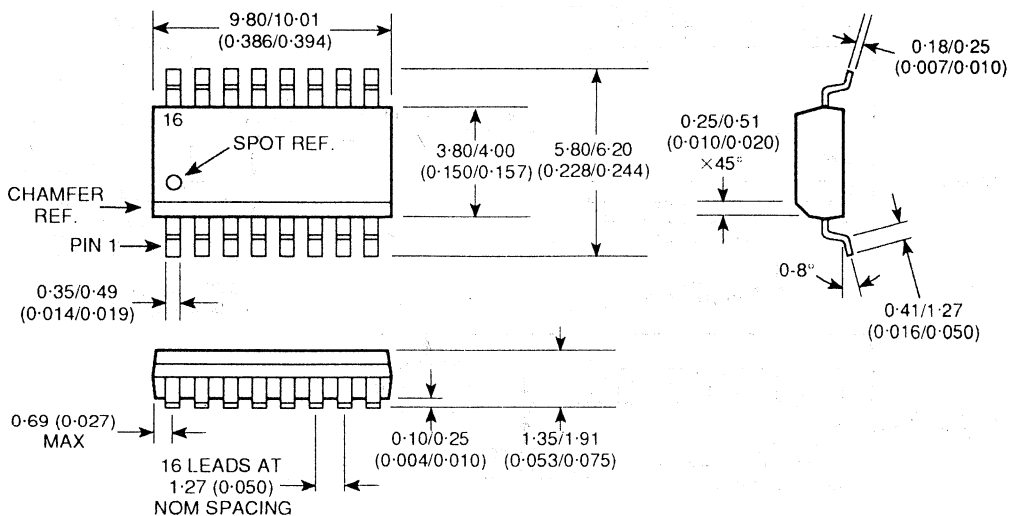
28-PIN LEADLESS CHIP CARRIER - LC28



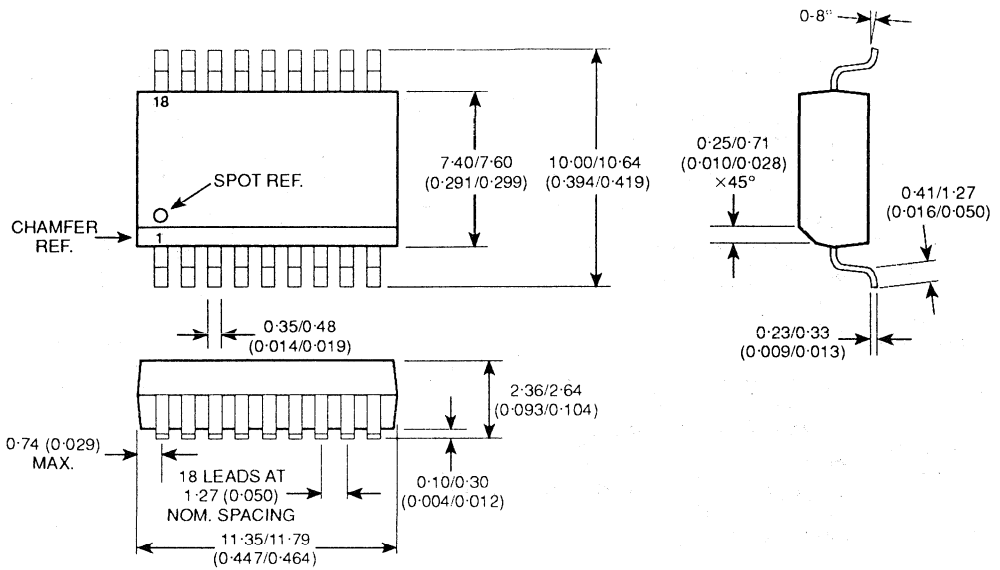
8-LEAD MINIATURE PLASTIC DIL - MP8



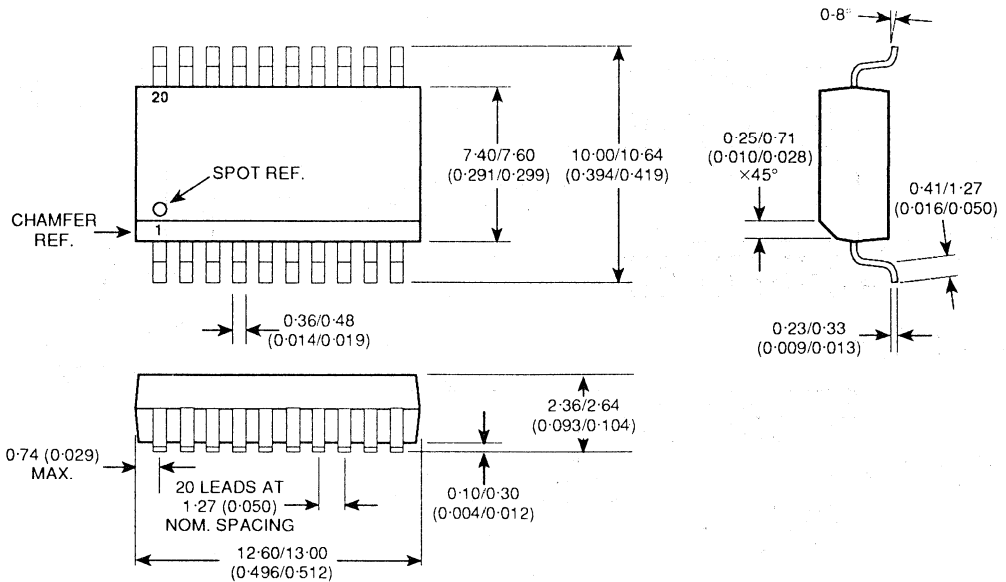
**14-LEAD MINIATURE PLASTIC DIL - MP14**



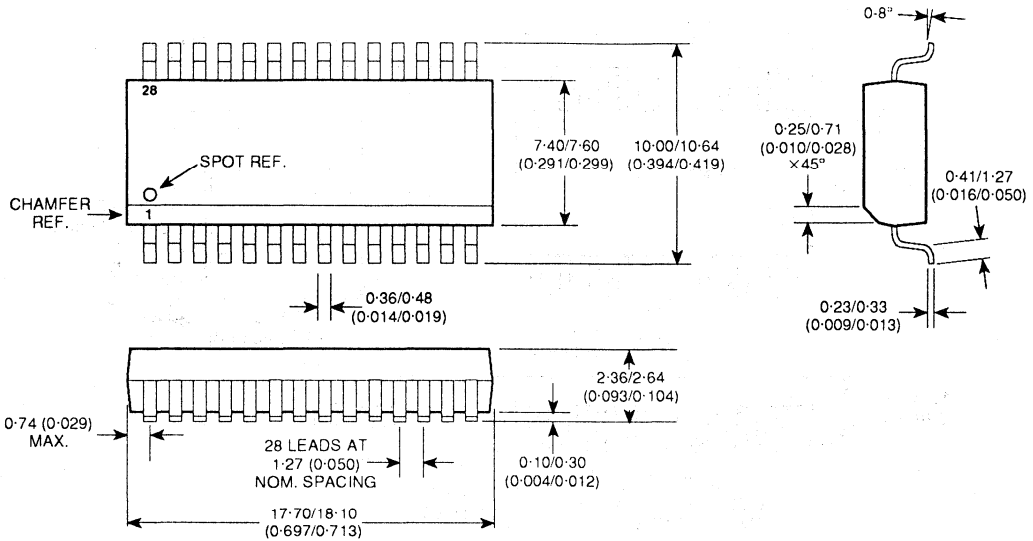
**16-LEAD MINIATURE PLASTIC DIL - MP16**



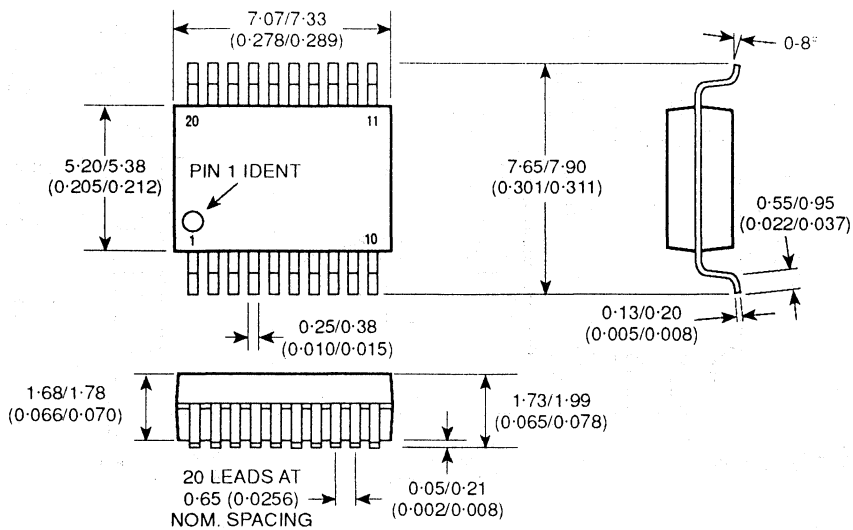
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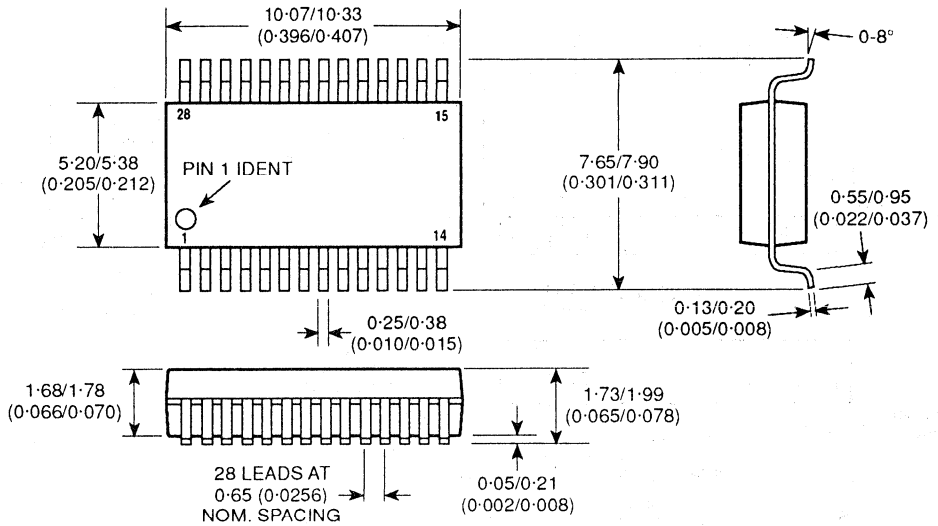
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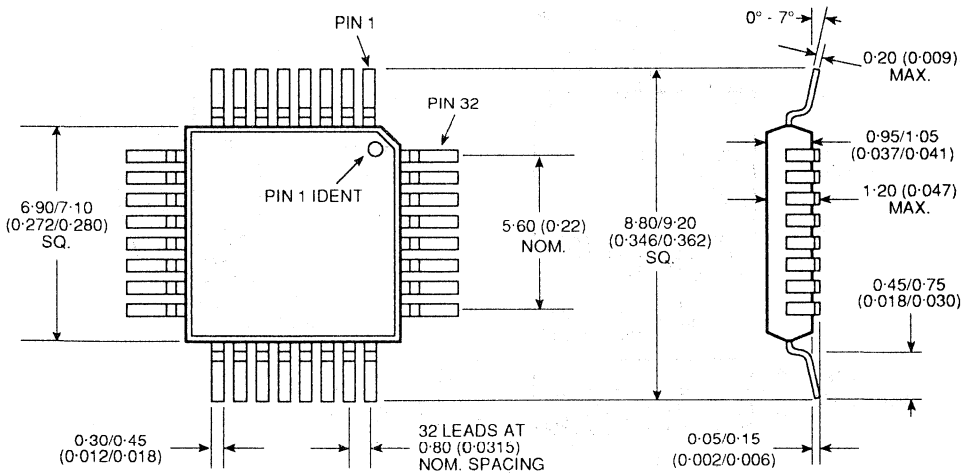
**28-LEAD MINIATURE PLASTIC DIL - MP28**



**20-LEAD SHRUNK MINIATURE PLASTIC DIL - NP20**



**NP28 SSOP PACKAGE**



**32-LEAD THI PLASTIC QUAD FLATPACK - TP32**



# Section 10

## GPS Locations



1. The first part of the document discusses the importance of maintaining accurate records of all transactions and activities. It emphasizes that this is crucial for ensuring transparency and accountability in the organization's operations.

2. The second part of the document outlines the various methods and tools used to collect and analyze data. It highlights the need for consistent and reliable data collection processes to support informed decision-making.

3. The final part of the document provides a summary of the key findings and recommendations. It stresses the importance of ongoing monitoring and evaluation to ensure that the organization remains effective and responsive to changing circumstances.

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